INNOVATIONS IN BACKPANE DESIGN

By Drew Berding

The words "innovation" and "backplane" are rarely used in the same sentence. In fact, some engineers assume that all that is needed to verify the functionality of a backplane is an ohmmeter. As long as there is a good electrical connection between the corresponding pins at each slot, the backplane can do its job. However, VMEbus backplane technology has been (and still is) the focus of a lot of innovations. In this article Drew provides a history of the most significant backplane innovations that have been introduced since the VMEbus standard was introduced, and then he gives us a peek into the future.

One of the cleverest early innovations in VMEbus backplane design was conceived by Performance Technologies, when they came up with VME64 concept. They used the 31 address lines (A01-A31) plus the LWORD* signal (which were all inactive during the data transfer portion of the bus cycle) as data lines D32-D63. This doubled the VMEbus bandwidth from a theoretical maximum of 10 MHz (40 Mbytes/sec) to a theoretical maximum of 80 Mbytes/sec.

The 2eVME concept

Subsequently, Force Computer introduced another significant innovation with their 2eVME concept. It used both the rising and the falling edges of the data strobes to signal valid data. Prior to that, the data strobe signaling required a bandwidth twice that of the data lines, thus limiting the maximum data transfer rate. The 2eVME protocol doubled the theoretical maximum bandwidth again, raising it from 80 Mbytes/sec (10 MHz) to 160 Mbytes/sec (20 MHz).

The VME320 concept

In spite of these innovations, the physics of conventional VMEbus backplanes prevented faster data transfers. Problems included:

- transmission line effects
- long bus settling times
- long bus propagation delays

Since the laws of physics could not be changed, Arizona Digital proposed an alternative strategy — in the form of a radically different "radial wiring scheme" for interconnecting the slots on the VMEbus backplane. All backplane signals propagate to the *center* of the backplane, and then from the center back out to all of the slots. They called this new approach VME320.2

When driving a VME320 backplane, each VMEbus board sees the "hub" of this radial backplane as a "lumped" capacitive load, which it drives through the serial inductance of the trace between its own board slot and the hub — in effect, a low-pass LC filter.

This low pass filter eliminates an important source of signal skew — the "hesitation" seen as each VMEbus signal makes its transition from low to high. Since the voltage level during this hesitation is slightly different at each board slot of a conventional VMEbus backplane, some boards in the system might see the voltage level during this "hesitation" as being high, while others might see it as being low. If the backplane is long (such as a 21-slot backplane) the hesitation time will be long, and there will be a large apparent "skew" between arriving transitions at different board slots. However, because VME320 signal transitions rise continuously through the threshold region (without a hesitation) this major source of skew is eliminated.

Reduced skew greatly improves the performance of the 2eSST (two edge Source Synchronous Transfer) protocol1, since skew is the primary constraint on how fast that protocol can transfer data over the VMEbus. By using the VME320 backplane in conjunction with the 2eSST protocol, the data transfer rates can be increased by a factor of four — from 160 Mbytes/sec to about 640 Mbytes/sec.

Improving on the VME320 concept

However, the "worst-case" LC low-pass filter (which is determined by the serial inductance of the longest trace, combined with the lumped capacitance at the center of the backplane) prevents higher data transfer rates by imposing a propagation delay, and by increasing the rise-time of the backplane signals.

In order to reduce this performance constraint, Arizona Digital has developed a technique to reduce the trace inductance

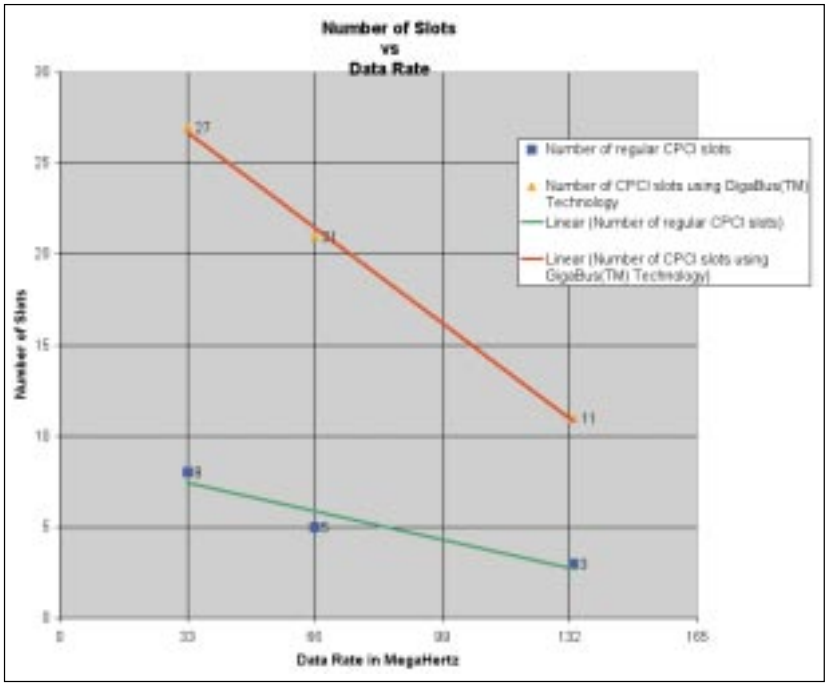

Figure 1

between each board slot and the hub at the center of the backplane. This is accomplished with a negligible effect on the lumped capacitance at the hub2. The greatly reduced LC product:

- reduces the delay by about 33%
- shortens the rise time by about 33%
- increases the bandwidth by about 50%

This reduced-inductance technique permits VMEbus data transfer rates as high as 1.066 Gbytes/sec, while at the same time maintaining compatibility with all existing VMEbus boards.

Side benefits of this design technique (compared to conventional VMEbus backplanes) are:

- greatly reduced crosstalk
- inherent hot-swappability
- a reduced number of PCB layers
- reduced cost

Improving the slot-bandwidth product in CompactPCI systems

The CompactPCI standard has also been the target of innovations. As is well known, CompactPCI suffers from a limited slot-bandwidth product — the larger the number of slots, the lower the bandwidth. For example:

- at 33 MHz only 8 slots are allowed
- at 66 MHz only 5 slots are allowed
- at 133 MHz (which is currently under consideration) only 2 or 3 slots are allowed

A bus bridging scheme can be used to provide more slots. However, this uses up some of the already-limited number of bus loads on each bus segment. The use of such a bridging scheme on 133 MHz CompactPCI systems is obviously of questionable value.

To solve this problem Arizona Digital has developed a backplane design based on *GigaBus*[3] technology that uses an *active boost circuit* at the center of the backplane to assist the weak PCI drivers on the CompactPCI boards in driving the backplane signal lines. With this boost circuit:

- up to 11 slots can be supported at 133 MHz
- up to 21 slots can be supported at 66 MHz
- up to 27 slots can be supported at 33 MHz

Note: 24 is the maximum number of VMEbus slots that will fit within a 24-inch-wide telecom relay rack.

This boost circuit improves the slot-bandwidth product of CompactPCI backplanes by a factor of four over conventional CompactPCI backplanes, as shown in Figure 1.

Using buried series resistors on VMEbus backplanes

This same active boost circuit can be supplemented with another technique (buried series resistors) to further increase the bandwidth of VMEbus backplanes. Each signal line in the backplane has a buried series resistor at the point where the signal line joins the common point in the center of the backplane. This series resistor has a value that approximates the characteristic impedance of the signal line.

When the driving VMEbus board produces a signal transition, that transition propagates along the radial signal line to the center of the board, where its energy simultaneously:

- triggers the active boost circuit
- is absorbed by the series resistor

The absorption by the series resistor eliminates any reflection back toward the driving board, thus keeping the signal waveform on that board's radial signal line as clean as the waveforms on all of the other radial signal lines. The resulting backplane signal waveforms are so clean that they can support data transfers at rates up to 2 Gbytes/sec!

The addition of these series resistors also provides a side benefit — it shifts the power dissipation from the active boost circuit to the passive resistors.

The performance benefits of the active boost circuit and the buried resistors are startling, and must be seen graphically to be fully appreciated. Figure 2 shows the VMEbus bandwidth versus the anticipated year of introduction for these new two new backplane design techniques. The rate of increase is so steep that it curves upwards — even on a logarithmic scale!

Additional work that needs to be done

Bandwidth is not the only problem that needs to be solved. Figure 3 shows some of the areas that still need improvement.

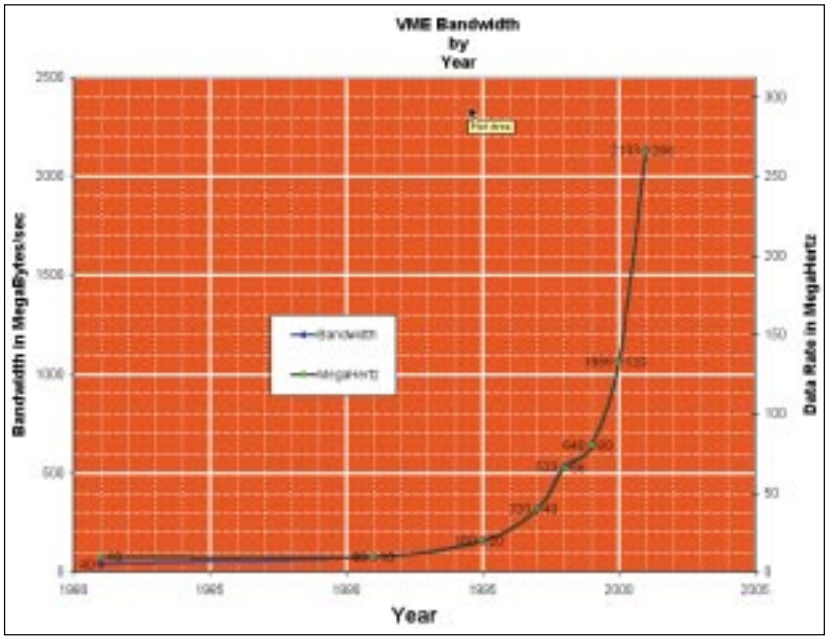

Figure 2

Figure 3: Items needing improvement

Item	Area
1	Signal integrity: Settling time Reflections
2	Crosstalk reduction
3	Power distribution
4	Hot swap
5	Slot count
6	System architecture
7	Interrupt handling
8	Bus arbitration
9	Multiprocessing

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Items 1 and 2 have already been addressed, since they are so important to bandwidth.

DC power distribution

Some very significant unsolved problems remain in the handling of DC power distribution (Item 3) within VMEbus and CompactPCI systems. These problems have been caused by several factors, including:

- the lowering of the DC supply voltages for some onboard components
- the need for many different DC supply voltages within a single plug-in board
- the increase in integrated circuit power dissipation
- the increase in the DC current conducted through the backplane pins
- the requirement for fail-safe power

One solution to all of these problems would be to distribute the DC power in the form of higher DC voltage (such as 24V or 48V DC) and then "step down" this DC voltage locally on each board, using DC-to-DC converters. This greatly reduces the backplane power distribution problems.

One side benefit to this approach is that it lowers DC current drawn through the backplane connector pins, virtually eliminating the ground shift between VMEbus boards, thus improving the signal noise tolerance.

Megabridges — where cost is no object

Hot swap requirements (Item 4), limitations on slot count (item 5), the need for failure isolation in high-reliability systems, and the need to allow each board to transfer data at its maximum clock frequency are causing some to consider another radical step in system architecture — the use of *megabridges* (Item 6) instead of traditional "wired" backplanes.

These megabridges would be active interconnection devices that would be able to automatically connect or disconnect any of the board slots that they serve. Embedded in these megabridges would be versatile interrupt handling (Item 7) and bus arbitration (Item 8) mechanisms that would facilitate multiprocessing (Item 9) and would transfer data at the maximum clock rate that each individual board can handle.

Does this mean wired backplanes will suddenly become obsolete? No. Wired backplanes are extremely cost effective, robust and have a long future ahead. However, the extreme high-end segment of the market (which needs performance at any cost) will be examining the megabridge approach.

Summary

Backplane technology forms the heart of every bus-based architecture. If tomorrow's systems are to satisfy the increasing performance demands placed on them by faster silicon, we will need to see continued progress in the design and fabrication of backplane technology, both through evolutionary and revolutionary innovations. This article has discussed the history of the past innovations in VMEbus backplane design, and has provided a preview of some of the innovations that will be implemented in the near future.

Notes:

[1] See http://www.vita.com/vso/draftstd/2eSSTd1.9.pdf for a copy of the draft standard for 2eSST.

[2] See http://www.ArizonaDigital.com/patents.htm

[3] **GigaBus** is a trademark of Arizona Digital, Inc.

Drew Berding is the founder and president of Arizona Digital and the inventor/designer of the high-speed VMEbus backplane technology that has now become known as VME320. Prior to founding Arizona Digital, Drew founded (and was the vice president of engineering at) Ultra Network Technology, which produces very high speed interfaces to supercomputers such as the Cray XMP48. This involved the design of 200 Mbyte/sec backplanes, I/O channels, and frame buffers. Drew was also the founder and president of Dawn Technology, a turn-key engineering design firm, and one of the first to produce products for the VMEbus specification. In his earlier professional years Drew served on the corporate engineering staff at Memorex, as manager of disk drive development, He also founded (and was the vice president of engineering at) Advance Memory System, which produced the industry's first 1 Kbit DRAM and first 10 nsec bipolar RAM, and later became known as Intersil. He also worked for IBM in several advanced development efforts, one of which eventually became Motorola's MECL III family. Drew has a BSEE from Rensselaer Polytechnic Institute, and a Master in Arts in Counseling Psychology from Santa Clara University. He has been happily married for 38 years, has 3 children and 7 grandchildren.

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