FAIRCHILD SEMICONDUCTOR™

February 2002
Revised April 2002

# Section 1 - Introduction Backplane Designer's Guide

The telecommunications and data-communications infrastructures are growing rapidly to meet consumers' demands for services. This rapid, worldwide growth has created an escalating need for increased system performance. In this context, backplanes have become a focal point, and backplane designers are faced with many pressures: the requirements of high performance, upgraded applications, the increased need for throughput, and rapid time to market. Ultimately, the designer's goal is to deliver a backplane with the performance required by the system.

## Application Demands

The need for increased throughput is critical as applications are upgraded for high-performance data communication and telecommunication systems and for servers that transmit enormous amounts of information at extremely high rates. Much of this demand comes from an increase in peer-to-peer communication with cell phones and the Internet.

## Basic Backplane Considerations

Throughput and reliability are two measures of backplane performance. These two benchmarks ultimately derive from backplane signal integrity. Backplane signal integrity and throughput are frequently referenced in this guide because of the critical role they play in system speed and system reliability.

## Signal Integrity

Signal integrity refers to the degree to which a signal is free of distortion. The quality of a signal in a backplane will ultimately define the rate at which data passes through the backplane. The designer's objective is to obtain the highest possible degree of signal integrity within the defined backplane design constraints. For this reason, designers must recognize and address the factors that affect signal integrity.

In many backplanes, signals will be transmitted through the system at extremely high frequencies. At these frequencies, it is important that the signal be free from noise because noise affects the ability of receivers to interpret signals from the drivers. If there is a significant amount of noise associated with the signal, then the receiver will not be able to interpret it accurately. If this happens, the frequency of the backplane may have to be decreased so the receiver can correctly decipher the signal.

Backplane design sometimes requires system design compromises. For example, good signal integrity may be achieved by maximizing some performance parameters while sacrificing some others. This type of customization is a typical practice in the art of backplane design.

Other parameters that affect backplane signal integrity include the impedance characteristics of the load, propagation delays, transmission setups, stub lengths, and connectors. This Backplane Designer's Guide addresses these issues as well as other topics that affect signal integrity and throughput. It can also serve as a tool to aid in designing backplanes with high levels of signal integrity.

## Demand for Higher Throughput

Throughput can be defined as the rate at which data is transmitted through the backplane. In an asynchronous type of application, throughput can be defined as twice the data switching frequency multiplied by the number of parallel data bits being transmitted across the backplane. In a synchronous switching application, throughput can be defined as the clock switching frequency multiplied by the number of parallel data bits being transmitted across the backplane, assuming the clock is twice this data rate.

A direct relationship can be made between throughput and backplane speed. The performance of a backplane can be measured by the maximum throughput processed. This guide emphasizes the importance of increasing throughput in a backplane design.

The technology chosen to drive the backplane is one of the major factors affecting the backplane's maximum throughput. The market offers a broad spectrum of technologies that have the ability to achieve different rates of throughput, and it is up to the designer to decide which technology offers the greatest throughput in a specific backplane environment.

## How to Use this Guide

This Backplane Designer's Guide presents information to aid in the design of high-performance backplanes. Written with the design engineer in mind, it presents information that will help make the decision process smoother and faster as the engineer is faced with the constant demands of increased performance and short time to market. Because each section can stand on its own, this guide may be used as a reference.

 

## Section Reference

The following table provides a summary of information contained in the Backplane Designer's Guide. It will be repeated in each section with the section under discussion highlighted.

| Section | Section Title | Contents |
|---|---|---|
| **1** | **Introduction** | **Application demands, basic backplane considerations, and how to use this guide.** |
| 2 | Backplane Protocols | Descriptions of different backplane bus protocols, including PCI- and VME-based protocols. |
| 3 | Backplane Architecture | Topics relevant to backplane configuration, including parallel versus serial configuration and different configuration topologies and timing architectures |
| 4 | Backplane Design Considerations | Issues relevant to backplane layout, including distributed capacitance, transmission line effect, stub length, termination, and throughput. |
| 5 | Backplane Signal Driving and Conditioning | Signal driving and conditioning, including power consumption, rise/fall time, propagation delay, flight time, device drive, pin conditioning, live insertion, and incident wave switching. |
| 6 | Noise, Cross-talk, Jitter, Skew and EMI | A review of the enemies of signal integrity and high frequency. |
| 7 | Transceiver Technologies | Detailed information about the following technologies: TTL-based (ABT, FCT, and LVT); ECL; and GTLP. |
| 8 | Mechanical Considerations | Information about mechanical considerations such as backplane chassis/cages and connectors. |
| 9 | Layout Considerations | Physical layout of the receiver and driver cards plugged into the backplane, primarily focusing on construction of the physical layer and the configuration of the devices that comprise the cards. |

## Design Guide Bibliography

MUCH OF THE INFORMATION IN THIS DESIGN GUIDE IS A RESULT OF EXPERIMENTATION AND TESTS IN THE APPLICATION LABORATORY AT FAIRCHILD SEMICONDUCTOR. AS WELL AS THE FIRST HAND KNOWLEDGE OF MANY OF THE ENGINEERS OF FAIRCHILD SEMICONDUCTOR CORP. OTHER INVALUABLE RESOURCES ARE INCLUDED BELOW.


- JOHNSON H. AND GRAHAM M., HIGH SPEED DIGITAL DESIGN (A HANDBOOK OF BLACK MAGIC) PRENTICE HALL INC. 1993
- HALL S. HALL G. AND MCCALL J., HIGH-SPEED DIGITAL SYSTEM DESIGN (A HANDBOOK OF INTERCONNECT THEORY) JOHN WILEY & SONS INC. 2000
- LAVERGHETTA T., MICROWAVE MATERIALS AND FABRICATION TECHNIQUES ARTECH HOUSE INC. 2000
- MASSOBRIO G. AND ANTOGNETTI P., SEMICONDUCTOR MODELING WITH SPICE MCGRAW-HILL 1993
- BREWER R., CABLE, CONNECTORS AND ELECTROMAGNETIC COMPATIBILITY CONNECTOR SPECIFIER OCTOBER 2001