FAIRCHILD SEMICONDUCTOR™

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Section 4 - Backplane Design Considerations Backplane Designer's Guide

This section focuses on designing high-performance parallel backplanes, a task that can be extremely complex. To assure high performance and good signal integrity, many issues must be considered during the design process. To a large extent, system requirements will define backplane design, determining if distributed capacitance effects will be present on the backplane. Due to the frequencies of high-performance backplanes, transmission line behavior is common in most applications. For backplane design, the minimum system requirements are backplane frequency, the number of loads, and, assuming a multidrop/multipoint configuration, the number of outputs switching.

Section Reference

This section presents information covering:

- Backplane layout and design parameters
- Distributed capacitance
- Transmission line effects
- Impedance
- I/O device capacitance
- Stub effects
- Termination
- Throughput

Section	Section Title	Contents
1	Introduction	Application demands, basic backplane considerations, and how to use this guide.
2	Backplane Protocols	Descriptions of different backplane bus protocols, including PCI- and VME-based protocols.
3	Backplane Architecture	Topics relevant to backplane configuration, including parallel versus serial configuration and different configuration topologies and timing architectures
4	**Backplane Design Considerations**	**Issues relevant to backplane layout, including distributed capacitance, transmission line effect, stub length, termination, and throughput.**
5	Backplane Signal Driving and Conditioning	Signal driving and conditioning, including power consumption, rise/fall time, propagation delay, flight time, device drive, pin conditioning, live insertion, and incident wave switching.
6	Noise, Cross-talk, Jitter, Skew and EMI	A review of the enemies of signal integrity and high frequency.
7	Transceiver Technologies	Detailed information about the following technologies: TTL-based (ABT, FCT, and LVT); ECL; and GTLP.
8	Mechanical Considerations	Information about mechanical considerations such as backplane chassis/cages and connectors.
9	Layout Considerations	Physical layout of the receiver and driver cards plugged into the backplane, primarily focusing on construction of the physical layer and the configuration of the devices that comprise the cards.

Backplane Distributed Capacitance

Distributed capacitance is an important issue when designing high-speed backplanes. As driver frequencies increase, the system capacitance design must be carefully considered. The backplane medium itself has a capacitance and each connector and each card plugged into the backplane also has some level of capacitance. The total backplane capacitance has a direct effect on maximum system speed. The higher the capacitance, the longer the signal flight time, because the capacitance of all components of the backplane must be charged as the signal propagates down the backplane to threshold levels. Due to this phenomenon, careful attention to minimizing capacitance in a design can achieve significant performance gains.

Backplanes can be classified as low-, medium-, or high-performance systems. A low-performance backplane can be modeled as a lumped load. Medium- and high- performance backplanes can contain transmission line characteristics and should be modeled as distributed loads.

In a low-performance backplane, the backplane driver senses the load as a lumped capacitance. In some cases, the capacitance is actually a distributed load but is still modeled as a lumped load. This model is used when the rise time of the signal is slow compared to the flight time down the backplane.

In higher-performance, parallel backplane designs, fast edge rates and multidrop architecture cause the capacitance load to be distributed over the length of the backplane. This model is used when the rise time of the signal is fast compared to the flight time along the backplane.

Transmission Line Characteristics

Due to fast edge rates, most medium-performance and all high-performance backplanes will be made up of transmission lines. A transmission line consists of a conductor interconnecting two or more circuits. This conductor has a distributed series inductance and distributed capacitance. This is why the backplane must be calculated as a distributed load.

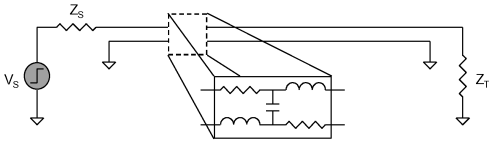


FIGURE 1. Graphical representation of a transmission line showing source voltage and source termination impedance, line termination impedance, the resistive and inductive line components, and the capacitive relationship to the power planes

Figure 1 shows the transmission line as a distributed resistive, inductive and capacitive load. The backplane driver charges the capacitive load and the signal is delayed by the inductance along the line.

A transmission line has a characteristic impedance (Z_O) for any length in which the distributed parameters are constant. The Z_O is the ratio of transient voltage (or instantaneous changing voltage) to transient current (or instantaneous changing current) passing a point in the line when a signal change or other electrical disturbance occurs.

The driver output signal sees the line as impedance, given by the equation:

$$Z_O = \sqrt{L_O/C_O} = \frac{V}{I}$$

Where:

Z_O = Characteristic Impedance

L_O = Distributed Inductance per Unit Length

C_O = Distributed Capacitance per Unit Length

Lines that have a propagation delay time greater than one-third of the output edge rise time of the driver should be evaluated for transmission line characteristics. When transmission line analysis is performed on a backplane, only the longest and most heavily loaded line and the shortest most lightly loaded line need be analyzed. If any line shows transmission line characteristics, all lines need to be terminated equally as transmission lines to ensure similar signal behavior on all the lines

Distributed Capacitance Effects

For a designer, two of the most significant transmission line parameters are $Z_{O\ (EFF)}$, or Z'_O, also known as the effective impedance, and $t_{PD(EFF)}$. or t'_{PD}, also known as the effective propagation delay down the line. For both of these parameters, the intrinsic values are geometrically dependent upon the trace and connector layout. All receiver inputs as well as their connectors and stubs have capacitive load characteristics. Adding stubs, connectors, and loads will significantly alter a transmission line's effective impedance (Z'_O). These features will alter signal propagation on the transmission line.

As an example, assuming an ideal transmission line with a distributed inductance of 44.9 nH and a distributed capacitance of 17.9 pF, impedance can be calculated with the equation:

$$Z_O = \sqrt{\frac{L}{C}} \quad t_{PD} = \sqrt{LC}$$

Where:

L = Distributed Inductance

C = Distributed Capacitance

In this example, transmission line impedance equals 50Ω, and propagation delay equals 896 ps. When the intrinsic values are known, the effects of the total receiver loading (also called gate loading) can be calculated and compared.

Figure 4-2. shows a layout of a distributed capacitance schematic of a multipoint connection, with capacitor values of 12 pF. This 12 pF value represents the additional capacitive loading of 10 stub-connector-card combinations.

Backplane Distributed Capacitance (Continued)

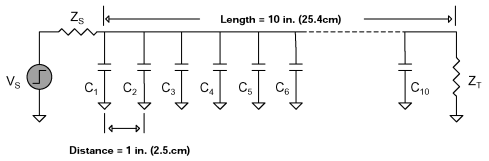


FIGURE 2. Equivalent multipoint application

This figure assumes that the spacing between card slots is within the rise/fall time of the driver signal and that all slots are occupied with cards. The capacitance can then be distributed uniformly at an even rate of capacitance per inch. When all the slots are filled, the 10-inch transmission line has a 12 pF capacitance distributed at 1-inch intervals. The distributed capacitance (C) affects both the propagation delay and the characteristic impedance of the strip-line. The result is a new effective impedance, Z'_O, and a new effective propagation delay, t'_{PD}, as shown by the following equations:

$$Z'_O = \sqrt{\frac{L}{C + NC_L/X}} \qquad t'_{PD} = \sqrt{L\left(C + \frac{NC_L}{X}\right)}$$

Where:

L = Distributed Inductance

C = Distributed Capacitance

C_L = Total Load Capacitance

N = Number of Loads

X = Line Length Over which the Loads are Distributed

Z'_O = 39Ω

t'_{PD} = 1.145 ns

Note that the formulas show that the capacitive line load (C) decreases the effective impedance of the line and increases the propagation delay.

Distributed Loading and Signal Performance

As noted in Figure 3, the loads on a transmission line that includes distributed loads will have an effect on waveform shape and the effective impedance of the line. These loads will slow the signal propagation on the line and also cause reflections.

All capacitive loads on a transmission line that are not terminated at their source will cause signal reflections. Reflections from two adjacent loads tend to overlap if the time required for the incident wave to travel from one input to the next is equal to, or less than, the signal rising or falling edge time. As the edge rate increases, these individual reflections will combine.

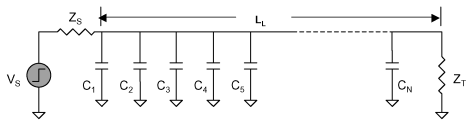


FIGURE 3. Distributed Loading on a Transmission Line

The combined reflections change the shape of the input waveform, and the signal will begin to appear as if the termination resistance value is larger than the line impedance value. By lowering the transmission line's effective impedance (Z'_O), these loads oftentimes cause a mismatch between the line and the termination. Hence, the line termination values must take into account the line loading and be matched to the line effective impedance. Proper termination will minimize any transmission line reflections.

Backplane Stub, Connector and Device Capacitance

From the standpoint of both signal integrity and system timing, the capacitive loading effects of all components connected to the transmission line and used in a backplane system must be accounted for. To minimize the distributed capacitance on the backplane lines, select connectors with low capacitance and low inductance. It is advisable to use devices with low I/O capacitance, and keep the stub lengths to a minimum.

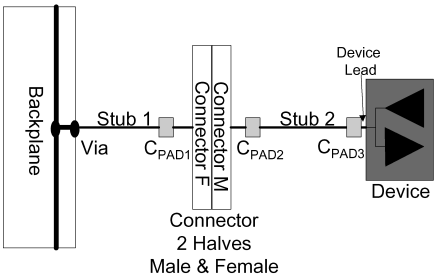


FIGURE 4. Typical Connection Scheme of a Backplane

Figure 4 shows an example of a typical worst-case connection scheme between the backplane strip line and the driving and receiving devices on the daughter cards of a backplane. As shown in the illustration, this can include a via from a backplane buried trace stub. This can involve a via to the connector pad, two connector halves, daughter board connector pad, stub, device pad, and device lead and device. Each item contributes some capacitance and a potential discontinuity.

The total capacitance in this setup can be calculated as:

$$C_T = C_{VIA} + C_{STUB1} + C_{PAD1} + C_{CONF} + C_{CONM} + C_{PAD2} + C_{STUB2} + C_{PAD3} + C_{IO}$$

Where:

C_T = Capacitance Total

C_{VIA} = Via Capacitance

C_{STUBn} = Stub Capacitance

C_{PADn} = Pad Capacitance

C_{CONn} = Connector Capacitance

C_{IO} = Device I/O Capacitance

Device I/O Capacitance

The I/O capacitance of transceivers, drivers and receivers can compromise backplane loading. Selection of transceivers or drivers and receivers with low I/O capacitance will have a significant positive impact on the overall design. This selection will give the design a reduced bus loading, lower propagation delays, and reduced capacitive glitch

Backplane Distributed Capacitance (Continued)

effects. The I/O capacitance of a device is usually listed in the manufacturer's databook, and this information should be used in calculating the design's overall system capacitance.

Device Decoupling

High-performance and high-drive logic families such as those used in backplane designs have special decoupling requirements. High-drive devices require more current during transitioning (switching) than do most standard logic devices. Local high frequency decoupling is required to assure clean power to the driver when the it is switching.

These local decoupling capacitors ensure adequate power by filtering out voltage drops on the local V_{CC} line. They charge during normal and high voltage cycles on the V_{CC} line and give up this charge during low voltage transitions on the V_{CC} line. It can be theorized that these capacitors act as small batteries that keep the driver from experiencing current starvation during switching.

In most applications, at least two sizes of decoupling capacitors are needed to cover the various harmonic frequencies seen on a V_{CC} line. The recommended topology is to place the capacitors as close to the V_{CC} pin as possible. It is also advised that connections to the ground plane be positioned closely. This positioning reduces V_{CC} starvation effects by minimizing path inductance and by shorting frequency flight time of the V_{CC} pulses. For the same reasons, when multiple sizes are used, place the smallest (highest frequency) decoupling capacitor closest to the V_{CC}, and step the other capacitors away from V_{CC} in ascending order.

The following equation can be used to calculate the capacitance for decoupling:

$$C = (I * t)/V_{DD}$$

Where:

I = Current

t = Edge Rate

V_{DD} = Voltage on the Bus

Connector Impedance

Card connectors also have an effect on backplane loading, and connector design has an effect upon capacitance and inductance, and, therefore on the backplane impedance seen by the driver. For high-performance backplanes, selection of connectors with low inductance, capacitance, and controlled impedance will have a direct, positive impact on system performance.

Stub Impedance

Stubs are the traces between the card to backplane I/O devices and the connectors, and the connectors and the backplane. Stubs have inductance and capacitance; they change the overall impedance of the transmission line; and they affect the signals that operate on the backplane. These characteristics coupled with capacitance change the impedance and delay constants of the transmission line. Stub length is measured from the backplane through the connector pin, stub, and the series termination resistor to the device pin.

If a stub is long enough (length > t_{RISE} / 3), transmission line effects take place causing potential signal integrity problems. Because of this phenomenon, it is advisable to keep stub lengths to a minimum. Short stub lengths result in reduced propagation delay, less change in rise and fall times, and minimum change in termination resistance. In theory, a design goal for stub length is less than 0.33 * t_{RISE}, but the stub length will depend on overall design needs and constraints.

Stub Effects

In backplane design, stub layout has an impact on the driver stub and in the receiving stubs, that is, on all other stubs on the backplane. The effects in the driver stub fall in two distinct categories, flight time and rise time. The longer the stub, the longer it takes a signal to propagate down it. This delay, called stub delay, causes increased flight time from the driver to the backplane line. The inductance of the stub and the connector form a system that acts like an RCL circuit between the driver and the load. Figure 5 illustrates a Thevenin equivalent.

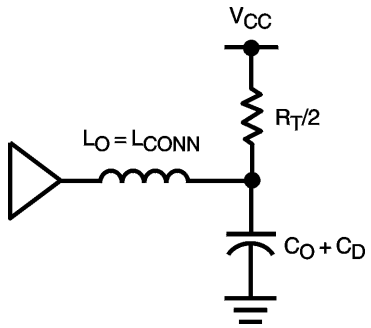


FIGURE 5. Thevenin Equivalent of Load. $R_T/2$ represents termination at both ends of the backplane.

The receiver stubs, connectors, and device inputs are seen as a capacitive load to the driver. Each stub in a multidrop application adds a capacitive load along the backplane transmission line that the driver must charge or discharge during switching. The impact is an increase in the edge rate during transitions. These are seen on the signal as small voltage droops (a voltage droop is defined as a momentary reduction of the voltage level) on the rising edge or peaks on the falling edge. Each of these droops or peaks corresponds in time with the stubs along the backplane. The results are a slowing of the edge and an increase in switching time.

Stub Length Termination Effects

Stub length must be considered as part of the calculations for stub termination resistance values. As the length of a stub increases, its capacitance increases, lowering the effective impedance of the line. This lowering of effective impedance requires a lower termination value to match the lower effective impedance.

To assure proper termination of the backplane, it is necessary to account for the increased capacitance of the stub and to adjust the termination resistance appropriately.

Termination

Termination is the method by which a signal propagating through the backplane is discontinued. Ideally, the termination method chosen should increase performance and promote good signal integrity. From a signal integrity perspective, an ideal termination will match the backplane impedance. This optimal termination results in a single monotonic (nonstepped) signal with no reflections. As with other aspects of backplane design, termination options offer performance trade-offs.

No termination or severely under-matched termination on a transmission line will result in a non-monotonic or stepped waveform that is the product of reflection from the backplane end. This situation results in a full round-trip flight delay from driver to backplane end and back before all receivers reach voltage threshold level. Some backplane designs, such as PCI, depend on this feature to function. However, high-speed backplanes with fast edge rates will experience unacceptable delays as well as uncontrolled reflections, ringing, and unacceptable voltage excursions above V_{CC} and below ground. These effects can degrade the system's speed and increase the amount of noise in a backplane.

A properly designed termination scheme will promote signal integrity on the backplane. By properly matching the termination to the backplane impedance, the signals traveling the backplane see only a continuous line when reaching the termination. All the signal energy is absorbed by the termination. The outcome is a clean transition on the backplane line, with no reflections or voltage spikes. High-speed backplane termination is considered so critical that backplane driver technologies such as Gunning Transceiver Logic Plus (GTLP) are designed to work specifically with this termination scheme.

Reflection Behavior

With a termination that matches the Z_O of the line, the ratio of voltage to current traveling the line is matched by the ratio of voltage to current at Z_T (termination impedance). If Z_T is not equal to Z_O, the initial voltage change and current flow on the line is still determined by the source and the line impedance. However, this initial voltage-to-current ratio is not equal to the ratio demanded by Z_T. Because of this, a second voltage and current wave is generated to satisfy Ohm's law at the transmission line to termination interface.

Depending on the value of the termination in relation to the transmission line, this energy wave will be reflected back toward the driver or absorbed by the termination. This relationship is illustrated in Figure 6.

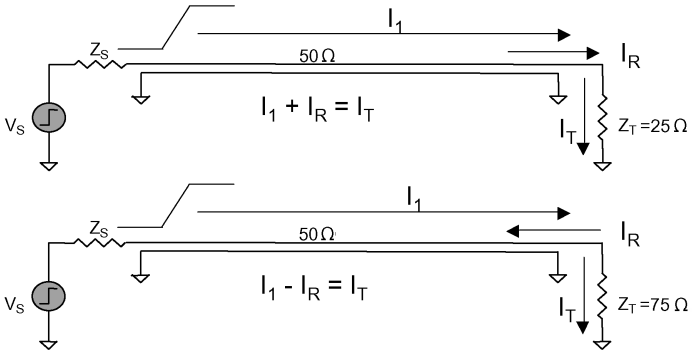


FIGURE 6. The relationship between transmission line and termination values will define signal reflection polarity.

Application of Kirchoff's laws to the line end at the instant of the initial wave arrival results in the following:

- When termination value is less than the transmission line value:

  $I_1 + I_R = I_T$ = current into R_T

- When termination value is greater than the transmission line value:

  $I_1 - I_R = I_T$ = current into R_T

  Where:

  I_1 = Initial current wave propagating down the line

  I_R = Reflected current into the termination

  I_T = Total current into the termination

When this reflected wave arrives at the driver, the same phenomenon occurs if the driver impedance is not a match for the line impedance. With each successive reflection, the line comes closer to the final steady state voltage level. The ratio of the impedance mismatch determines the amplitude and behavior of the reflected wave. The reflection coefficient formula is used to calculate the ratio and for both the termination and the driver.

$$\text{Reflection coefficient at termination} = \frac{Z_T - Z_O}{Z_T + Z_O}$$

The polarity of the initial reflected voltage (V_R) is dependent upon the ratio of the termination to line impedance.

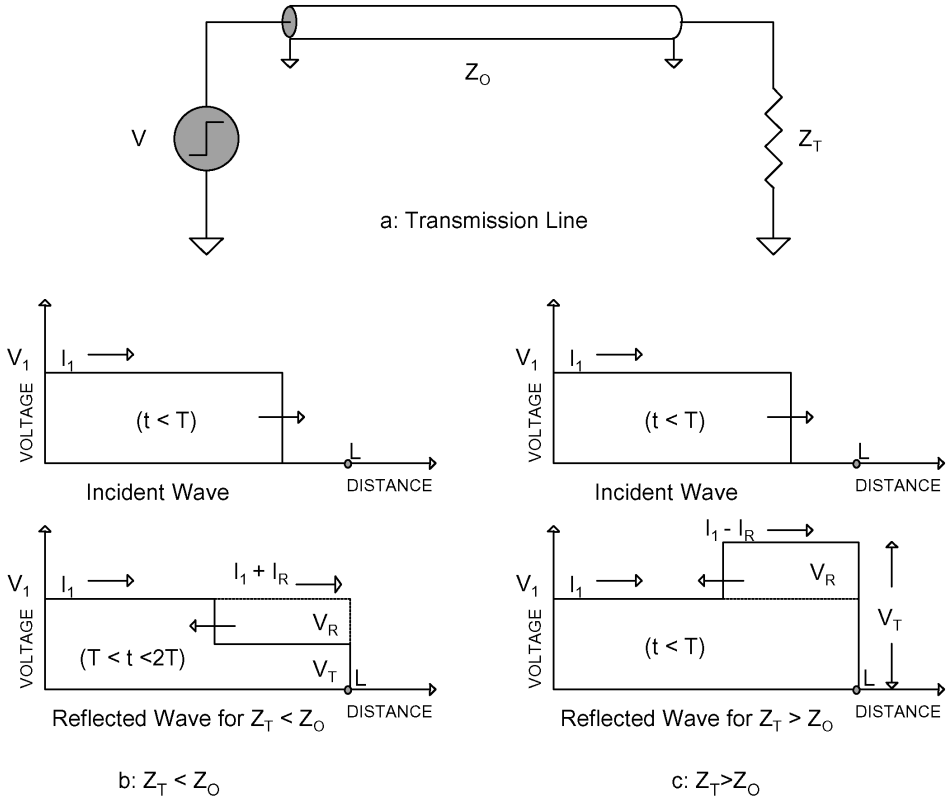
Termination and Reflection

The ideal line-to-termination ratio is 1 to 1. This ratio means that for a transmission line with a Z'_O of 50Ω, a termination design that gives a Z_T of 50Ω at the required frequencies is ideal. Such a 1 to 1 match will result in no reflection. However, many I/O technologies are not

Termination (Continued)

designed to drive very low impedance terminations such as a 50Ω DC termination at the end of a 50Ω line. This design requires design with higher termination values (moving the coefficient value closer to +1) or transmission line and termination schemes that help negate this effect and still retain a low reflection coefficient, such as AC termination.

An impedance mismatch will cause reflective energy waves. The behavior and duration of these waves depends on whether the mismatch is higher or lower than line impedance, and whether the mismatch is of a great magnitude.



L = Length of Transmission Line
T = Delay of Transmission line
t = Time of Sample
I_1 = Incident Wave Current
V_1 = Incident Wave Voltage
I_R = Reflected Wave Current
V_R = Reflected Wave Voltage
Z_O = Characteristic Impedance of Line
Z_T = Termination Impedance
V_T = Voltage at Termination

FIGURE 7. Transmission Line and Reflected Waves for Line Termination values higher than Line Impedance and lower than Line Impedance

When to Use Termination

Although termination is not mandatory, it is recommended that a termination scheme be implemented, and there are situations in which termination schemes should always be used. For example:

- When line lengths meet a transmission line criteria, as calculated by $t_D > t_R/3$
  (t_D is the delay time, and t_R is the rise time)
- Noise critical signal lines
- If a device is designed to operate specifically with termination. For example, GTLP devices must be terminated.

Termination Recommendations

There are several termination options - no termination, series termination, parallel termination, Thevenin termination, AC termination, and clamp diode termination. The term technique used depends on system power requirements, signal line layout, and the I/O technology used in the backplane.

No Termination

No termination is the simplest approach and works well in a point-to-point environment as long as precautions are taken.

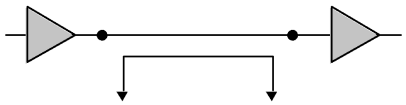


FIGURE 8. I/O with No Termination

In a multiple-receiver environment, any receivers between the driver and the line end will receive the signal in a two-step waveform. The first step will be the incident wave (V_I). The second step will be the return from the receiver to the driver. Incident amplitude depends on driver output impedance and line impedance. The incident amplitude level will determine whether the line receivers will switch on the incident wave or the return wave.

For non-terminated lines, the length should not exceed the round-trip delay time for one- half the driver output edge rate. If the driver technology has unbalanced output drive, the fastest edge time should be used to calculate the allowable line length. For example, if output fall time (t_F) is 3 ns, the total signal round-trip time should be 1.5 ns or less. At these round-trip times, the line will not behave as a true transmission line, and the impact of reflections and ringing will be minimized. The propagation time per inch or millimeter of the line must be known, and is directly related to line geometry. The maximum allowable line length can be determined by the formula:

$$L_{MAX} = 0.5t_R / 2t_{PD}$$

Where:

L_{MAX} = Maximum Acceptable Driving Length

t_R = Rising or Falling Output Edge Rate

t_{PD} = Propagation Delay Units (Time per Length)

Low drive technologies may permit round-trip times of up to one time the rising or falling edge. This characteristic is due to slower edge rates and lower drives that produce slower current changes on the line and minimize ringing. Older Also, lower drive technologies with higher V_{CC} allow a higher degree of signal noise margin.

If line length exceeds the round-trip delay time of one-third the rising or falling edges of the driver, the line will exhibit transmission line characteristics. Multiple reflections are likely to occur in this scheme because both the receiver and driver are likely to be mismatched to the line impedance.

In most I/O technologies, receiver input impedance is much higher than line Z_O, even though the 'ON' impedance of a driver is much lower than line Z_O. These impedance mismatches result in a reflection coefficient at the receiver of close to +1 and a reflection coefficient at the driver of close to –1. These opposite reflection coefficients cause the signal level change to be reflected back and forth with a polarity change each time it is reflected from the driver. Thus, after a signal switch, multiple reflections on the line will occur, each will be a reflection of an opposite polarity and each will decrease in magnitude until line voltage settles to the quiescent level.

An additional concern for unterminated lines is voltage undershoot and overshoot, often referred to as ground bounce or V_{CC} bounce. Although bounce is a concern on any signal line, short unterminated lines have properties that can generate significant ground bounce or V_{CC} bounce due to a short unterminated line that is capacitive to the driver. Hence, the shorter the line, the more this line will behave as a capacitor connected directly to the driver. A capacitive load generates more instantaneous current than a resistive load. This larger current generates more over- and undershoot. A receiver that is designed to tolerate these voltage excursions is necessary in this environment. However, signal evaluation should also be done to ensure that the over- and undershoot excursions do not cross the switch threshold of the device.

Using a short nonterminated line for driving multiple outputs will increase this capacitive effect. Every additional output will add its capacitive input value to the lump load effect felt by the driver.

Series Termination

Placing a resistor in series with the output works well for point-to-point applications, or in situations where the loads are grouped at the far end.

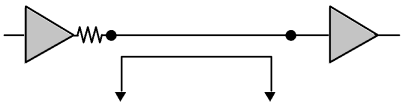


FIGURE 9. Series Termination Design

By matching the driver output impedance to the line impedance, reflections returning from the receiver are dampened out. The resistor in the series configuration should be set to: Resistor = $Z_O - Z_{OUT}$.

As with a no-termination design, loads between the driver and the line end will receive the signal in a two-step waveform. The first step will be the incident wave (V_I).

When to Use Termination (Continued)

Amplitude is dependent upon driver output impedance, series resistor value, and line impedance. The formula to calculate this is:

$$V_I = V_{DD} * Z'_O/(Z'_O+R_S+Z_S)$$

Where:

V_{DD} = Power Supply Voltage

Z'_O = Effective Line Impedance

R_S = Series Resistor Value

Z_S = Driver Output Impedance

V_I will be one-half the voltage swing if the series resistor value plus the driver output impedance equals the line impedance. If this is the case, all inputs not at the end of the line will receive a valid input only after the wave has propagated to the end of the line and back past that input towards the driver. Therefore, all inputs on the line will switch within two times the line delay.

This design uses no additional system power, and is among the simplest termination schemes to implement. Some I/O technologies are offered optionally with the series resistor designed into the output structure. The value of this resistor is usually in the 25Ω range, coupled with the intrinsic output resistance, this gives a driver on impedance in the 50Ω range. This design also offers a slower driver output edge that is caused by the series resistor and that reduces ground bounce in comparison to equivalent non-series resistor devices.

Parallel Termination

Parallel termination, which is also called DC parallel termination, effective at reducing or eliminating reflections from the termination end of a transmission line. The design is implemented by connecting a resistor between the termination end of the transmission line and ground or V_{CC} as in Figure 10. Termination to V_{CC} is more properly referred to as Thevenin termination, but because it is often referred to as DC parallel termination it is included in this discussion.

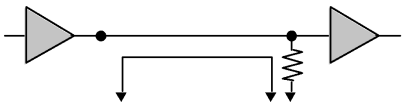


FIGURE 10. DC Parallel Termination Design

Selecting a resistor with the same value as line impedance eliminates reflections. The signal senses no mismatch between transmission line end and termination. AC and DC currents are returned to the V_{CC} or ground plane. Because of this current path, DC power consumption is increased significantly over many other termination designs. In the DC parallel termination design, DC power consumption is directly related to the duty cycle; therefore, signals with a lower duty cycle use less power.

The load as sensed by the driver is resistive, not capacitive. Therefore, the capacitive portion of the load does not affect power consumption. Because of this feature, parallel termination dissipates less AC power. At higher frequencies, parallel termination may consume less power than other termination designs, such as the no termination design. Depending upon the load capacitance, duty cycle, and line impedance, this power consumption crossover point may be as low as 40 MHz.

There are disadvantages to DC parallel termination. The impedance of most transmission lines is 50Ω or 75Ω. Matching parallel termination for this design requires high drive capability and consumes significant static power.

For some I/O technologies, an additional drawback to parallel termination is the unbalanced output this design creates. Tying the termination to the ground causes the Voltage Out High (V_{OH}) to be degraded due to the high drive required to overcome the DC load. Conversely, tying the termination to V_{CC} will degrade the V_{OL} level. These levels will still be above minimum voltage input high (V_{IH}) and below V_{IL} for low voltage CMOS, provided maximum current specifications are observed. However, some I_{CC} current will be added at the receiver inputs due to this level degradation.

Thevenin Termination

A Thevenin termination design is ideally suited for backplanes and environments where long line lengths and heavy loads exist. By holding the line quiescent, that is, by holding the voltage level at or near the center switch point, less drive is needed to switch the bus. This quiescence enables drivers to switch lines that have very low impedance levels and heavy loads. However, this design has very high DC power consumption. The usual implementation of this termination design is a voltage divider, with a resistor that is tied from the receiver end of the line to the power supply, and a resistor that is tied to ground as in Figure 11.

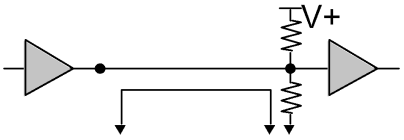


FIGURE 11. Thevenin Termination Design

The resistors in the Thevenin termination should be set to twice the amount of Z_0. However, various resistor value combinations may be selected depending upon system design needs. By selecting pull-up and pull-down resistors of the same value, CMOS outputs will not be unbalanced, although the output swing is reduced for both V_{OH} and V_{OL}. Lines with these values cannot be allowed to float or high power dissipation through I_{CC} and receiver oscillations will result. If the bus will be left floating, a termination resistor ratio that moves the quiescent voltage level to a V_{IH} or V_{IL} level should be selected and this will allow the bus to be left in an undriven state, without I_{CC} and oscillation problems. The trade-off for this selection choice is unbalanced termination and driver outputs.

AC Parallel Termination

This design, commonly called AC Termination, is similar in layout to DC parallel termination. A capacitor is added to

When to Use Termination (Continued)

the termination in series with the termination resistor as in Figure 12. The capacitor blocks DC current flow through the termination. The capacitor negates DC power consumption while maintaining the AC current path.

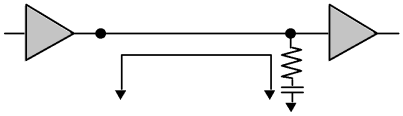


FIGURE 12. AC Parallel Termination Design

The resistor should be the same a Z_0 and the capacitor set to the following.

Capacitor = $C > (3 * t_{RISE}) / Z_0$

Where:

Z_O = Characteristic Impedance

t_{RISE} = Rise Time

The benefit of this design is elimination of termination reflections. This allows for greatly reduced power requirements compared to DC parallel or Thevenin termination designs. After the initial voltage step, the capacitor is charged to the rail supply voltage at a rate determined by the RC time constant of the circuit. The capacitor value needs to be carefully determined. If the RC time constant is too small, the termination will act as an edge generator that creates both over- and undershoot. Increasing capacitor value reduces overshoot, but also increases power consumption. As a rule, the RC time constant should be greater than three times the line delay.

At lower frequencies, the termination capacitance increases the total signal trace impedance. Therefore, the termination capacitance also increases the power consumption in this low frequency range. At higher frequencies, the capacitor is unable to charge or discharge fully. The power curve rolls off in this frequency range. At very high frequencies, this termination behaves like a parallel resistor tied to an intermediate power supply. The voltage level of this power supply is determined by the duty cycle of the signal.

The power consumption slope is dependent upon the power dissipation capacitance (C_{PD}) of the driver technology. The power consumption curve crossover point between AC parallel termination and no termination is dependent upon signal duty cycle and capacitive line loading and may be as low as 15 MHz.

AC Parallel Termination is an excellent choice for CMOS I/O technologies, and works well with distributed load backplanes. Due to the termination to line impedance match, reflections are eliminated and incident wave switching is achieved for all receivers on the line. Power consumption is significantly lower than DC parallel and Thevenin terminations and at higher frequencies, less than no termination.

Diode Termination

Diode termination design consists of one diode between the receiver and ground and often an additional diode connected to V_{CC} as in Figure 13. Schottky diodes are normally used for this design because of their low turn-on voltage level (0.5 V). Unlike other termination designs, diode termination does not attempt to terminate a line into a matched impedance value.

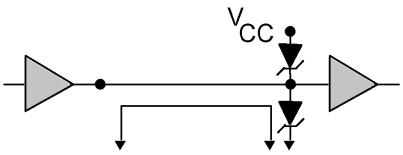


FIGURE 13. Clamp Diode Termination Design

This clamp diode termination design functions by shunting voltage under- and overshoot excursions onto the ground and V_{CC} rails. Since the diodes are normally reverse-biased, the design consumes virtually no DC power and minimal AC power. A fast turn-on time (t_{ON}) diode is required for this termination design to work correctly. The higher the frequencies and edge rates used in the system, the more critical this criterion of fast turn on time becomes.

Diode termination is ideal for a line where multiple devices will both drive and receive. Because of its ability to shunt voltage excursions off of signal lines and its minimum power increase, this clamp diode termination design is often used in conjunction with other termination designs to eliminate voltage undershoot and overshoot.

Throughput

Throughput becomes more important as designers strive to create faster backplanes capable of passing large amounts of data at increasingly higher speeds. Throughput can be defined in the following ways:

- For an asynchronous application, throughput is data switching frequency times the number of parallel data bits being transmitted across the backplane. For example, Fairchild Semiconductor's GTLP16T1655 has a maximum throughput of 1.6 Gbits/s operating at 100 MHz. This is because at a 100 MHz input signal the GTLP device can process information at the rate of 1.6 Gbits/s due to its 16 bits.
- For a synchronous application, throughput is defined as clock switching frequency times the number of parallel data bits that are sent through the backplane.

Factors that affect the throughput of the backplane include throughput of the I/O devices, overall capacitance of the backplane, number of loads, stub lengths, and impedance.

A designer should consider carefully the total capacitive load that the drivers will sense. This load will be a result of distributed capacitance of the backplane itself and all the loads. These loads include the receivers, connectors, and stubs. The total distributed capacitive load value is inversely proportional to propagation time down the backplane. The more loads and the higher their value, the slower the propagation time, which results in a lower maximum frequency.

Termination design has a significant effect on throughput. A termination that is matched to the backplane impedance will have little or no signal reflection. An unmatched termination design can have a significant number of reflections back and forth over the length of the backplane. These reflections will require settling time before the next signal can be sent. This limits maximum frequency.

Incident wave switching is a key factor in determining throughput. If the backplane drivers are capable of producing incident wave switching for all receivers, then the overall throughput of the backplane will be much higher than that of reflected wave switching.

The ability of the signal drivers to create incident wave switching will depend on the dynamic output drive of the devices, the number of loads, the backplane impedance, and the termination used. If a backplane has a large number of loads, the device may have a difficult time producing incident wave switching, and it will have to rely on a reflection to achieve a valid change of state on the receivers. Reflected wave switching could take up to twice the time of incident wave switching depending upon the location of the receivers on the backplane. System throughput will be significantly decreased if the receivers have to wait for a reflected wave front from the driver.

There are many elements in a backplane that play a role in throughput. It is critical for the designer to recognize and address every factor, issue, and parameter of the backplane to ensure optimal performance.

Summary

Although system requirements define minimum backplane performance, understanding critical parameters and careful design practices have a direct impact on maximum performance. It is an easy task for designers to fulfill standard system requirements to define minimum backplane performance. However, it is more of a challenge for designers to understand the critical parameters and the design techniques that define optimum backplane performance.

Medium- and high-performance backplanes should be considered transmission lines with distributed capacitive loads. The means by which the loads are laid out and the individual as well as total capacitive values have the single largest effects on signal propagation down the backplane.

Termination design is critical to high-performance backplane design because design of the termination circuit affects the existence of reflections on the backplane, and, therefore, has an impact on maximum frequency.

All of these parameters have a direct impact on maximum frequency and this impact defines the maximum backplane throughput.