FAIRCHILD SEMICONDUCTOR™

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Section 5 - Backplane Signal Conditioning Backplane Designer's Guide

One of the most important decisions that a backplane designer makes when defining system performance is the selection of the driver integrated circuit (IC) or IC input/output (I/O) technology. To achieve a high level of signal integrity, the physical backplane must be designed with specific signal behavior in mind. The physical backplane includes, but is not limited to, the number of loads, the number of outputs switching, and the termination type. Signal behavior refers to characteristics such as frequency, static and dynamic drive, edge rate, and incident wave or reflected-wave switching.

Although backplane design as a whole determines signal behavior, the choice of driver technology affects the behavior of the signals traveling the backplane and the upper performance limit of these signals. Driver technology defines the maximum parameters for dynamic switching current, static current, edge rate, and frequency. Although the backplane design can be tuned to take advantage of these parameters, or designed for more conservative operation, the driver technology defines the upper limits.

Because of driver technology's impact on the system as a whole, understanding backplane requirements and the role driver ICs play in signal behavior and backplane functioning are critical when selecting a driver IC.

Section Reference

This section covers:

- Dynamic and Static Drive Characteristics
- Signal Edge Rates
- Signal Propagation and Flight Time
- Incident Wave and Reflected Wave Switching
- Power Consumption
- Live Insertion
- Pin Conditioning

Section	Section Title	Contents
1	Introduction	Application demands, basic backplane considerations, and how to use this guide.
2	Backplane Protocols	Descriptions of different backplane bus protocols, including PCI- and VME-based protocols.
3	Backplane Architecture	Topics relevant to backplane configuration, including parallel versus serial configuration and different configuration topologies and timing architectures
4	Backplane Design Considerations	Issues relevant to backplane layout, including distributed capacitance, transmission line effect, stub length, termination, and throughput.
5	**Backplane Signal Driving and Conditioning**	**Signal driving and conditioning, including power consumption, rise/fall time, propagation delay, flight time, device drive, pin conditioning, live insertion, and incident wave switching.**
6	Noise, Cross-talk, Jitter, Skew and EMI	A review of the enemies of signal integrity and high frequency.
7	Transceiver Technologies	Detailed information about the following technologies: TTL-based (ABT, FCT, and LVT); ECL; and GTLP.
8	Mechanical Considerations	Information about mechanical considerations such as backplane chassis/cages and connectors.
9	Layout Considerations	Physical layout of the receiver and driver cards plugged into the backplane, primarily focusing on construction of the physical layer and the configuration of the devices that comprise the cards.

Drive Characteristics

Drive is the capacity of a device to sink or source current. For this reason it needs to be considered when determining if a device will be capable of operating in a specific environment. Conventional technology devices source current from V_{CC} when the output is conditioned HIGH. These devices sink current to ground when conditioned LOW. This is illustrated in Figure 1.

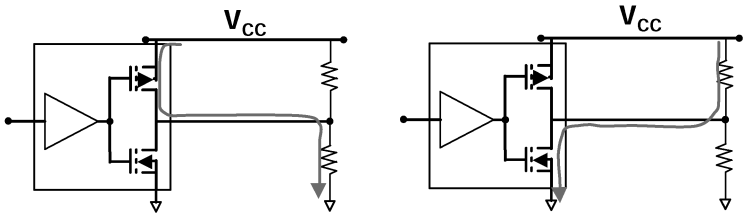

FIGURE 1. A Driver sourcing current to a load (left) and sinking current from a load (right)

Static drive is the current supplied or sunk when Voltage Out High (V_{OH}) or Voltage Out Low (V_{OL}) levels have been reached. Dynamic drive is the amount of current that can be supplied or sunk during switching.

Each application varies in the amount of drive needed because the amount of drive is based on the number of loads in an application and the speed or edge rate needed to switch them. In every application, a minimum amount of drive is required to achieve the required edge rates, and to achieve and maintain the correct V_{OL} and V_{OH} levels.

Static Drive

When it is not switching, an output is referred to as static. This means it is trying to maintain a DC voltage level. The static output drive of a device is a measure of the current available at a steady state, non-switching output. A device with high static drive is useful in applications that use resistive termination methods.

Static drive datasheet specifications are usually listed as Current Output Low (I_{OL}) and Current Output High (I_{OH}). These ratings reflect the ability of an output to source or sink a specified current. I_{OL}/I_{OH} ratings are typically the maximum recommended output current per bit.

When dealing with the issue of backplane current drive, simple equations can be used to calculate the load dependent static drive of a backplane. This calculation is an Ohms law equation: V = IR to I = V/R. In backplane terminology this equates to:

$I_{LOAD} = V_T / R_T$

Where:

I_{LOAD} = The Output Load Current

V_T = Termination Voltage

R_T = Termination Resistance

For example, in a backplane using GTLP devices as in Figure 2, The I_{OL} current can be calculated by taking the termination voltage (usually 1.5V) and dividing by the equivalent termination resistance of 50Ω in parallel. The following equations demonstrate this:

$I = V / R$

$I_{OL} = V_T / R_T$ (for GTLP using a parallel termination setup)

Resulting in:

$$I_{OL} = \frac{1.5V}{[1/(1/50+1/50)]} = 60\ mA$$

The variable of R_T can be adjusted so that, I_{OL} < Max I_{OL} of a device. I_{OL} can be thought of as the load-dependant, static current drive in this backplane application.

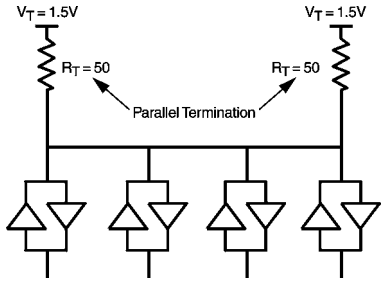

FIGURE 2. Backplane using GTLP Open Drain Devices and 50Ω Termination

Drive Characteristics (Continued)

Dynamic Drive

Dynamic drive is a measure of a device's ability to charge or discharge a load during switching. The driving device must effectively transition from a sourcing current to a sinking current or visa versa. The dynamic drive strength of a device will define the switching speeds of that device in a variety of applications. Typically, the higher a device family's rated output drive, the better or "faster" it will pull a load to a high state or to ground. However, both CMOS and BiCMOS output structures offer a nonlinear response to changes in current and voltage as shown in Figure 3. The voltage out verses current out curves show that the resistance of the output structures varies across voltage levels.

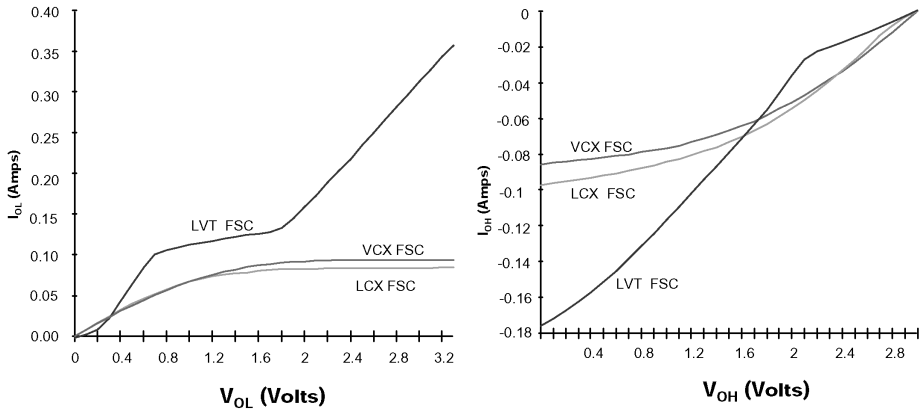

FIGURE 3. Output Characteristics for some of Fairchild Semiconductor's CMOS and BiCMOS Families

In addition to a nonlinear drive response over voltage and current, specific device family performance attributes need to be taken into account. Some families, such as LVT do not have balanced output drives. The LVT family is designed and specified with an I_{OH} of 32 mA and an I_{OL} of 64 mA at 3.3 V_{CC}. The LVT design gives this family different switching performance behavior between LOW-to-HIGH and HIGH-to-LOW transitions.

GTLP backplane drivers also have an unusual output structure. GTLP outputs are open drain and designed to work with a pull-up termination. With this technology, the termination defines the LOW-to-HIGH transition edge rate, LOW-to-HIGH dynamic drive, and the available static I_{OH}.

Drive and Load Relationships

Output signal behavior of a driver device will directly depend on the backplane environment that the device senses during operation. Both load composition and load size affect the V_{OL} and V_{OH} and output edge rate of a driving device.

Different components of the load affect the static and dynamic drive components. The static component of the output drive will see the load as purely resistive. The resistive load component affects V_{OH} and V_{OL} levels. The dynamic component of the output drive will see an impedance characteristic. The impedance will be in the form of capacitance and inductance due to the change in voltage and current over time. The load impedance will have a direct impact on driver output edge rates.

Due to wide load variation from system to system, it is important to understand how driver propagation delay and edge rates vary with loading.

The output load does not affect the internal propagation delay of a device. However, the effective propagation delay will change with output load size. Propagation delay variability is due to the change in output edge rates that are directly affected by the load. The longer the output edge takes to cross the threshold switch point, the higher the measured propagation delay time will be. In addition, the longer the signal spends driving to a HIGH or a LOW, the less time available for a valid V_{OL} and V_{OH}. Therefore, edge rate and loading have a direct impact on system maximum frequency and can significantly impact timing and skew.

It may appear that the easiest solution is to design backplane drivers with the highest rated drive, but too much drive can create as many problems as too little. Very fast edge rates can produce large under- and overshoots, generate cross-talk, and create undesirable transmission line effects. Fast edge rates also generate more Electromagnetic Interference (EMI) radiation than slower edges do. Another caution when using high-drive technologies is the amount of power these technologies dissipate. Increased power dissipation requires a corresponding increase in the backplane and total design power budget.

Conversely, too little drive in the application will cause a loss of V_{OH} and V_{OL} and a slowing of the edge rates in addition to a reduction in maximum frequency. The loss of V_{OL} and V_{OH} can limit signal threshold and noise margin resulting in signal integrity problems. Very slow edge rates cause the signal to spend too much time in the device threshold region, and this delay can result in false switching and oscillations.

Drive Characteristics (Continued)

An understanding of driver technology output characteristics and how to calculate behavior for specific applications is critical for an optimized design.

Calculating Needed Drive

If a system is to be designed with pull-up and pull-down termination, the designer will have to calculate the required DC static drive. When the output drives a static load, the maximum current the output supplies is an Ohms law calculation of the difference in potential across the equivalent static load resistance seen by the driver. This calculation was discussed previously in the section on static drives. The calculated I_{OL} or I_{OH} current can be used to compare datasheet specifications.

When determining the dynamic drive requirements, it is critical to look at all components of the load environment. Most environments demand a particular set of dynamic drive requirements. I_{OL} and I_{OH} curves can be used to approximate the capability of the device to switch complex loads (represented by R, L, and C components). Driver performance in an application can be calculated with a Bergeron plot. This is accomplished using I_{OL} and I_{OH} curves as well as matching V_{IN} curves. The result is a current performance envelope for the driver and load lines that can be used to understand how it will perform in the application. An explanation of how to calculate and use Bergeron plots is included in the "Descriptions and Family Characteristics Section" of the Fairchild Semiconductor FACT™ family databook.

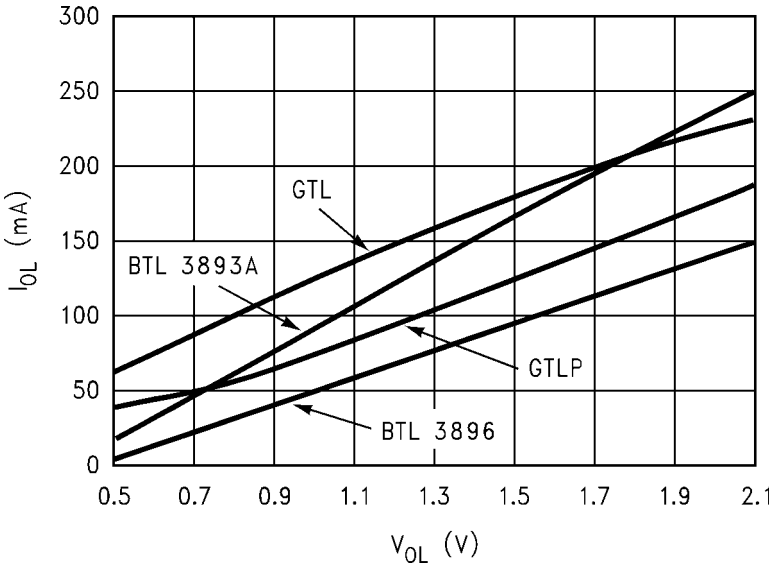

FIGURE 4. Typical Backplane Driver I_{OL} Characteristics

A simpler calculation method is to calculate the application load line and overlay the I_{OL} and I_{OH} curves. Figure 4 shows the I_{OL} curves of four backplane driver technologies. Device I_{OL} and I_{OH} curves establish the upper bounds of the envelope of available current for switching a complex load. The output load limits the usable drive of a device, and its characteristic can be drawn as a load line.

The drive characteristics and load line characteristics can be mapped on the same plot to demonstrate the dynamic operating range of a device. The performance of a GTLP device in a 50Ω backplane environment has been plotted in Figure 5. The load line is calculated for 25Ω rather than 50Ω because the driving device will see two 50Ω parallel paths to ground, resulting in the equivalent of a 25Ω load.

Drive Characteristics (Continued)

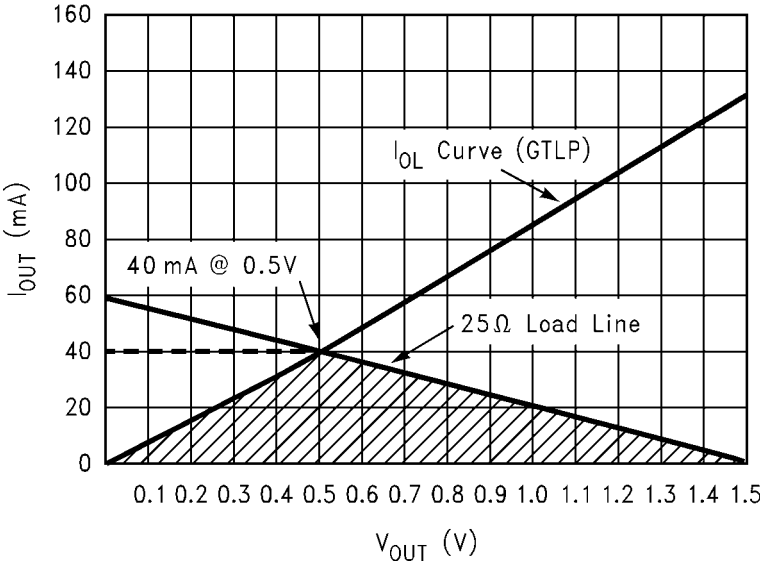

FIGURE 5. GTLP16612 I_{OL} Curve and 25Ω System Impedance Load Line

At some point on the graph, the load line will intersect with device I_{OL} drive characteristics. The shaded area under the curve represents the available drive current in that application during a switching event from HIGH-to-LOW. The intersection of the load line and the device output drive represents the maximum output drive current available in the application.

Given a fixed load line, better device drive performance will shift the intersection toward higher available dynamic drive and allow lower V_{OL} levels for static conditions. The intersection also represents the theoretical incident wave switching amplitude.

The fastest and most accurate method for determining the dynamic drive requirements would be to run system simulations using the proposed driver model. Most semiconductor manufacturers offer Spice and IBIS models of their devices.

When designing backplane architecture with the goal of incident wave switching, it is critical to consider the load line and drive curve relationship. Making trade-off decisions with backplane impedance, termination schemes, and device driver technology will improve incident wave switching performance. It is important to consider performance trade-offs when optimizing backplane performance for incident wave switching designs.

Reducing the backplane characteristic impedance or opting for a higher current device driver increases the noise characteristics of overshoot and undershoot. The driver also exhibits fast edge rate characteristics that are a significant cause of system-generated Electrical Magnetic Interference (EMI). The optimum balance of these parameters governs the data rate performance of the backplane.

The Resistive Load

Resistance in an output load is seen primarily when a system has DC coupling to V_{CC} or ground. DC coupling can be divided into two types. The first, signal termination structures, provide DC coupling. These types include the Thevenin voltage divider and DC termination (essentially a line impedance-matched resistor tied to ground). The second type, conditioning resistors, are pull-up and pull-down resistors, normally in the 10Ω to 50Ω range, which are used to condition undriven inputs.

DC coupling has only a minimal effect on active edge rates. To some degree, a resistor will help the edge rate in the direction that it is tied. For example, a DC 100Ω termination to ground resistance will speed the HIGH-to-LOW edge transition. This increase in speed is due to the resistor acting in parallel with the device output to sink current. Conversely, some negative effect may be seen on the opposite driver edge because of the higher amount of current that the driver will have to source. The lower the resistor's value, the more impact the resistor will have on edge rates.

V_{OL} and V_{OH} levels and system power may be affected significantly by DC coupling, depending upon the design scheme and the values used. In simplest terms, the smaller the resistive value, the larger its impact on V_{OL}/ V_{OH} levels and power usage.

Device output drive will also have an impact on how DC coupling affects edge rates as well as V_{OL} and V_{OH} levels. Adverse effects can be minimized or eliminated by using medium drive (24 mA) or high drive device families (≥ 50 mA). DC coupling will have a greater effect on edge rates, as well as V_{OL} and V_{OH} when lower drive families (≤ 12 mA) are used.

DC coupling will have a direct impact on disable time edge rates. For conditioning resistors due to very low disable times, a system designer must compromise between active

Drive Characteristics (Continued)

system power consumption and Switching Power Consumption.

The Capacitive Load

The size of the capacitive portion of the load has the single largest loading impact on switching edge rate. When driving a capacitive load, the On Resistance as well as the saturation point of a device output limit the transition time. This limitation is due to the finite rate at which the output load can be charged or discharged. This behavior is essentially the same for a Bipolar, BiCMOS, or CMOS device. When a transistor enters saturation, the transistor acts as a constant current source.

$$\Delta V = \frac{I\,\Delta t}{C}$$

Where:

ΔV = Change in Voltage Across the Capacitive Load

I = Saturation Current

Δt = Change in Time

C = Capacitance Value of the Output Load

When the transistor charges or discharges the load to the point where it falls out of saturation mode, the device acts resistive, and the RC time constant takes over charge/ discharge rate.

$$\Delta V = \frac{I(t)\,\Delta t}{C}$$

Where:

ΔV = Change in Voltage Across the Capacitive Load

$I(t)$ = Instantaneous Current

Δt = Change in Time

C = Capacitance Value of the Output Load

Rise and Fall Time

Rise time is the amount of time required for the output to rise from its V_{OL} value to its V_{OH} value. The opposite of rise time is fall time, the time it takes a signal to fall from V_{OH} to V_{OL}. Typically these values are measured from 10% to 90%. Figure 6 shows rise and fall times with typical measure points.

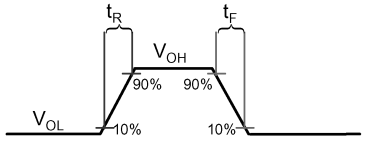

FIGURE 6. Rise and Fall Times with 10% to 90% Measure Points

Another term for rise and fall time is edge rate. Many factors affect device output edge rate, including type of driver, stub length, distributed capacitance, impedance of the backplane, termination, and noise.

To help select a driver, check the manufacturer's databook and look for a device that offers edge rates that will fit into the system's window of operation. Static output drive specifications are a good indicator of device edge rate. In simplified terms, the higher the I_{OH} and I_{OL} values, the faster the edge rate.

As noted in the section on dynamic drive, many high-drive backplane technologies have "unbalanced output drive" specifications. For example, LVT and ABT devices are specified with an I_{OH} of 32mA and an I_{OL} of 64mA, into an equivalent load. The fall time of these devices will be faster than the rise time. Another example of different rise- and fall-time behavior is GTLP devices, which uses an open drain pull-down output structure. GTLP devices are designed for use with a pull-up termination matched to the application impedance. This results in a fall time that is determined by the GTLP device and the application. However, the GTLP device has no effect on rise time, which is determined by the termination structure.

Other factors, such as dynamic drive capability, device edge rate control, and the application load have significant effects on output edge rates. However, when reviewing driver technologies, the specified I_{OH} and I_{OL} values are useful for gaining a rudimentary understanding of device edge-rate performance.

Stub Effects on Edge Rate

Backplane stubs have a significant effect on the signal as it propagates down the backplane. The number of stubs, their placement, their length, and their capacitance all have an effect on the signal edge rate.

Stub Length Effects

The length of the stub directly effects the rise time of a backplane driver. Stub length effects become more significant if the length of the stub is greater than 1/3 the signal edge rate. At stub lengths greater than 1/3 of signal edge rate, transmission line reflections can become significant. With no termination on the stub, reflections from the stub are seen on the bus. These reflections are seen as a step out or ledge on the signal edge. The longer the stub length in relation to edge rate, the more significant the step out becomes.

Because of this relationship and to promote good signal integrity, the length of the stub must be properly sized so that the rise time fits the system's requirements. For most applications, this will result in the shortest stub length possible.

Stub Capacitance

The capacitance of the stub is a combination of the stub and all components on the stub, such as a device I/O. This capacitance is seen on the rising edge as small voltage dips that are caused by the charging effect of the capacitance as the wave front passes the stub. Each stub induces a voltage dip. The additive effect is to roll the edge over, slowing the edge rate as it propagates down the bus. More information on stub capacitance effects is in Section 4 of this Backplane Designer's Guide, "Backplane Design Considerations."

Propagation Delay

Propagation delay is the delay per unit length of a signal traveling down a transmission line. Propagation delay is usually expressed in terms of inductance and capacitance, as shown in the equation:

$$t_{PD} = \sqrt{LC}$$

Where:

L = Distributed Inductance

t_{PD} = Propagation Delay

C = Distributed Capacitance

Propagation delay is affected by many factors. The amount of propagation delay depends on load size and composition, signal rise and fall times, flight times, noise margins, and transmission line effects. Propagation delay affects the timing and speed in an asynchronous system and signal skew in a synchronous system. In designing high-performance backplanes, it is important to account for the amount of delay the backplane design will have.

Flight Time

Flight time can be defined as the time it takes a signal to propagate from the driver to the farthest receiver on the backplane. Flight time depends on factors such as:

- Length of the backplane
- Permittivity of the trace and board material

  Number of receivers
- Capacitance and length of the stubs and connectors

Calculation of Total Propagation Delay

The total propagation delay of a backplane can be calculated as the sum of the devices in the system, as shown in the following calculation.

$$\text{Total } t_{PD} = t_{PD}\text{ (driver)} + t_{PD}\text{ (receiver)} + t_{PD}\text{ (backplane)}$$

Where:

t_{PD}(driver) = Driver Propagation Delay

t_{PD}(receiver) = Receiver Propagation Delay

t_{PD}(backplane) = Backplane Propagation Delay

This equation takes into account the propagation delays of the overall design that affect system speed and assumes incident wave switching. Another calculation can be performed to determine the effective propagation (t_{PD}') of a backplane. The equation for this calculation is:

$$t_{PD}' = \sqrt{L\left(C + \frac{NC_L}{X}\right)}$$

Where:

L = Distributed Inductance

C = Distributed Capacitance

C_L = Total Load Capacitance

N = Number of Loads

X = Line Length Over which the Loads are Distributed

This equation illustrates that the backplane number of capacitive loads and the distributed capacitance have a significant effect on propagation delay.

Driver Propagation Delay

Driver propagation delay is also critical for backplane design. The driver's internal propagation delay will affect backplane switching speed and throughput. Typically, the driver's propagation delay is measured as the difference in time from the input signal to the output signal, and it can be measured as the LOW-to-HIGH transition and the HIGH-to-LOW transition. Device families offer a wide and growing range of propagation delays. When choosing a device technology, it is important to select one that fits in the timing window while satisfying all the other requirements of the design.

Incident Wave Switching

Incident Wave Switching (IWS) is the ability of a device to provide an initial (or incident wave) voltage step of sufficient amplitude across the entire backplane so as to be recognized by all the receivers as a valid change in state. A signal with sufficient amplitude would have the initial rising or falling edge reaching a valid input-low and input-high voltage state. This is also referred to as a monotonic signal edge.

The driver must generate this monotonic edge during the first propagation down the backplane. If the transceiver cannot switch the bus on the incident wave, then it must rely on a minimum of one reflection to raise or lower the bus voltage above the threshold region of the receiving device.

Improving Throughput with Incident Wave Switching

The ability of a driving device to achieve incident wave switching in a backplane environment improves the throughput of the system. Incident wave switching allows increased data/clock frequencies because it eliminates the need to wait for a reflected wave front to achieve a valid V_{IH} or V_{IL} receiver level across a backplane.

In an equivalent backplane, incident wave switching can almost double the frequency over reflected wave switching. This is because all receivers recognize a state change on the initial wave front, resulting in a reduction of the bus signal propagation delay by one-half. The frequency increase will generate substantial gains in data rates. The result is a dramatic improvement in throughput.

Factors of Incident Wave Switching

Optimization of a backplane environment for incident wave switching requires careful design and control of many factors. These factors include low capacitive loading through low driver/receiver capacitance, small stub lengths, efficient connectors, and correct termination. These characteristics reduce voltage reflections from discontinuities at each receiver/connector interface to the backplane. An impedance balancing backplane improves IWS by reducing the reflections generated in the system.

Non-incident Wave Switching

For TTL solutions such as ABT, LVT, and FCT, incident wave switching will be accomplished only in the most ideal backplane environment. In many applications, these three device technologies rely on a reflected wave to signal the

Incident Wave Switching (Continued)

drivers in a backplane. Because of this, many TTL devices are categorized as non-incident wave switching devices.

The problem with non-incident wave switching is the increased time taken by the driver to signal the receivers, decreasing the speed at which the backplane operates. Figure 7 illustrates a backplane with a reflected signal.

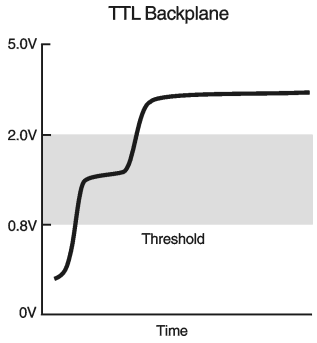

FIGURE 7. Nonmonotonic Backplane Signal. This requires a reflection to enable the receivers to change states.

GTLP Incident Wave Switching Technology

The GTLP family of devices was specifically designed to achieve incident wave switching. GTLP achieves this on the first signal that is propagated through the backplane. This increases the efficiency of the device and the backplane. Figure 8 shows a clean incident wave switching backplane using a GTLP device.

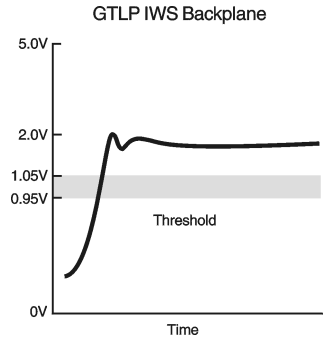

FIGURE 8. GTLP Incident Wave Switching Backplane

Input and Output Pin Conditioning

Input and output pin conditioning in a system is critical to proper system performance. Digital signal input pins must be kept at valid logic levels regardless of whether the device is driving signals or is in high-impedance mode (also known as 3-STATE). A device input with no signal present is referred to as “floating”. If device data and control pins are allowed to float or are left in an unknown state, system power dissipation can increase significantly. False signals, system damage, and device damage, are also possible results of floating pins.

Floating Inputs

Allowing inputs to float should be avoided. CMOS and

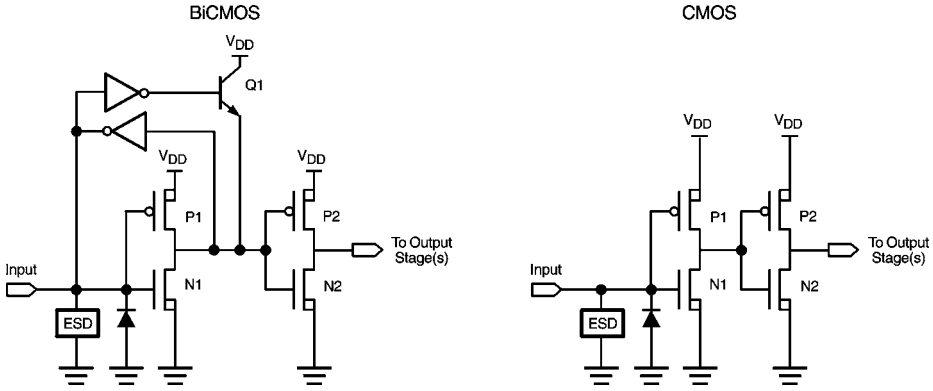

FIGURE 9. BiCMOS and CMOS Input Structures

Stray signals introduced into a floating CMOS gate can cause the device to begin to switch. When the device reacts to these stray signals, it will switch back and forth and may develop self-sustaining oscillations that cause internal device I_{CC} to rise significantly. If these oscillations persist in the device, heat and even thermal damage are likely to result. If the device is connected to a bus and the output is not in High Z, the entire bus can be driven into oscillations. This multiplies potential problems by the number of devices on the bus, significantly affecting the system power budget as well as system and device heat dissipation and causing potential device thermal damage.

Some older Bipolar system designs allowed unused inputs, or inputs of devices in High-Z to float. Because of their design, bipolar devices are less susceptible than CMOS devices to letting spurious input signals on the base causing oscillations. However, less susceptible should not be interpreted as immune. Ground bounce or cross-talk can cause signals on a floating transistor base to develop oscillations in the device. The resulting problems are the same as those seen in a CMOS device.

Conditioning Solutions

There are multiple solutions for conditioning undriven inputs. Each method has benefits and potential drawbacks. System design and system requirements will play a major role in which type, and in what system locations, each is appropriate.

Common requirements that come into the design decision process include active and standby power consumption, signal termination requirements, mixed supply voltage operation, partial system power-down, and live-insertion requirements. The need for one or more of these will affect the decision of which type or types of conditioning solutions are appropriate. External conditioning methods are the most common methods of input conditioning. There are multiple types of external conditioning.

Pull-up and Pull-down Conditioning

The standard design uses a resistor connected to V_{CC} or ground to pull the input to a valid high or low state. If the devices being conditioned are pure CMOS, conditioning the outputs HIGH or LOW is acceptable. With BiCMOS or Bipolar devices, it is generally recommended that the devices be conditioned so that the outputs are in a high state. The output structures of most BiCMOS and Bipolar device families are designed so that the devices generate much lower static I_{CC} when the outputs are driven HIGH. Consult the data sheet or a vendor manufacturer for family specifications.

Conditioning Resistor Example

An example of pull-up and pull-down conditioning resistors used in a system can be seen in a preliminary Double Data Rate (DDR) SDRAM specification as in Figure 10. The bus switch IC is defined to incorporate a pull-down resistor for the DDR module data bus. This resistor ensures that SDRAM ICs on the module will never draw excessive current due to a floating memory system data bus.

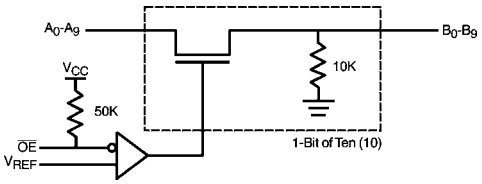

FIGURE 10. DDR Bus Switch with Pull-down and Pull-up Resistors

A critical design consideration in implementation is the impact of the pull-down resistor on the SDRAM input edge rate. This answer can be calculated given the input and board capacitance on a given trace along with the pull-down resistor value.

This configuration requires two memory I/O devices on each data bit shown in Figure 10. With an I/O capacitance of 6.5pF per memory device and about 2 inches of PCB trace, at 2pF/inch, the total capacitance on each bit of the B Port will be 17pF. The time constant of this RC network is 170ns.

The disable fall time can be approximated with the formula:

$$t_F = RC / 0.67\ V_{CC} = 77ns / V$$

Where:

t_F = Disabled Falling Edge

0.67 V ≅ 1 Time Constant

V_{CC} = 3.3V

RC = Resistor Capacitive

Logic device input slew rate is generally specified to be in the range of 0-10ns/V. However, the calculations show it is all but impossible to guarantee an edge rate of 10ns/V and maintain a reasonable DC power consumption per bit on the bus in this example. With all system signal lines switching at a 50% duty cycle, DC power will be consumed for 50% of the cycle when the bus is active.

During the transition to inactivity, system power will be consumed in the form of an increased I_{CCT} current component for every listener on the bus. This is due to the slow falling disable signal caused by the relatively large (~10K) pull-down resistor value.

In the example shown in Figure 10, a pull-down resistor value of 1K would be required to guarantee a sub 10ns/V input edge rate. This lower resistance would increase the total power dissipation on the SDRAM module by 400 mW, typically and over 750 mW in some extreme cases.

Signal Termination Conditioning

In addition, their primary function of damping out reflections and noise present on signal lines and backplanes, some signal termination designs can provide a valid logic level during disable states. Two types work well for both termination and conditioning needs.

Thevenin Termination

Thevenin termination is usually employed in a multidrop environment such as in cable driving or a backplane. If this termination is set up with resistor values that ensure the bus will be pulled to a valid Voltage Input High (V_{IH}) or Voltage Input Low (V_{IL}), it will both dampen out reflections and noise as well as ensure that undriven inputs are pulled to a valid level. This scheme works best with output drivers capable of sinking heavy DC loads. The drawback to this termination design is high static power dissipation.

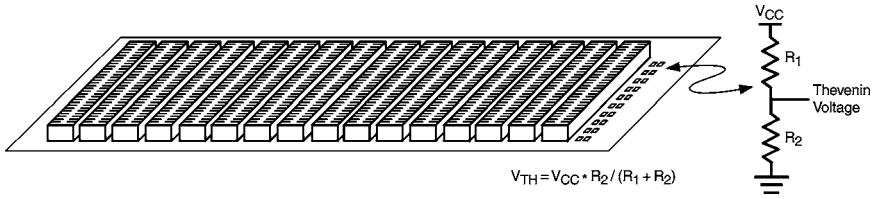

FIGURE 11. VME Backplane with Thevenin Termination

Conditioning Solutions (Continued)

Parallel Termination

Also called DC termination, parallel termination normally consists of a resistor tied to ground to dampen undershoot. This termination will pull all inputs on the bus LOW during inactive or High Z conditions. The penalty from this design is high power dissipation when the inputs are driven to a logic HIGH.

The difference between parallel termination and conditioning resistors is the value of the resistor used. Parallel termination is designed to impedance-match the line and dampen out undershoot, whereas conditioning resistors are sized simply to pull an unused input LOW. This means that a resistor selected for parallel termination is normally a low value and this requires output drivers capable of sinking heavy DC loads. A conditioning resistor is normally a high value ($\geq$ 10 kΩ) to avoid excessive power usage.

Bus-arbitration Unit

The bus-arbitration unit solution is for large systems and often used to complement the termination resistor solutions. It uses a bus master or bus-arbitration unit to actively drive the bus to a known state during periods of inactivity. The Peripheral Component Interface (PCI) in Figure 12 is an example of a bus architecture that uses a combination of bus master drive and pull-down resistors.

Internal Device Conditioning Techniques

Some device designs incorporate specialized internal circuitry to prevent floating inputs. These designs include bus-hold and internal pull-down resistors. These conditioning methods have the advantage of needing no external components, landing pads, or additional trace lines

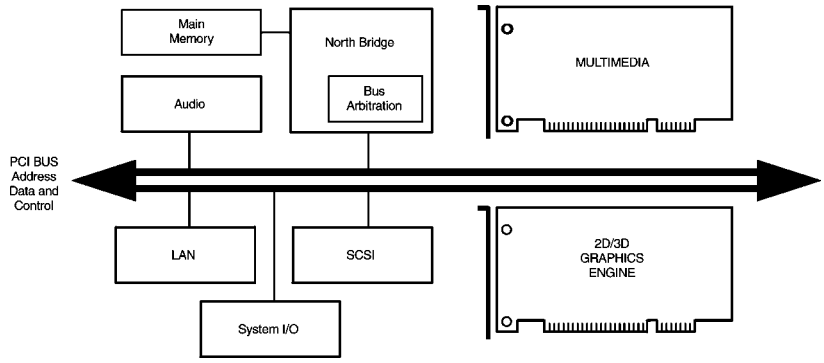

FIGURE 12. PCI Bus Arbitration with North Bridge

Bushold

Bushold works by incorporating a low drive latch in the input stage as in Figure 13. When the input signal is removed, the bushold latch will hold the input, and any other inputs on the bus, at the last valid logic input level. The bushold circuit will maintain this level until it overdriven by the next valid input. An additional benefit is that by holding the device or bus at the last received valid input level, bushold devices can serve a pseudo-memory function. In contrast, a conditioning resistor will always pull the bus to the same state.

Internal Pull-down Resistors

Internal pull-down resistors are switched out of the circuit when the device is not in High Z. The benefit of this device type is that during normal switching no additional power or edge rate penalty is incurred because the conditioning resistor is disconnected. An example of this device type is the Fairchild Semiconductor LCXP16245 in Figure 14. The "P" designation denotes internal pull-down resistors.

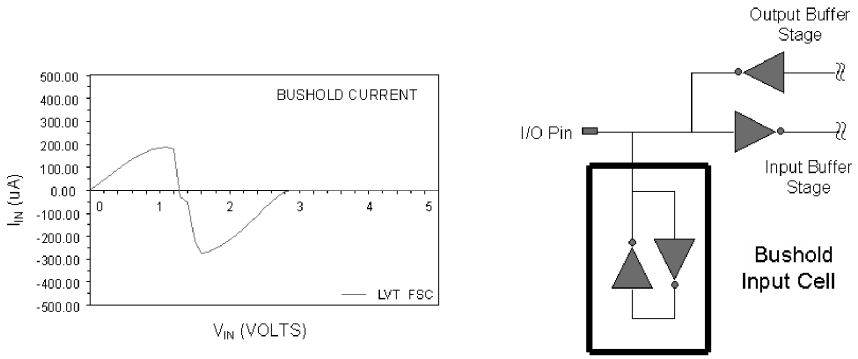

FIGURE 13. Bushold Input or Transceiver Input/Output

Bushold (Continued)

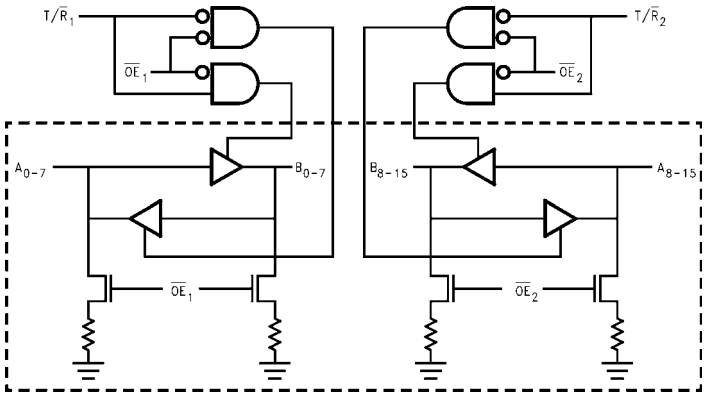

FIGURE 14. Fairchild Semiconductor LCXP16245 with Internal Pull-down Resisters

Control Pin Considerations

The conditioning of device control pins needs special consideration. Control pins should never be allowed to float for all the reasons stated in the section on floating inputs. Because of their functions, control pins have an increased potential for data corruption and reliability problems in comparison to data pins. Therefore, care and planning for control pin logic condition during all system operational states is vital to a robust design.

The power-up and power-down cycles are a critical time for conditioning and must not be overlooked. It is recommended that output enable (OE) control pins be tied via a resistor to the voltage level that makes them active. For example, if the device OE control pin is active LOW, i.e., a high logic level on the OE pin places the device in High Z, the OE pin should be tied to V_{CC} through a resistor. This will ensure that the device will switch into 3-STATE, if no signal is present on the OE pin.

Devices with the power-up High Z feature should not be assumed to be immune from problems. For example, if a device is specified to remain in a high-impedance state at a voltage of 1.5 volts or below, and is running in a system with a V_{CC} of 3.3 volts, there is a potential unknown state between 1.5 volts and 2 volts as illustrated in Figure 15.

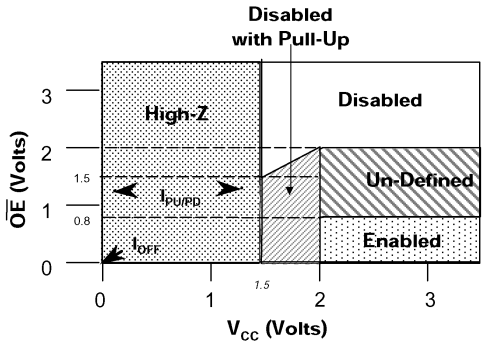

FIGURE 15. Diagram illustrating power-up High Z diagram for the LVT device family output state diagram. Note that between 1.5V and 2V is an unknown state. If left unconditioned, the device may begin driving signals.

In this situation, it is possible that some system devices will begin to operate and drive signals before other system devices are fully powered up. By adding a pull-up resistor, power-up and power-down protection are raised to the full system operating level. All device control pins should be tied to a valid logic level through a resistor. This powers the device up into a known state and provides a known default state if the input signal is removed.

Output Pin Conditioning

Output pin conditioning is in a large part the result of system design requirements. It is acceptable to float output pins provided the device inputs are properly conditioned.

Bus contention is the state where one or more devices on a bus are driving LOW at the same time that one or more devices on the same bus are pulling HIGH. Careful consideration must be taken to ensure bus contention does not occur because it may result in significant system problems ranging from data faults to outright device and system failure.

Data faults result when slow transitions cause timing errors, or by lingering in the center invalid logic level for too long a period of time will cause glitches or oscillations resulting in data faults.

System damage occurs when devices on the bus attempt to source or sink excessive amounts of current either for extended periods or during repeated cycles. These large currents can generate extreme thermal stresses, leading to premature device failure. In addition to device failure, thermal damage can extend to the board itself and, potentially, overstress the power supply. Avoiding bus contention will ensure a safe, low-fault environment.

Live Insertion

Live insertion or hot swap can be defined as the insertion or removal of modules from a system that is in a powered state. The need for systems with live-insertion capability has been present for some time and this requirement has grown exponentially with the proliferation of communications and data systems into many aspects of society. If proper precautions are not taken with live insertion techniques, operational disruption, data corruption, and system damage are all possible. Therefore, thorough understanding of proper design and insertion techniques is critical for a reliable system that incorporated hot swap capability.

Levels of Isolation

In hot-swap systems, varying levels of ability are required. For example, in some systems it is only necessary to swap modules without damaging the powered system. In these cases, interruption of data flow and normal operation are permissible. Other systems of a more critical nature require more involved criteria so that full operation is maintained during module replacement.

Two often-cited examples of systems requiring full hot-swap-ability are air traffic control systems and telephone switching centers. Additional examples include electrical power grid control systems and banking systems. The list continues to grow. Typically, there are three classification levels of live insertion. These definitions may vary slightly between manufacturers, but they are generally the same.

- The first level of isolation states that the ability of the interface device must allow live insertion of the board without having to power down the system.
- The second level of isolation states that the interface device must allow board insertion without having to power down the system or suspend bus activity.
- The third level of isolation states that the interface device must allow board insertion without any limitations, restrictions, or requirements of other circuits.

Solutions and Recommendations

System-level Solutions

System-level design solutions and recommendations are exhaustively covered in many published articles and white papers as well as in industry specifications such as the CompactPCI® Hot Swap Specification. Consequently, this presentation will be a high-level discussion focusing on I/O devices and power up.

System damage, disruption, and false data signaling all stem from individual semiconductor and discrete device disruption or damage. Therefore, system integrity and protection are the direct result of device integrity and protection.

Board Connection Pin Layout

A staggered pin layout is crucial to proper a hot-insertion design. Long ground, control, and power pins on the daughter card ensure connection before the signal pins as in Figure 16. Intermediate pin length is used for control signals such as board reset and output enable control, and intermediate power pins can be employed when sequential board power up is used. This pin layout allows board devices to power up and achieve a stable state before receiving and sending signals to and from the bus.

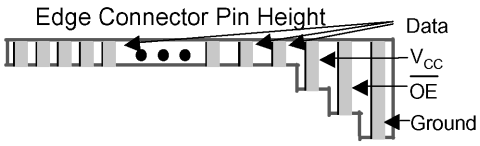

FIGURE 16. Staggered Card Edge Connections for Hot Swap

Pull-up and Pull-down Resistors

The use of conditioning resistors is a common way to place devices in a known state during power-up or power-down cycles as well as to keep an inactive data bus from floating. When the output-enable pins are tied HIGH, the device will be much less susceptible to transient signal spikes that could otherwise cause inadvertent device turn-on.

As noted in the section on pin conditioning, this is good design practice even when using devices with power-up high impedance. Using pull-ups on these devices gives additional assurance that the devices will not transmit signals prior to full-board or system power up. Other control signals can also be conditioned HIGH or LOW to help avoid the transmission of false signals.

Pre-charge Biasing Voltage

Pre-charge biasing voltage is used to place buffer outputs that connect to the bus at or near center switching voltage level. By placing the outputs at this level, less current is needed to charge or discharge the capacitance of the individual signal stubs and device outputs on the newly installed board. This results in less voltage disturbance (glitching) on the bus when a board is plugged in.

Implementation can take several forms. The most common is a resistor between the device output board trace line and a biasing level voltage line. Some off-board driver-specific devices incorporate a prebias voltage input pin and circuit

Solutions and Recommendations (Continued)

on the device, eliminating the need for pre-charge resistor pull-up connections.

Power Supply Regulation And Control

Power supply regulation is critical in any system. In a hot-insertion compliant system however, a new factor is added. When additional boards are plugged into or removed from a powered-up system, the supply will suddenly see a sharp increase or decrease in power demand. This is observed as large current swings and voltage spikes when a board is powered up or down.

It is critical to understand the power demands each board will make and to know how to regulate the supply voltage to avoid system disruption or damage. In addition to sizing the power supply to ensure it meets system hot-swap demands, current limiting resistors or filters are required to control the potentially damaging current flow during board power-up.

In systems where larger, more complex boards are used, power-up is often achieved in multiple steps. This is accomplished by splitting the board power planes and by connecting power to the board in two steps. Off-board drivers are powered first with the longest length power pins. Devices that do not drive signals off the board are powered up second, with intermediate length power pins. This design reduces the instantaneous current load on the system power supply during board power-up.

Another supply voltage design is the decentralized power method. Unstabilized voltage is applied to each module where regulation and stabilization take place. Even in this design, controlling current during board power-up is necessary to avoid voltage level fluctuations on the ground line.

Monitor and Control Circuits

Circuitry designed to monitor voltage level and to control device reset are commonplace in systems of medium complexity or greater. These circuits are designed to keep board devices in reset until a predetermined voltage threshold is reached, and to put devices or boards back into reset quickly if the voltage level drops below the threshold. Integrated circuits of this type coupled with external components are used to set specific voltage thresholds as well as to enable delay of when the part turns on and reset times.

Device-level Solutions

Semiconductor manufacturers have added device features that enhance system protection and increase hot-swap capability.

Power Up/down 3-STATE and Power-off 3-STATE

The power-up/power-down circuit is designed to keep the device outputs in a high impedance no-drive state during the time that the device is ramping to operating voltages. This feature is also activated during the power-down cycle. Internal circuitry holds the output enable (OE) circuit in 3-STATE until a predetermined voltage level is reached. This feature is specified on a data sheet as IPU/PD. Power off 3-STATE keeps a device from being powered up through an input or output pin. This feature is usually specified as I_{OFF}. These features prevent device damage and data corruption by keeping devices from driving signals before reaching operating voltage.

Over Voltage Tolerance (OVT)

OVT adds an additional level of protection to the device. This protection is useful whether it is used in a hot-swap application or not. In hot-swap applications, OVT adds protection in two ways. Devices connecting to the bus are protected from damage from active bus voltages before and during power-up and power-down. Also, during board power-up, devices may not reach operating voltage level at the same rate. OVT will protect devices that are slower to power up from signals driven by devices that have reached operating level.

Low Current Leakage (I_{OFF}, V_{ID}, I_{PU}, I_{PD}, $I_{OZH/L}$)

Current leakage is specified in a number of ways that cover leakage during varying device conditions. All of these conditions relate to OVT, and power-up and power-down 3-STATE. These design features prevent a device from sourcing or sinking current in inappropriate states.

- I_{OFF} — input and output power-off leakage current — is the current flow into or out of a device input or output with device powered down while forcing the tested input or output from 0V to device rated maximum high voltage.
- V_{ID} — voltage input current with the device off — is a variation of the I_{OFF} test. The device is held in a power-down state with all pins except the one under test at ground potential. Current is forced on the input under test. (Fairchild Semiconductor ABT spec is 1.9 uA.) The resulting voltage is measured
- I_{PU}/I_{PD} — current leakage on outputs during device power-up/power-down — is the current flow into or out of a device output during the power-up and power-down cycles.
- I_{OZH}/I_{OZL} — output off current — is the current flow into or out of an output in 3-STATE when a specified low or high voltage is applied to that output.

Undershoot Hardening

Often associated with buffers designed to drive memory modules, undershoot hardening has become more common for pass gates and bus switch devices. During hot-swap, glitches caused by current surges can result in pass gates and bus switches turning on if the undershoot is sufficiently negative. An undershoot of –0.8V on the drain or source of an NMOS switch will result in the device turning on. This will cause the data bus to be exposed to signals that could cause bus contention or data corruption. Undershoot protection provides isolation during live insertion by blocking voltages that could turn on a bus-switch or pass gate NMOS. This prevents unintended signals or glitches from reaching the bus and causing contention or data corruption.

Power Consumption

Power consumption is an important factor when designing a high-performance backplane. Design factors that contribute to the overall power consumption of a system include signal frequency, device and signal trace loads, signal duty cycle, termination, system V_{CC}, and component values.

Backplane interface devices can account for considerable system power. This is dependent on parameters such as the number of devices per board and the method by which the system is terminated. When designing a high-performance backplane, refer to the specifications of selected interface devices for the static power ratings and dynamic switching power requirements.

Power Consumption Due to Termination

Termination of a device in the backplane plays a role in the power consumption. As discussed in the termination sections of Section 4, a variety of designs are possible and all of them can affect power consumption.

For low-frequency signals, termination circuits without DC components will use less power (no termination, series termination, and AC parallel termination). At higher frequencies, parallel termination will consume less power because of lower AC power consumption. The AC power consumption of a parallel termination setup will include the termination capacitance at low frequencies.

The DC power consumption of a parallel termination will drop as duty cycles decrease. For very low duty cycle signals, this design may consume the least amount of power. At low frequencies, the slope of the AC parallel termination curve is greater than any other type of termination and is a function of three parameters: driver power dissipation capacitance, capacitance loading, and termination capacitance. At higher frequencies, the pulse width is less than the RC time constant and the slope starts to drop off. At a frequency less than that of parallel termination, the AC termination set-up will use less power than using no termination at all.

CMOS and BiCMOS Power Consumption

In some backplane applications, low power consumption is necessary and low power consuming devices must be used. Many devices rely on the CMOS technology for low power consumption.

For the CMOS and BiCMOS logic families, power consumption can be classified as two types: static power and dynamic power. Static power is the amount of power consumed when the device is driving a steady state LOW or HIGH level. Dynamic power consumption is the power consumed by the device during transition from LOW-to-HIGH or HIGH-to-LOW.

The following equations can be used to calculate static and dynamic power for CMOS and BiCMOS logic families. (Note: These power dissipation calculations can be found in any databook provided by a device manufacturer.)

CMOS:

Static Power: $PD_Q = (I_{CCq} * V_{CC}) + [(I_{CC} * DC_H * N_T) * V_{CC}]$

Dynamic Power: $PD_D = (C_L + C_{PD}) * (V_{CC})^2 * f_I$

BiCMOS:

Static Power $PD_Q = [(I_{CCL} * DC_H) + (I_{CCH} * DC_L)] + [(I_{CC} * DC_H * N_T) * V_{CC}]$

Dynamic Power $PD_D = [(C_L * V_{CC}{}^2 * F_I) * N_I] + [I_{CCD} * (F_{CP}/2 + F_I * N_I)]$

Where:

PD_Q = Static Power

$PD_{DYNAMIC}$ = Dynamic Power

C_{PD} = Power Dissipation Capacitance

C_L = Load Capacitance Output

f_I = Switching Frequency

I_{CCQ} = Quiescent Supply Current

I_{CCL} = The current flowing into the supply terminal when the outputs are in the high state

I_{CCH} = The current flowing into the supply terminal when the outputs are in the low state

I_{CCD} = The amount of current an IC will consume at a certain frequency

I_{CC} = Increase in I_{CC} per Input $V_{IH} = V_{CC} - 0.6V$

f_{CP} = Clock Frequency for Registered Devices

V_{CC} = Supply Voltage

N_T = Number of Inputs at V_{IH}

N_I = Number of Inputs at f_I

DC_L = LOW DC Current

DC_H = HIGH DC Current

Summary

Selection of the driver IC or I/O technology is a key parameter in defining backplane performance. The I/O technology will define the upper limits of system performance.

Driver technology defines the maximum parameters for dynamic switching current, static current, edge rate, and frequency. Due to its impact on these parameters, driver technology has a dramatic effect on backplane signal behavior. Signal behavior refers to characteristics such as frequency, static and dynamic drive, edge rate, and incident wave or reflected wave switching.

Other technology parameters that have a significant impact on backplane performance are hot-swap features and device power consumption.

When selecting driver technology, the designer should understand its crucial impact on backplane and signal behavior.