



Xilinx High-Speed Serial Backplane White Paper

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Reference Documents

Xilinx High-Speed Serial Backplane Routing Tradeoffs Guide

Glossary

Terms used throughout this document

Channel	A differential pair and its complementary direction pair (Tx and Rx).
Lane	Alternate naming for a channel. Sometimes referred to as x1, x2, x4, x8 lane to indicate multiple lanes (channels) aggregated to carry data.
Pair	Two signals each driven complementary (180 degrees out of phase).
Star	A routing concept where all nodes attach to a single point (hub).
Hub	The center of a star network.
Node	One of many end points in a star network.

Abstract

This white paper covers the design process implemented at Xilinx for developing a high-speed serial backplane to explore interconnects using a variety of connectors and PCB materials.

It is intended for persons needing to design a high-speed backplane but are either new to backplane design or who have only worked at sub-1Gbps speeds. Tools, methods, tradeoffs used during the development of the backplane are discussed.

Overview

The backplane *is* the backbone in a variety of systems deployed world-wide. Backplanes are used in telecom equipment, industrial controllers, flight-control systems, computing systems, and more. Backplanes are *not* a customer upgrade option for many reasons which forces the backplane to consider today *and* tomorrow's technologies or land in a scrap-pile as an obsolete piece of junk.

The challenge today is how to make a working backplane without pouring lots of unnecessary resources and costs into the design. This document introduces the reader to the most important aspects of backplane design and offers suggestions on what to focus on when making decisions.

Before you start

Before starting the design of a backplane the following items, at a minimum, will need to have been decided:

- Topology to use
- Minimum slot-pitch that can be tolerated
- Number of signals that need to be routed between slots
- Number voltages that need to be supplied to line cards
- Maximum thickness of line card
- Minimum and maximum thickness of backplane
- Link budget
- Specifications that need to be followed.

Designing the Backplane

During the design of the High Speed Serial Backplane, the following considerations were taken under consideration:

- Size
- Cost
- Number of layers
- Number of slots
- Materials
- Connectors
- Performance
- Interconnect topology

Although this particular backplane did not have to conform to a particular standard, most backplanes are standards based. The standard dictates the type of connector, pinout, and thickness whereas with a custom backplane the designer makes these choices.

Cost factors

Some of the more important factors that affect the overall cost of a backplane are:

- Connector type and quantity
- Number of layers
- Material types and thicknesses
- Panel size and utilization
- Number of drill holes and tolerance
- Back-drilling
- Edge plating

Connectors

There is no one connector that performs equally well for all backplanes. As stated previously, if the backplane is standards based then the connector and mechanical data is defined. However, when choosing a connector for a backplane it is important to consider the following:

- Signal density
- Signal crosstalk
- Slot pitch
- Cost

Sometimes a design can take advantage of a mix of connectors to achieve the needs of the system. The High Speed Serial Backplane for example uses the following connectors:

- Amphenol-TCS eHSD
- Tyco/Erni HM-Zd (ATCA Zone 2)
- Hard Metric 2mm (Type B with shield)

Tools

With today's interconnect speeds it is imperative to do channel simulations to determine whether or not the channel is going to work *before* the design enters the lab. Table 1 lists a number of tools that are considered to be capable of analyzing channel structures. This list is by no means complete and is provided as a general summary.

Engineers have always been faced with having to make tradeoffs between accurate simulation results and getting the product released. The challenge today is to make the product work today for tomorrow and keep the simulations simple but accurate.

In practice, a mixture of several tools is needed to accomplish proper channel modeling. Time domain analysis is needed since we are concerned about transient effects on the source signal and its arrival at the receiver. Frequency domain analysis is also needed for a landscape view of how the interconnect channel responds over a wide band of frequencies.

Element	Domain	Tool/Model type	Comments
Package	Freq	3D	Very good for analyzing multi-port structures in package. Must consider DC point interpolation issues
	Time	HSPICE/ IBIS	Package RLGC must be provided by vendor either by transform of freq. domain model
Trace	Time	RLGC	Fairly accurate for most simulations
	Freq	2D	Well known closed-form equations exist. Surface roughness not usually considered.
Connector	Time	RLGC	Simple model that may provide some crosstalk info but not effective at links >2.5Gbps.
	Freq	3D	Analyzes all pin-pin effects for accurate crosstalk and delay models. Suffers from DC interpolation issues.
Via	Time	RLGC	Very highly model dependent since return current path is not typically expressed.
	Freq	3D	Can provide very accurate results but proper modeling and port assignment needed.

Table 1 -- Tool Summary

Tool	Type	Description	Ease of Use	Accuracy	Cost
Ansoft	Mixed 2.5D, 3D	Ansoft tool suite: Designer SI Nexxsim SI Wave HFSS	HFSS – very complex	Considered very accurate when 3D is used	\$180,000
CST	3D	CST Microwave Studio	High	>99%	TBD
Mentor	IBIS with 2D & frequency solver	GigaHertz HyperLynx allows a mix of IBIS, HSPICE, and S-parameters to be used	High	Probably >90%	\$60,000
AWR	2.5D and 3D planar RF simulator with HSPICE	Microwave Office: Uses a mix of closed-form models and 2.5D EM simulation to solve transmission line problems	High	Probably >95%	TBD

Tool	Type	Description	Ease of Use	Accuracy	Cost
Cadence	IBIS with 2D & frequency solver	Similar to Mentor's tool. Fully integrated into PCB layout tool	Mid-High	Probably >90%	\$60,000 for 1 year license.
HSPICE	Time domain simulation with W-element transmission line models	Needed for any time domain analysis with encrypted HSPICE	Easy-Mid	Model dependent but can approach 100%	TBD
Agilent ADS	2.5D, 3D planar	Uses a mix of closed-form models and 2.5D EM simulation to solve transmission line problems	Mid-High	Probably >95%	TBD

Tools selected

For the Xilinx High-Speed serial backplane project, AWR's Microwave Office software with HSPICE option was ultimately chosen. This tool allowed Xilinx to quickly build frequency domain models of the channel interconnects and use 3rd party supplied s-parameter models when needed for the via and connector elements.

Using the HSPICE feature of AWR, a working interconnect model using Xilinx factory supplied HSPICE *encrypted* models of the Virtex-4 MGT drivers was created. HSPICE contains an embedded s-parameter transform function in it. Since the channel models were created as a frequency domain model along with the connector models, the transform feature was needed to examine channel performance in the time domain.

Layout Tools

Since the layout portion of channel design is as critical as the modeling, it is necessary to choose a layout tool and process that works well with backplane design and allows easy-to-use constraint features.

For the Xilinx High-Speed Serial backplane project Cadence's PCB Design CIS Studio was used. This includes both the OrCAD CIS schematic editor and Allegro PCB layout tool. The tool suite supports both forward and back annotation which allows designers the ability to apply design rules from either tool and annotate the changes to the other tool. Another nice feature supported by this tool suite is cross-probing which is very helpful for finding possible netlist issues.

With an upgraded license users can seamlessly integrate the Cadence PCB SI Explorer tool to do full channel analysis. This was not done during the High-Speed Backplane project.

Tradeoffs

The following sections introduce the most significant items which need to be considered when designing a backplane.

This section examines how the following items affect both cost and performance:

- Connector type
- Connector pinout
- Material
- Routing geometry

Connector type

Once the topology is known, a signal list between nodes and hubs can be established. The following tradeoffs work equally well on high-speed signals and low-speed signals.

Choosing a connector will define:

- Minimum slot pitch (horizontal)
- Number of pairs per inch (vertical)
- Inherent Crosstalk
- Cost/pair
- Estimated maximum signaling speed

Table 2 lists some industry accepted connectors for backplane design.

Table 2-- Typical connector parameters

Connector	Number of pairs	pairs/sq in	Min Slot Pitch	Total vias	Adv performance	Cost per mated pair	Xtalk (FEXT), freq	Notes
Amphenol xCede	24	27.5-82	25.4mm	96	20Gbps	N/A	-50dB, 5 GHz	Shown for reference only, not used Average price based Xilinx BOM Standard ATCA Zone 2 connector pair, 40 pair inch shown **Assumes Tyco-Amp high-isolation pinout per guidelines
Amphenol eHSD	30	N/A	22mm	120	10 Gbps	\$1.76	-25dB, 5GHz	
Tyco HMZd	40	20, 30, 40	25.4mm	120	6.5 Gbps	\$0.32	N/A	
2mm**	12	N/A	17mm	133	<1 Gbps	\$1.28	N/A	

N/A = not advertised

Connector pinout

There are several key points to consider when assigning pinouts to connectors:

- Row-Row crosstalk
- Signal phase
- Routing channels
- Pin-pair skew
- Pair-pair skew

Row-Row crosstalk will *always* occur so it is best to consider what the signal direction is: Tx or Rx. Tx-Tx pairing results in the far-end crosstalk at the receiver being diminished. Tx-Rx pairing causes near-end crosstalk at the receiver which increases the noise at the receiver diminishing SNR.

Pin-pair phase is important and is based mostly on routing strategy. It is highly recommended that a route study be performed before assigning final pinouts. It is very easy to induce a natural phase-error by reversing a pos-neg pin pair assignment.

Depending on how signals are distributed from slot to slot, the total number of routing channels has to be considered. Again, a route study is really needed so that a pin assignment can be made which minimizes total layers and avoids an unnecessarily high-cost backplane.

To avoid unintentional skew, keep like-signals on the same connector column pair. This is not a strict rule but a guideline.

Figure 1 below depicts each of these important points.

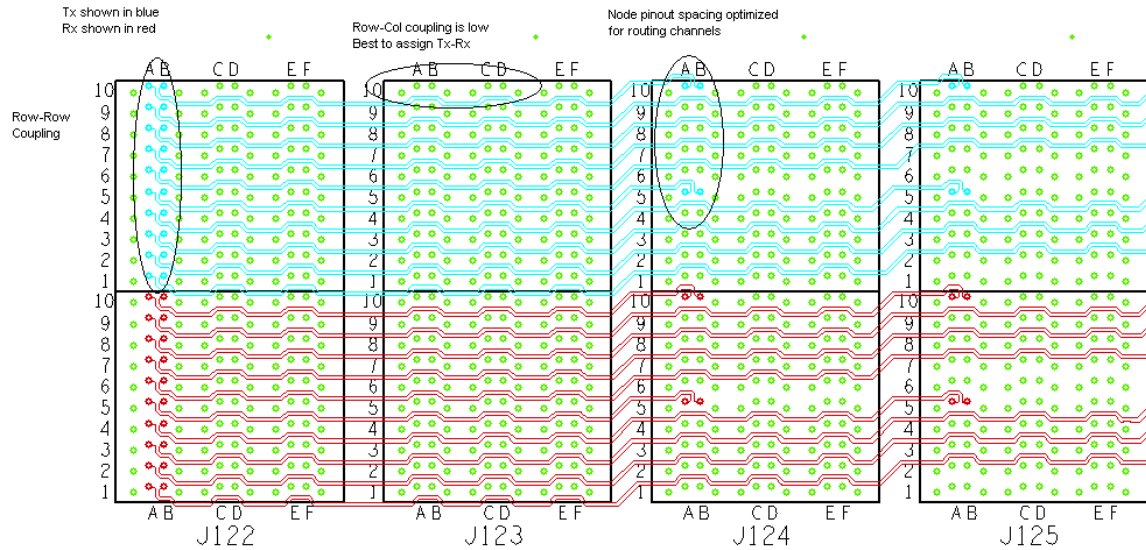


Figure 1 -- Connector pinout examined

It can be seen in Figure 1 that J122 (a hub in a dual-star network) has its Tx channels arranged in a row-row configuration to prevent its own transmit signals from talking into its own receiver. This becomes unavoidable at the junction (in J122) where the blue signals occur next to the red (Rx) signals. At the top of J123, AB and CD are circled showing the most desirable arrangement of Tx and Rx pins. This also forces a separate layer (stripline) to be used for Tx and Rx again increasing isolation. Above J124 the two Tx inputs are separated by five rows (AB10 and AB5). This was done to optimize routing channels (hub with five (5) nodes). This allows all of the other node signals to pass through this connector on their way to their node. Other combinations of Tx hub-node signals can be made to work as well but this shows one viable strategy.

Anti-pads

Anti-pads are an unavoidable consideration when designing a backplane. Most connector vendors selling connectors to operate at 3Gbps and above have already considered what anti-pads should work best with their connector. What needs to be considered is the overall thickness of the backplane and the stripline geometry.

The following diagrams look at stripline routing without anti-pad consideration and then with anti-pad consideration.

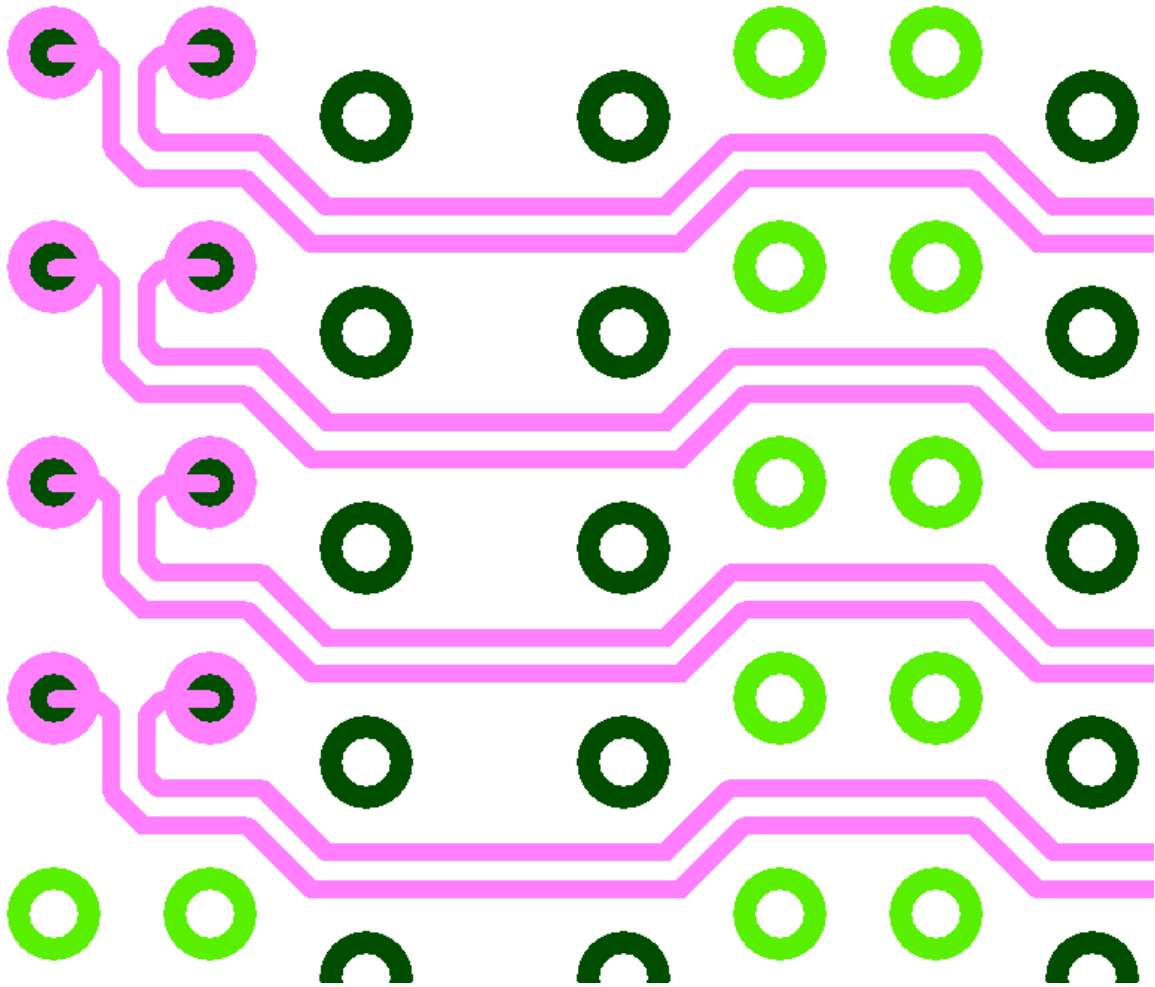


Figure 2 -- Stripline shown with no anti-pads

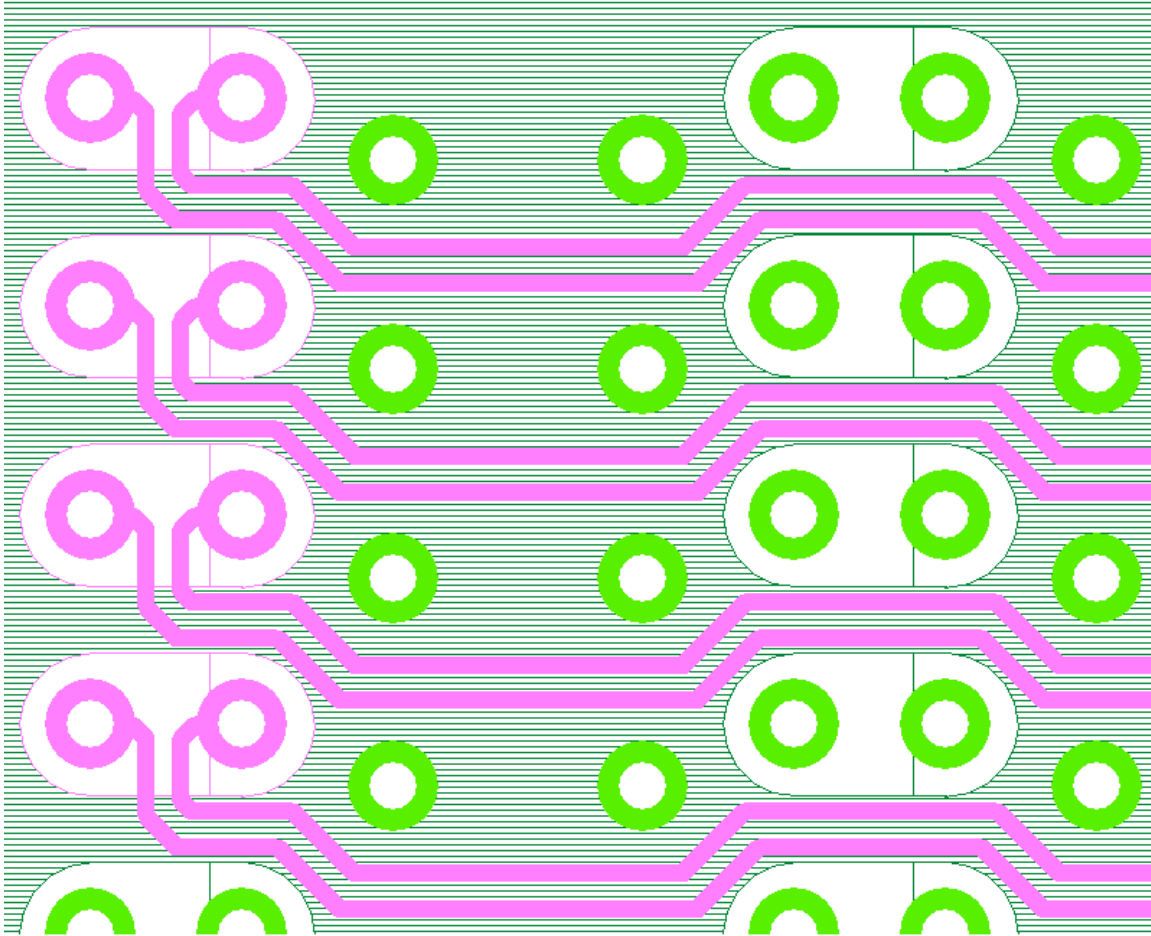


Figure 3 -- Stripline with anti-pads shown

Choosing the stripline geometry without considering the anti-pad design is bad design practice and will impact the design's performance. Be sure to examine the anti-pad sizes before deciding the stripline geometry. And do not forget that manufacturing tolerances allow mis-registration of layers up to 5 mils. This can impact the stripline impedance as one leg routes over the anti-pad opening unintentionally.

Note: If you are considering your own anti-pad design you probably have access to 3D planar electromagnetic simulation tools and can accurately predict the influence of the anti-pad. Without 3D tools, don't risk guessing your anti-pad design – work with your connector vendor and have them help you optimize their anti-pad for your application.

Material

When choosing a backplane material for your design, you should consider the following aspects:

- Cost
- Dielectric constant
- Dissipation factor
- Weave type
- Resin content

Before serial channel speeds started going above 2.5Gbps or so, most designers were not too concerned with material choice. In fact, there is a lot of press out there from the silicon vendors and connector vendors showing they have channels working FR4 at 36"! *All* of the aspects of your material must be considered before the final material choice is made.

Material choice will have a very dramatic impact to your design as it impacts:

- Producibility
- Processing cost
- Thickness
- Reliability

Table 3 lists a variety of backplane materials commonly used for backplane design. This is a partial sampling of data provided on the websites of these material vendors. The table shows how fabricators factor the cost of the finished product based on the laminate and how the laminate supplier cost factors affect the fabricator's cost. There are many more variables in the fabrication that affect the cost so be sure to study these factors with your fabricator.

Table 3 -- Relative cost of Materials

Material	Dk	Df	Weave	Resin content	Relative Cost Factor (Fab)	Relative Cost Factor (Laminate)
Nelco 4000-13SI	3.14-3.29	.008	106, 1080, 2116	53-75%	1.4	1.5
Nelco 4000-13	3.31-4.24	.009	106, 1080, 2113, 2116, 7628	38-58%	1.2	1.0
Nelco 4000-13EP	3.31-4.20	.009	106, 1080, 2113, 2116, 7628	38-68%	1.2	1.1
Nelco 4000-6	3.64-4.26	.022	106, 1080, 2113, 2116, 7628	39-69%	1.0	0.7
Isola FR408	3.65	.012	106, 1080, 2113, 1652, 7628	N/A	1.2	NA
Isola FR406	3.80	.020	106, 1080, 2113, 1652, 7628	N/A	1.0	NA
Isola 620	3.61	.008	106,1080,2113,3070, 2116,3313,1652	N/A	1.4	NA

In Table 3, one can see that by calling out a material by name is not sufficient. The material comes in a variety of glass weave types and resin contents which affect the overall dielectric constant. There is some variability in the dissipation factor but this data is not typically published by the vendors.

Picking the material is a multi-variable problem. The loss factors (Dk, Df) need to be studied to determine what amount of the link budget is assigned to backplane loss. Since overall cost is a determining factor it is not as easy as just picking the 'best' material available.

Materials chosen

For the High Speed Serial backplane project, a variety of different material types and conductor geometries were studied to examine the effects of copper width and dielectric loss. The following materials were chosen for the backplane to contrast their performance:

- Nelco 4000-13SI
- Nelco 4000-13
- Isola FR408

This is somewhat atypical for most backplanes but a hybrid combination of low-cost materials for low frequency signals and power and a high-performance (high-cost) material for selected signals is not uncommon.

Geometry

The stripline geometry chosen was based on many parameters but one dominant parameter was the anti-pad spacing between connector columns. In Figure 3 above, the anti-pads on the eHSD connector are shown and how far they encroach into the routing zone. The Xilinx backplane did not use any stripline geometries that would have protruded into the anti-pad region. By examining the physical attributes of the connector and anti-pads the maximum conductor edge-to-edge distance can be derived. The following table examines the eHSD physical dimensions:

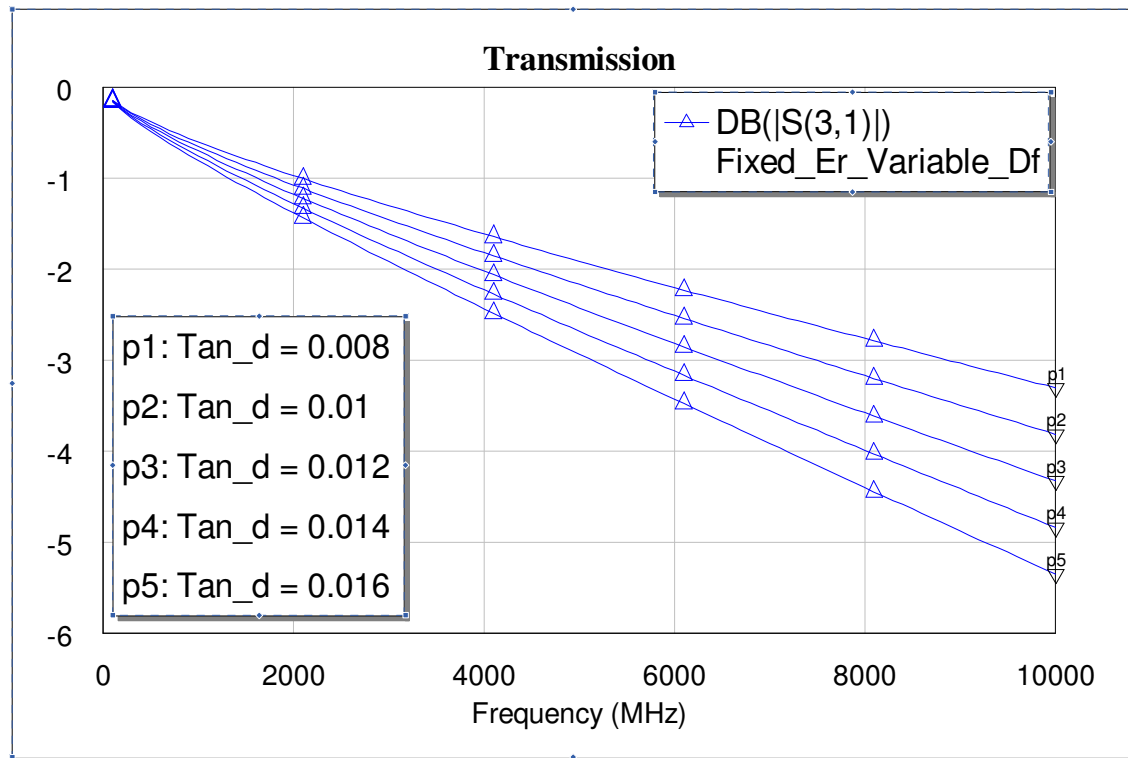
Measurement	mils
Pin-Pin column spacing	78.74
Pin Anti-pad size	54
Remaining plane copper	24.74
Mis-registration guard band	5
Final edge-edge maximum	19.74

It can be seen that only 19.74 mils +/- some tolerance remains for the stripline conductors. “Some tolerance” is noted because a 5 mil guard-band has already been applied to the numbers and if additional routing width is needed it can be borrowed from this guard band.

At this point the maximum spacing of the outside edges of the conductors is known but not how thick or wide they need to be. This is where simulation can really assist with the design.

Dielectric Loss

It is important to consider the D_f ($\tan d$) of the material when doing high-speed serial links. Figure 4 shows an arbitrary “100 ohm” differential pair (6 inch) insertion loss variation when the dielectric loss of the material is swept from 0.008 to 0.016. The figure shows that at 5GHz, the difference between $D_f=0.008$ and $D_f=0.016$ is approximately 1dB. This may not be significant enough to affect the particular link but needs to be a tradeoff against cost vs. performance.



Data from AWR Microwave Office

Figure 4 – Dielectric loss effect on stripline insertion loss

Once material choice has been made, the stripline geometry can be chosen. Differential pairs are defined as ‘loosely coupled’ or ‘tightly coupled’. It is unlikely that sufficient routing resources exist to consider loosely coupled striplines (where $Z_{odd} \approx Z_{even}$). In the current example, it is practically impossible to build differential pairs that are loosely coupled.

Thickness

At this point, a maximum distance of the outside to outside of our conductors had been determined but not the width and spacing of the conductors. Here practical limits guide us. For example, it does not make sense to call out 3 mil lines and 13 mil spacing even though that fits within our design limits.

Fabricator etching requirements play a large part of selecting a conductor width that works best. If spacing rules are set to 5 mils minimum then the largest trace width possible can be calculated along with its effects on overall plane spacing. In this the stripline edge-to-edge is $19.74\text{mils} - 5\text{mils} = 14.74\text{ mils}$. Dividing by 2 gives approximately 7 mils per conductor. If 5 mils is considered to be the minimum etch width, the variation of line widths and spacing that achieve 100 ohms and the resultant plane spacing (height) can be calculated.

Table 4 -- Example Stripline Calculations

(value in mils)		
(Er=3.38, Df=0.008), 1oz Cu		
Width	Spacing	Height between planes
5	5	25
6	5	38
7	5	100*
7	6	30
5	6	18
5	7	15.6
5	8	14.6
5	9	14

*limit in simulation reached

If each of the geometries in Table 4 results in 100 ohm differential pairs, then how does one choose? There is not one answer to this. However when the overall backplane thickness limits is considered, there will only be one or two of the practical combinations. If the overall backplane thickness can still not be achieved then the following choices need to be reconsidered:

- Changing conductor thickness
- Changing dielectric material
- Changing backplane thickness limits

- Choosing a connector with different geometries to allow more spacing for routes

The material chosen will decide one of the variables in the next decision point: thickness. The overall thickness will be affected by the kinds of glass weaves chosen. It is wise to include a ‘fill’ layer in the stackup to adjust the overall thickness of the backplane so that the stripline geometry is not inadvertently affected.

Laminate Skew

An effect known as ‘laminate weave skew’ or some sinister sounding skew effect is showing up in literature. Xilinx did examine this effect and in fact the problem does exist and there is no *certain* fix to the problem right now. Check the current literature to see if this problem is being resolved. First, what is the effect? Read on if you are not familiar; otherwise skip to the next section.

The laminate skew effect is an effect that can be measured where one leg of a differential pair has a different propagation velocity than the other pair. This results in signal eye-closure ultimately when hit by the effect. Measurements are widely ranging but it is not atypical to see 1.5-2.5ps per inch of skew. Over 20 inches, this can easily add up to 50ps of skew. For a given link, this amount of laminate skew can impact link performance.

To help minimize the effect, the glass weave chosen vs. the copper conductor width and spacing seems to have the greatest effect. In simple terms, what is happening is that one leg is falling into a ‘valley’ where the fiberglass strands are separated. This area tends to be resin-rich and has an effective Dk lower than the glass-rich areas.

There are several *patented* approaches to fixing the problem. The reader is encouraged to investigate the patents applied to the mitigation of laminate skew. Several fabricators are releasing new fabric weaves to help mitigate this issue as well.

Back-drilling

By now most engineers have heard of back-drilling. It is a post-fabrication step where the rear of backplane vias are drilled to a controlled depth to minimize the remaining stub. Figure 5 shows a pictorial view of back-drilling that was used on the Xilinx High-Speed serial backplane project.

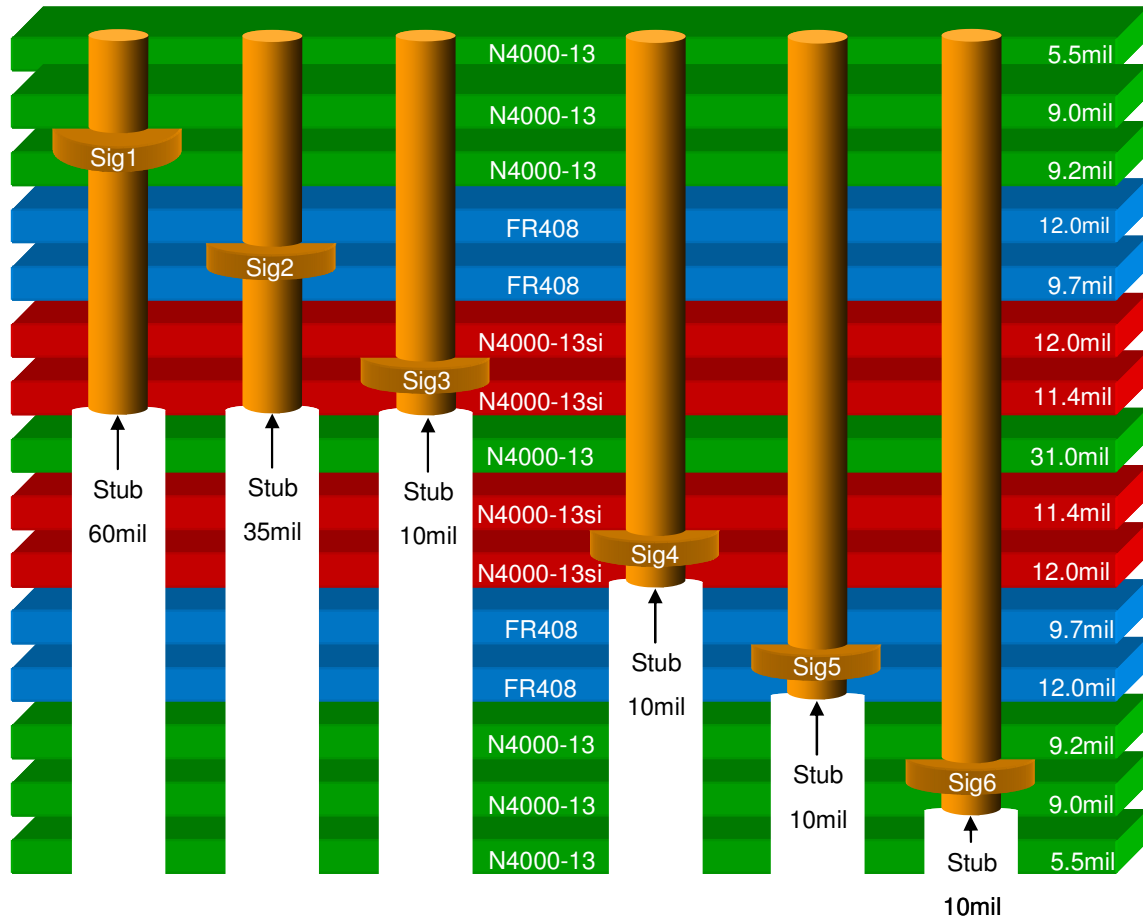


Figure 5 -- Back-drilling example

Upon examination of Figure 5 it can be seen that Sig1 and Sig2 have longer stubs than the other layers. This is because the pins used in backplanes are called “compliant” pins and need a minimum z-axis depth for proper functionality. Check with your backplane connector vendor to see how far the vias can be backdrilled and still function with the connector.

The need for back-drilling really depends on the application – it is not as simple as stating a particular frequency needs backdrilling. In the above figure, it is obvious that Sig6 would have a shorter stub naturally than Sig3 without back-drilling. 60 mil stubs can have resonant effects above 5GHz which is the first harmonic of 10Gbps links or the second harmonic of 5Gbps links. Back-drilling is *not* an absolute requirement even for these link speeds but with other effects being consider most companies are quick to jump on back-drilling before a full analysis has been performed to determine the system benefit. It is *highly* recommended that simulations using quality microwave tools be used to make decisions before checking the “back-drill” check-box on the fab drawing.

Hybrid Constructions

Another consideration for backplane design is to reserve only a few layers for high-speed low-loss routing. There is no need to specify higher-cost materials such as Rogers 4350, Isola 620 or Nelco 4000-13SI when FR406 would work.

An example of a hybrid backplane stackup is shown in Figure 6 below. Here the low-loss signal layers (Signal Layer 3, Signal Layer 4) using Nelco 4000-13SI have been placed in the middle of the backplane. Other lower cost materials can be utilized on remaining layers to reduce cost.

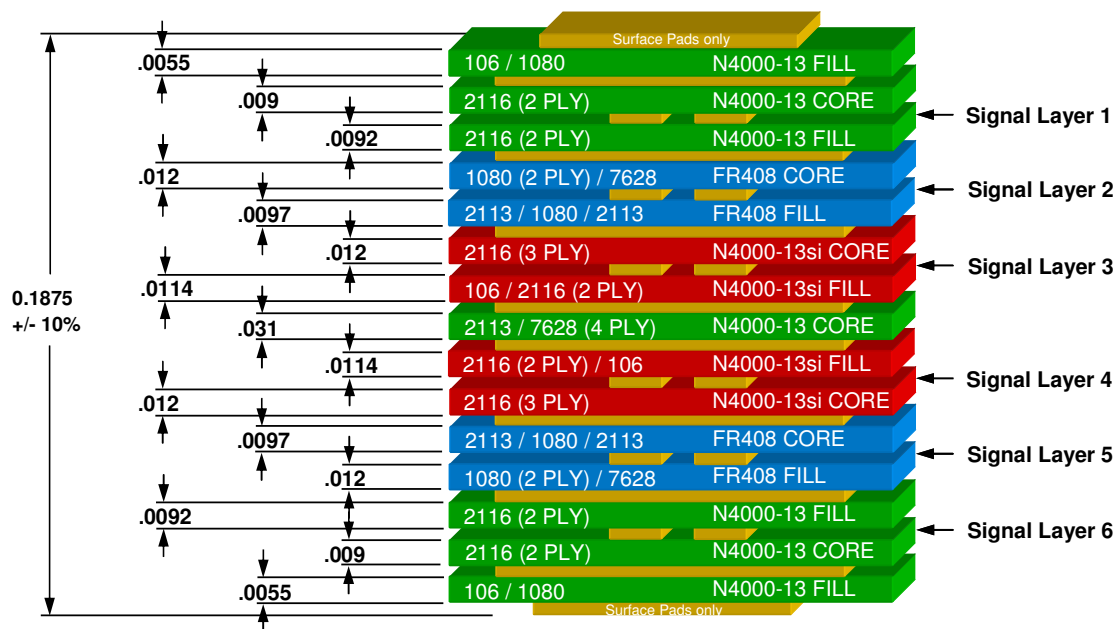


Figure 6-- Example Hybrid construction

Edge plating and ground via stitching

There are several techniques to mitigate EMI caused by energy generated by power plane resonances and signals routed close to the edge of the backplane.

Edge plating is not necessarily expensive. Be sure to check with your fabricator on the cost implementing edge plating. If your fabricator has little experience in edge plating you will find this a costly venture and perhaps ground stitching is a better alternative.

Ground stitching as defined here implies the use vias placed around the perimeter of the backplane which connect *all* of the internal ground planes together. The spacing between the vias helps define the attenuation frequency. A field-solver is typically required for final

determination but in practice randomly placing vias between 50 and 100 mils apart along the edge works for backplane designs.

Some things to consider before applying either one of these techniques is whether or not you have ground planes extending to the edge of the backplane and will the edge plating or vias contact the metal structure of the backplane unintentionally.

Routing Skew

Here routing skew is defined as intra-pair skew and inter-pair skew. Intra-pair skew is defined as the *route difference* between the copper trace for the positive leg and the negative leg. Inter-pair skew is defined as the route difference between one pair and another.

It is tempting to over-constrain a design and request that the skew between P & N legs be zero or skew between pairs be zero. This is both unnecessary and costly.

What *is* important is to make an interconnect budget and determine the maximum allowable skew for overall interconnect. Be sure to think about the laminate skew effects as well if your design is operating above 5Gbps.

Smart Thinking

There is significant literature presenting routing methods to equalize skew. Smart thinking is your best friend when thinking about minimizing skew. Next two interconnect routes are examined and the result of good up-front planning prevents additional wasteful routing methods to equalize skew.

In the following figure there are two node slots that have four (4) pair interconnecting the two slots. The goal was route the four pair as 6" matched pair.

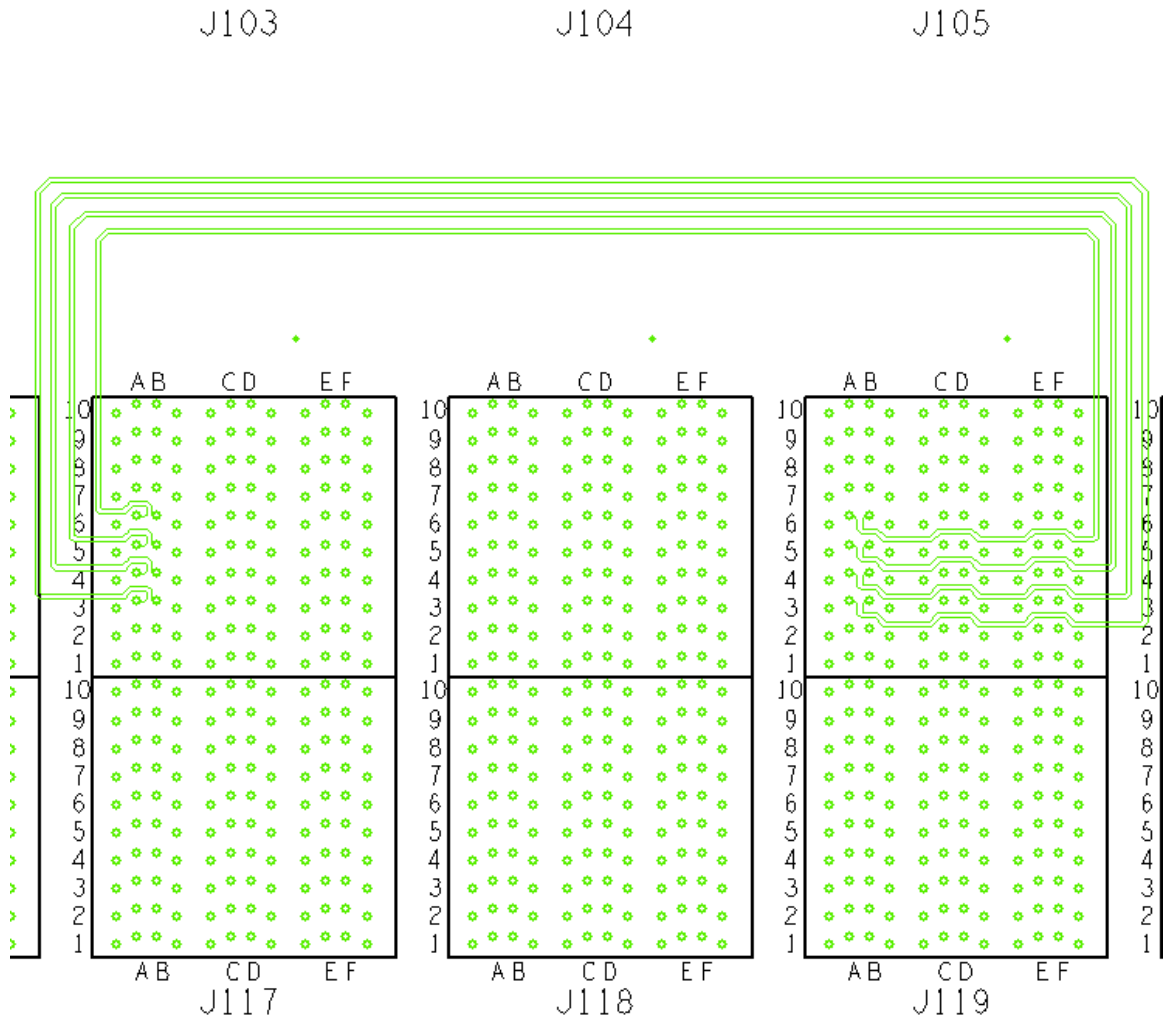


Figure 7 -- Point-to-point routing with inherent skew

Table 5-- Route lengths and skew

Route	Pos (mils)	Neg (mils)	Diff (mils)
J117 AB7	5437	5347	90
J117 AB6	5912	5822	90
J117 AB5	6375	6285	90
J117 AB4	6707	6797	90

Although at first glance the routes *appear* to be following the same path there are some inherent problems with these routes. This is where advice in existing literature recommends serpentine and corner-jogging to correct the problem. Table 5 shows the resulting path lengths of each of the four routes above.

Next the *same* routes with simply a direction change and right-turn/left-turn balancing are examined.

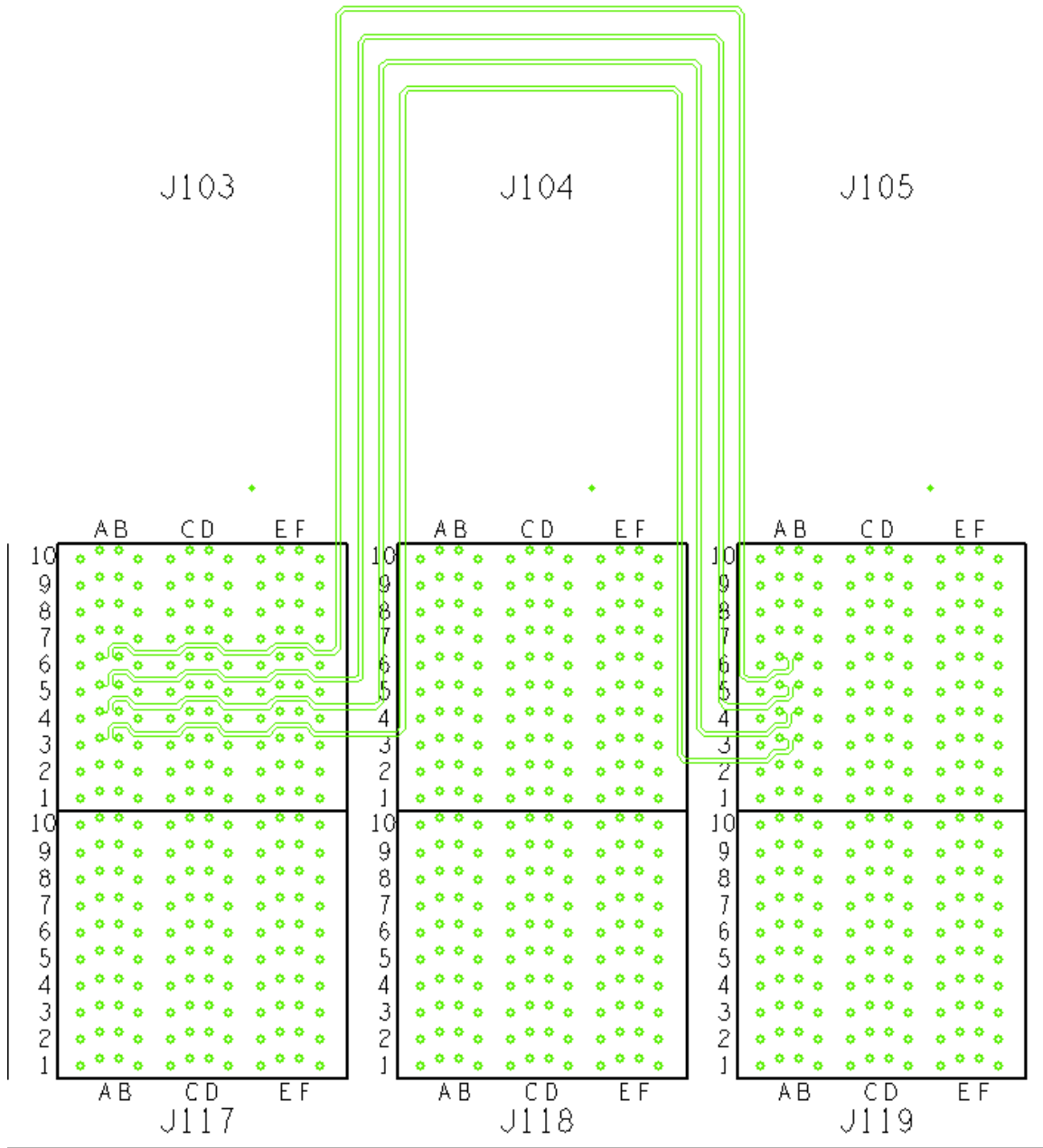


Figure 8 -- Point-to-point routing with inherent matching

Table 6 -- Route lengths and skew matched

Route	Pos (mils)	Neg (mils)	Diff (mils)
J117 AB7	5998	5998	0
J117 AB6	6000	6002	2
J117 AB5	6000	6002	2
J117 AB4	6000	6000	0

Now the goal of minimizing intra-pair skew *and* inter-pair skew has been accomplished by a simple change in routing approach. If you examine Figure 8 it can be seen that for every left turn there is a right turn and the pairs that are naturally pinned top to bottom are routed top to bottom.

Think about *how* to smartly route before wasting a lot of time with a bad plan.

Potential traps

- Line card material is different from backplane
- Backplane Signal layers use different material
- Z-axis skew
- Connector skew
- Laminate Weave effect

When doing a link budget don't forget that different materials and even different material *thicknesses* can cause velocity differences that result in skew. Be sure to check with your fabricator to find out if *they* have measured the *exact* combination of laminates prescribed and cross-check their data with the laminate supplier. Xilinx has found that the techniques used to measure Er vary from vendor to vendor and particular expectations may not be met upon delivery.

Another oversight is the z-axis distance the signal must travel down the via when entering and exiting a connector. An upper layer can be 15ps away from a lower layer which introduces 30ps inter-pair skew without much thought. And within the connector there *will be* intra-pair skew and additionally if one pair is routed on AB and another on pair CD, for example, there will be inter-pair skew because of the physical pin lengths inside the connector.

It must be repeated that you caution needs to be exercised if the link budget does not include

both intra-pair and inter-pair skew because of laminate weave related issues. Do not worry about how well the layout team matches pairs to 5 mils (800 femtoseconds) and then ignore laminate skew -- the design is destined to fail.

Things to think about

- Voltages
- Creepage/clearance
- UL requirements
- Return currents
- Soldermasks
- Silkscreens
- Mixing connector families
- Guide pins
- Mechanical holes
- Grounding
- Test and Measurement

The bulleted list above is a partial list of items that must be considered when designing a backplane. This document can not begin to touch on the importance of these items. Everything in the design interacts with everything else! Plan accordingly. Read the specifications. If the budget allows, build some test vehicles to experiment with laminates, vias, anti-pads, back-drilling, etc...

Lastly, be *sure* to plan for some test methodology for your backplane. Is a specialized test card needed to validate the design? What about snooping backplane signals in a working system? Be sure to budget for this and the *time* it will take to thoroughly test the backplane so your system will be a success.

Contacting your PCB fabricator

It can not be over-stated that you *must* develop a relationship with a trusted PCB fabricator *before* starting routing. Your fabricator needs to review your proposed stackup and confirm that they can build your backplane with the chosen materials and geometries. Too often this author has seen where hundreds of differential pairs had to be re-routed at the last minute when the gerbers arrived at the fabricator and they could not build to the specified impedances.

Simulations and Measurements

With any simulation the quality of the results depends on the quality of the models and the realism of the circuit being simulated. It is not for example atypical to ignore parasitics in a simple circuit model to make a simulation go faster. Inserting a simplified model of a component for simulation because a real model is not available or might take too long to simulate is not uncommon.

In a backplane channel simulation you need to determine what level of accuracy is needed to have confidence that your channel will be usable at the data rates and with the data patterns being sent. And after simulation comes measurement. It is imperative to have a measurement and validation of the final backplane.

Looking ahead to Measurements

Measurement and validation of backplane performance is a final proof of the design. Some measurement techniques to consider are:

VNA	4-port	Limited cross-talk measurements. Needs rigidly fixed SMA attachment.
VNA	12-port	Improved channel cross-talk measurements. Needs rigidly fixed SMA attachment.
TDR TDR	One diff head	Can be used with hand-held differential probe but typically needs rigid SMA attachment.
TDR TDR	Two diff Head	Offers single-ended, differential, and reciprocal measurements. Used with post-processing software this data can be transformed to s-parameters.
Oscope		Limited bandwidth. Very useful for 'looking' at eye patterns generated across channel. Can monitor live system

Depending on available test equipment a method for measurement of the backplane channel needs to be considered. This may include a passive test card which can be plugged into the backplane and provide SMA connections to the test equipment.

Simulation Models

As stated earlier Xilinx chose to use AWR's Microwave Office software with HSPICE option. *Good* s-parameter models of the backplane connectors and mounting vias were needed to accurately simulate the various channels. Accurate stripline models of the interconnects were done using Microwave Office. It was quickly found that the accuracy of the connector models quickly dominated the results of the channel interconnect.

For this product development, connector vendors were asked to supply accurate models of their connectors. The importance of this can not be understated if you do not have the ability to simulate your connectors with 3D EM simulation. Developing a good working relationship with your connector vendor is vital to the success of your project. Make sure they are committed to helping you get good simulation results.

Simulating the channel

The approach taken for simulating the channel was to generate each of the building blocks that made up our system interconnect model, simulate and verify each model independently, cascade the building blocks together and then simulate the complete interconnect. Whenever a vendor supplied model was used it was cross-checked with the simulation results from the vendor to make sure the models were in agreement with the results before proceeding.

After cascading the blocks together, AWR was used to perform frequency domain analysis of the channel insertion loss (Sdd21) and crosstalk (Sdd13, Sdd23). Since the channels were symmetrical, the channel was naturally reciprocal (Sdd21=Sdd12) and likewise for the NEXT and FEXT signals.

When the entire channel model has been constructed, the channel performance can be verified against any specification requirements if the specification includes limits for crosstalk and insertion-loss across frequency. The IEEE 802.3ap specification is one such specification that provides frequency based channel requirements.

AWR can generate a PRBS pulse-train and simulate it natively using a harmonic balance approach. The results can be displayed in an eye-diagram format which tends to be the metric that most people use for determining overall channel performance.

Lastly, the full system interconnect from MGT transmitter to MGT receiver was simulated in HSPICE. Xilinx provides HSPICE design kits for customers which can be used in AWR.

With the HSPICE models the amount of pre-emphasis and receiver equalization can be varied and channel response “seen” in near real-time.

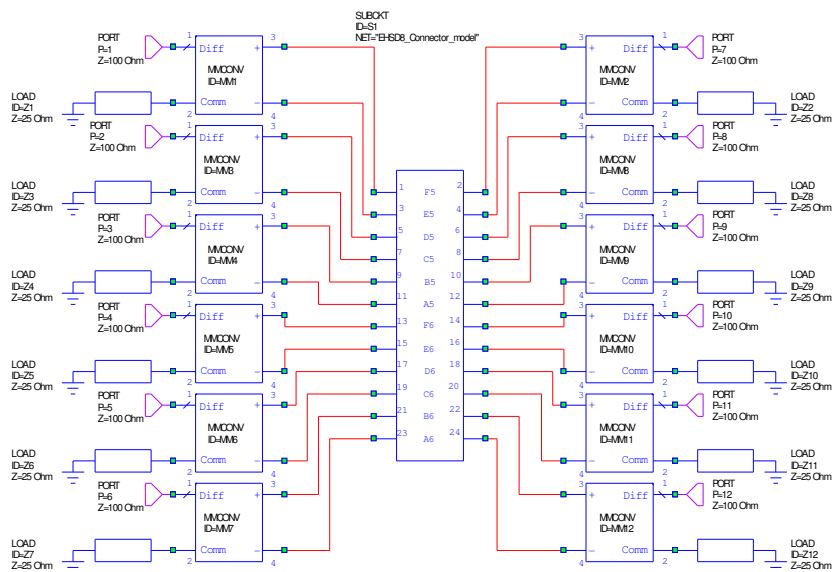
A look at simulations

As stated earlier, each piece of the backplane channel was simulated and analyzed before cascading that piece with other pieces of the backplane. This way any setup or model data problems could be identified before attempting to churn out an entire channel.

Here in Figure 9 the eHSD connector verification circuit model is shown. Using AWR’s element library the stimulus was converted to differential mode stimulus since the connector was being stimulated with differentially driven outputs. In the center of the figure is a black-box which contains the s-parameter data supplied by Amphenol-TCS for their eHSD connector.

Next the frequency is swept from approximately 0Hz to 20GHz to view the Sdd differential transmission of each of the signal pairs in the connector. The resultant sweep is shown in Figure 10. By examining this graph it can be seen that the pairs are well matched out to 15GHz which should be well beyond the backplane channel needs. Above 15GHz one can begin to see some irregularities and resonances which may be measurement induced or real. Most of this will disappear once the backplane vias are connected to the channel.

Figure 9 -- eHSD connector simulation



Schematic from AWR Microwave Office

Figure 10 -- eHSD connector Sdd transmission

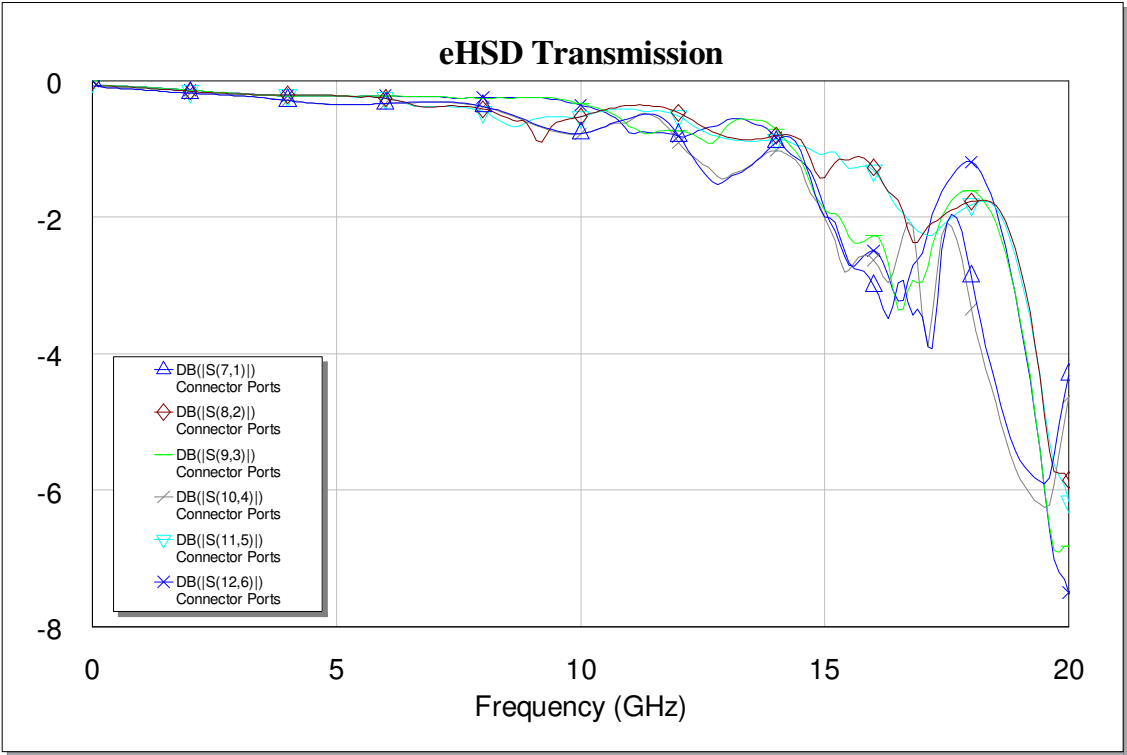
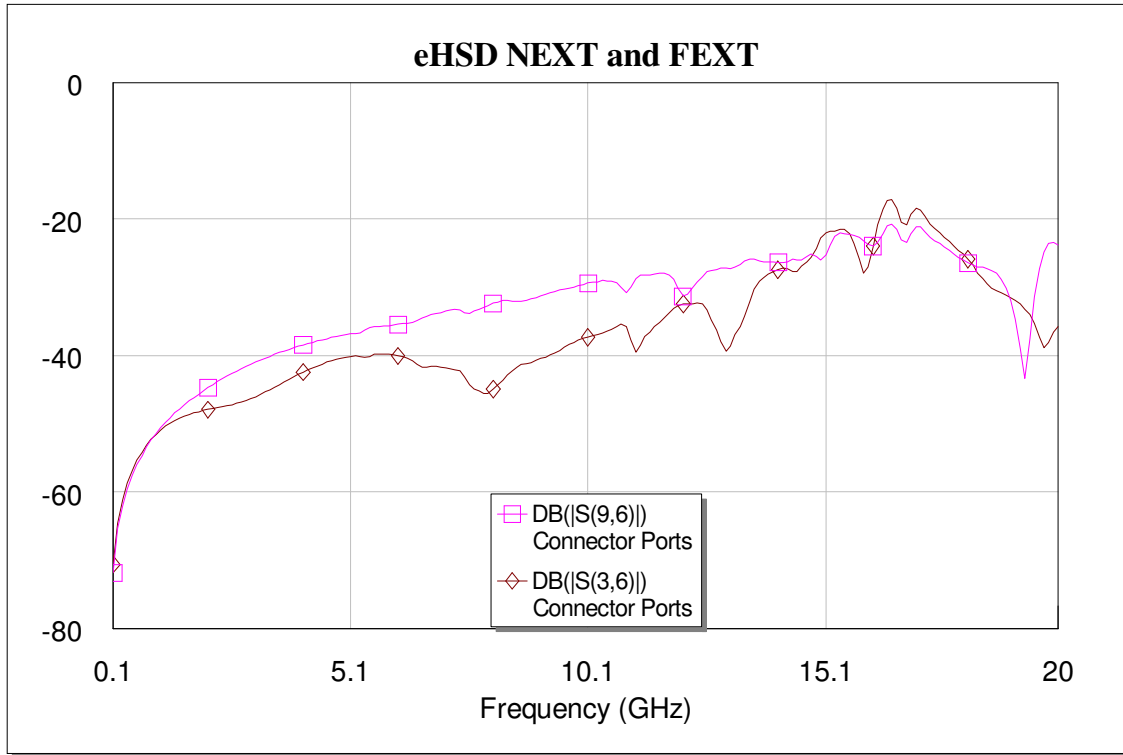


Figure 11 -- eHSD connector crosstalk



Exploring further near-end crosstalk (NEXT) and far-end crosstalk (FEXT) generated by the connector are examined. The example shown in Figure 11 shows that the arrangement of pins as Tx and Rx later on will matter as signals that transit the connector in a column-to-column arrangement will crosstalk *through* the connector. This coupled with backplane via coupling may degrade performance.

Stripline Simulations

Next this paper examines a simple equation-based stripline formula versus a closed-form model of a differential pair that is an element in the AWR library. Recall that stripline impedance is a function of frequency and its characteristic impedance can be estimated by the following formula:

$$\sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

where R is the ac+dc resistance of the etch, G represents the dielectric loss ($\tan_d$ or

dissipation factor), and L and C are the unit length inductance and capacitance of the line for a 50 ohm line surrounded by a homegenous dielectric (ϵ_r). Once the loss per unit length was computed, the linear loss factor was computed by multiplying the expected trace length by the unit loss. This was done at each of the frequency harmonics (1x, 3x, 5x, 7x).

Using AWR's data import feature, results from an Excel spreadsheet calculation of the stripline performance were plotted on the graph shown in Figure 12 along with a frequency sweep of the AWR closed-form model. The equation based model results and closed-form model results agree with some expected error since they are not identical models. This simulation gives confidence to the AWR model for going ahead with a cascaded system model.

Reference Channel Simulation

The first cascaded system model represents a 20" differential stripline and SMA connectors. This line was constructed and measured on the High Speed Serial Backplane project so the stripline performance could be verified over a range of materials. Once the backplane was actually measured it became obvious that the model for the SMA connector was too simplistic. Using the tuning feature in AWR, the values of inductors and capacitors were tuned to get close matching of the SMA performance in the time domain. Next the interconnect was swept in the frequency domain plotted against the measured s-parameter data from the VNA. The results are shown in Figure 14.

Figure 12 -- Comparing Equation based Stripline to AWR Model

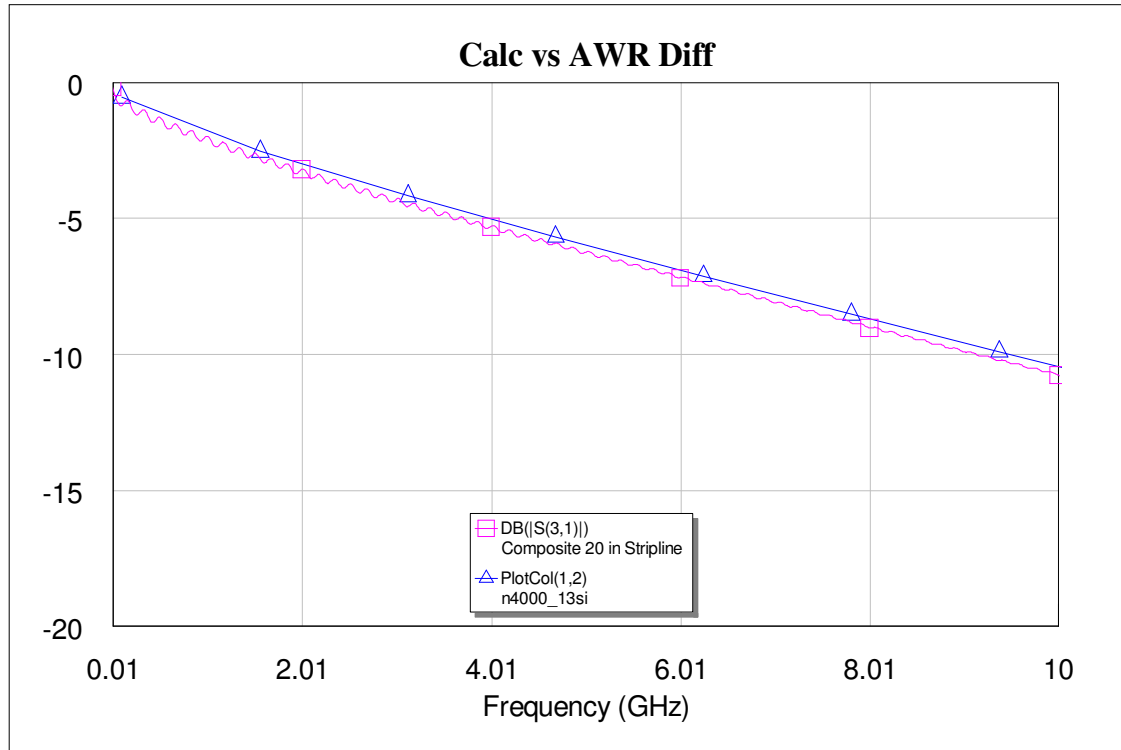


Figure 13 -- Cascaded reference channel model

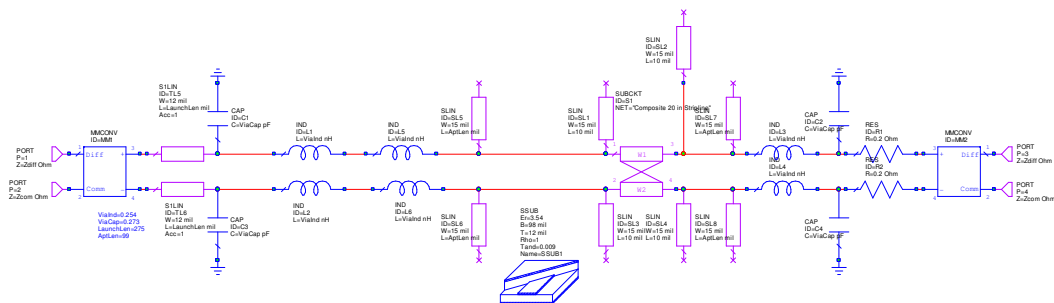
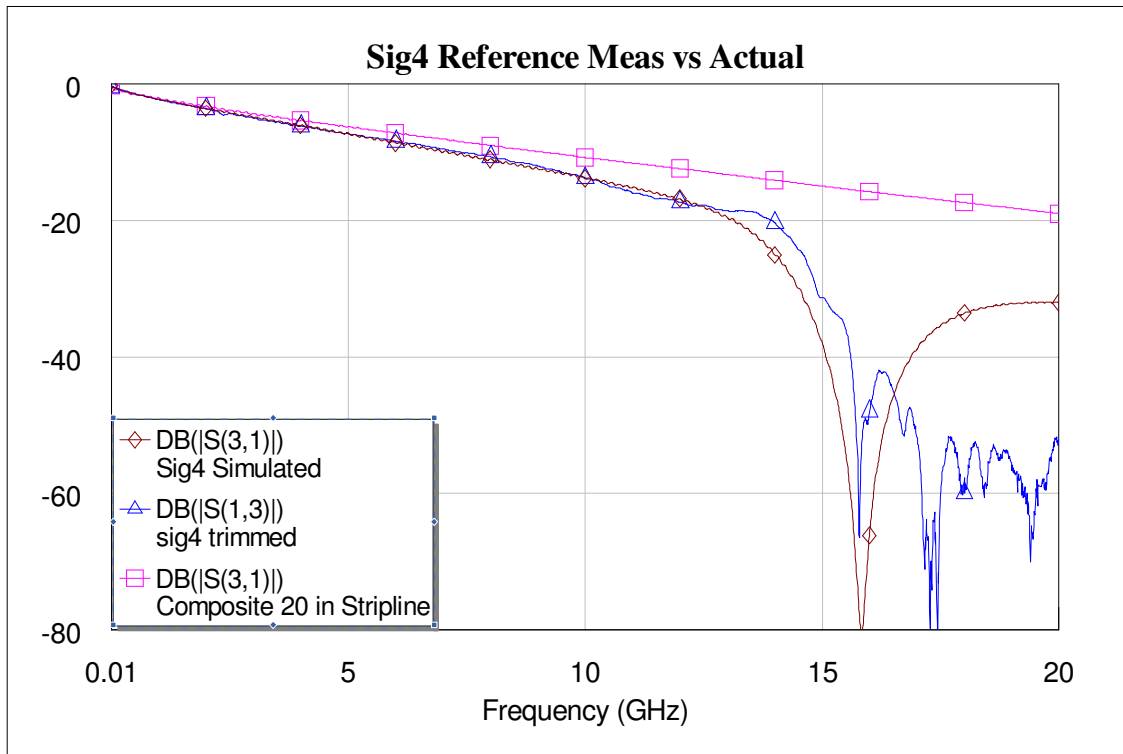


Figure 14 -- Reference channel simulation vs. measured



In the above graph, the differential stripline without connectors is shown in pink. This shows the best-case channel performance. The remaining two graphs compare the measured data against the predicted channel performance. Above 16 GHz the reference model does not match since the model is too simple. In this case it was decided the modeled performance was acceptable since contribution above 15GHz are not significant.

Next the harmonic balance feature of AWR was used to generate PRBS signaling across the channel (with SMAs). The results of the channel eye using this simple (but fast) approach to channel modeling can be seen. The channel was measured using a Xilinx ML-421 MGT test board to generate the source signal while driving through the channel and into an Agilent oscilloscope. The measured eye is shown in Figure 16.

Figure 15 -- Eye diagram of reference channel

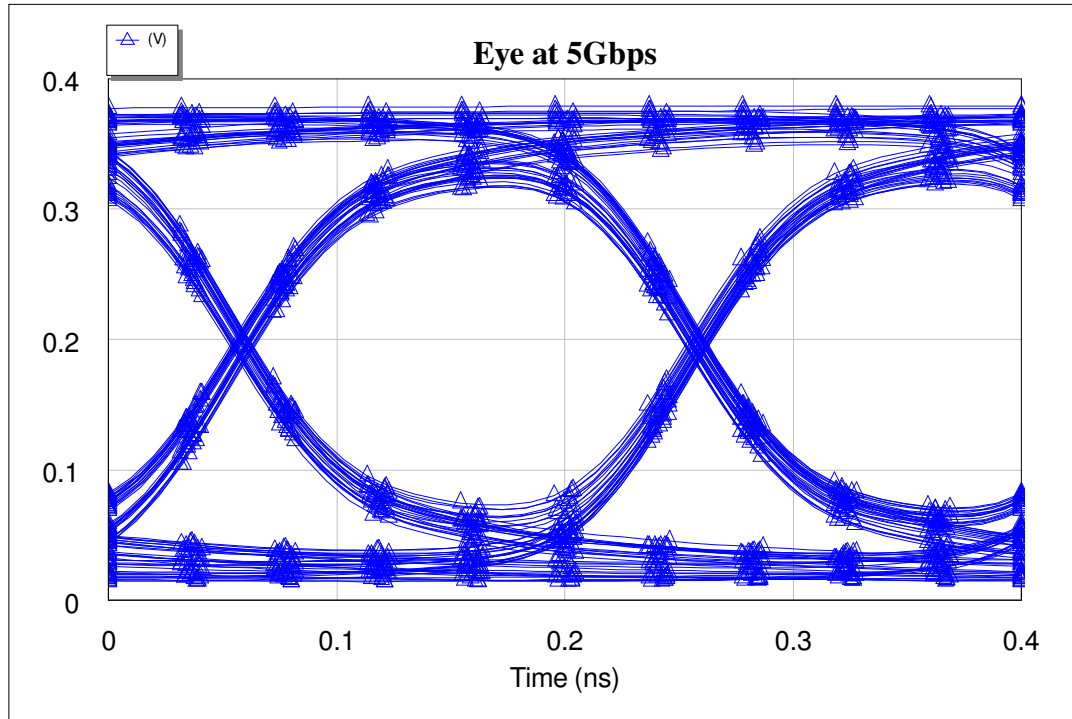
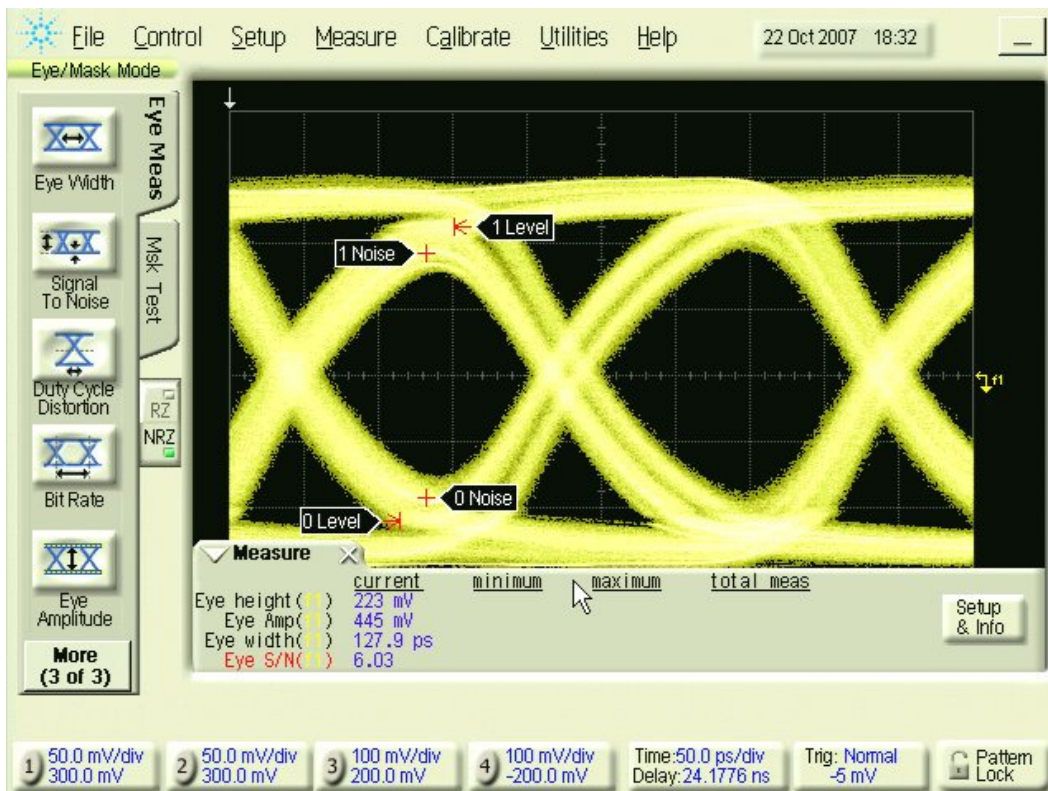


Figure 16 -- Measured eye on reference channel



Channel Simulation

Finally a complete system interconnect model was built that included SMA connectors, 8” of daughtercard trace, backplane connectors and vias, and backplane trace. That complete model is shown below in Figure 17. The connector and via models were imported and a wrapper was placed around the s-parameter file. At this point, frequency, harmonic balance, export to HSPICE, or transform to time domain could be done.

A frequency sweep of the channel simulation vs. measured is shown in Figure 18. Next the harmonic balance simulation is compared against the measured channel eye. Data rates of 3.125Gbps, 5 Gbps, and 6.5Gbps are shown in the following figures.

Figure 17 -- Backplane interconnect circuit model

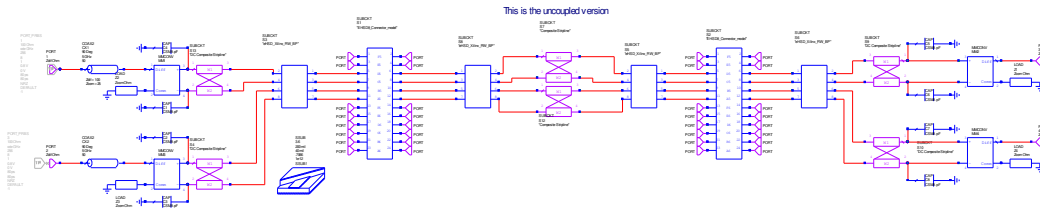


Figure 18 -- Complete Backplane channel model with eHSD

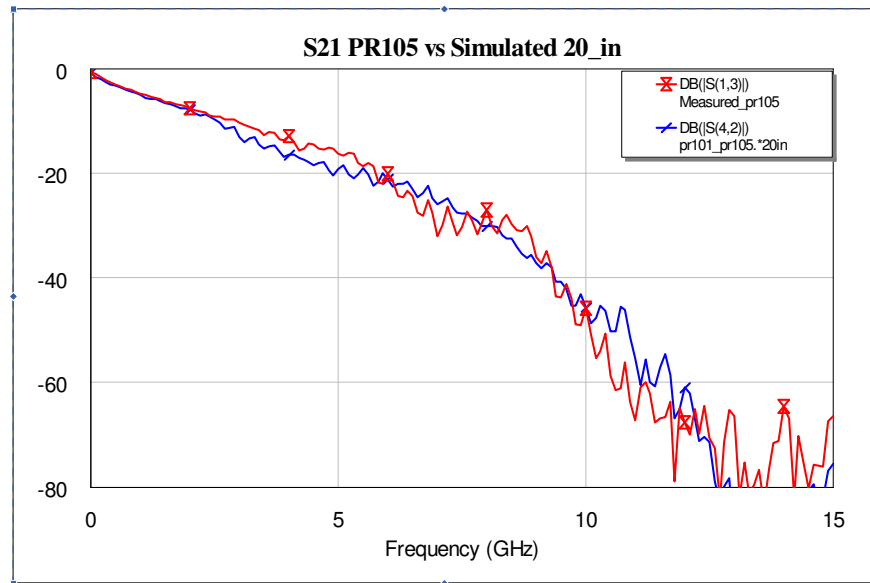


Figure 19 -- Harmonic Balance simulation of AWR model at 3.125Gbps

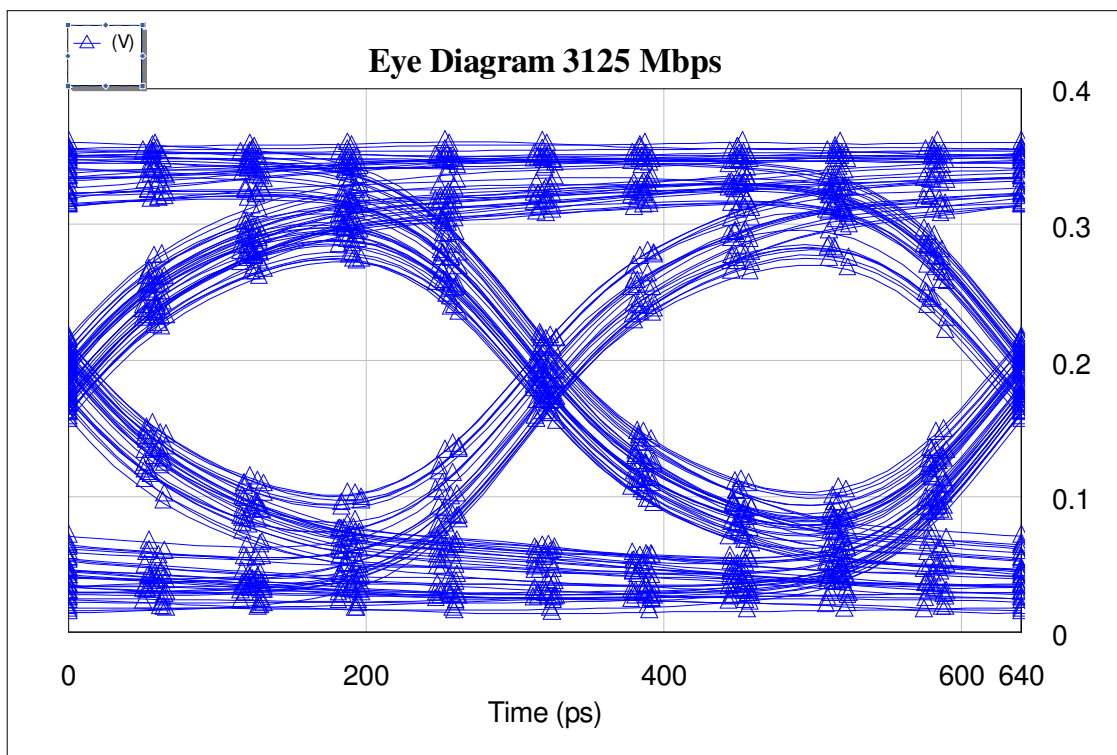


Figure 20 -- Harmonic Balance of measured channel performance

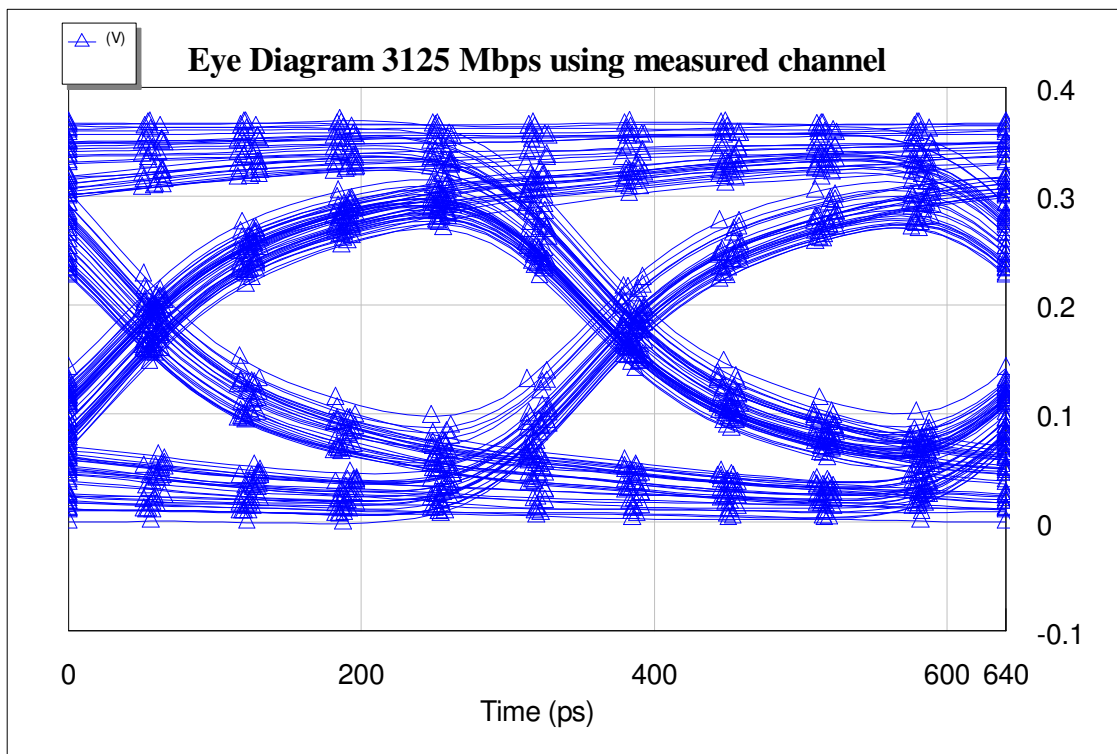


Figure 21 -- Harmonic Balance simulation of AWR model at 5 Gbps

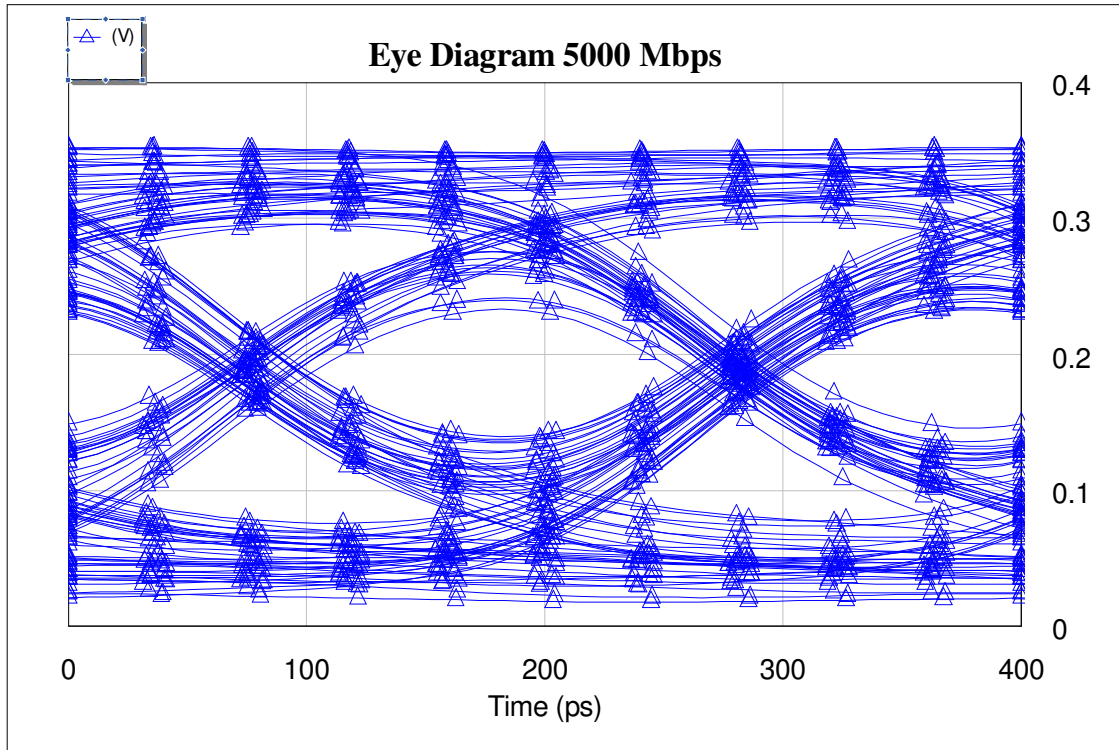


Figure 22 -- Harmonic Balance of measured channel performance at 5Gbps

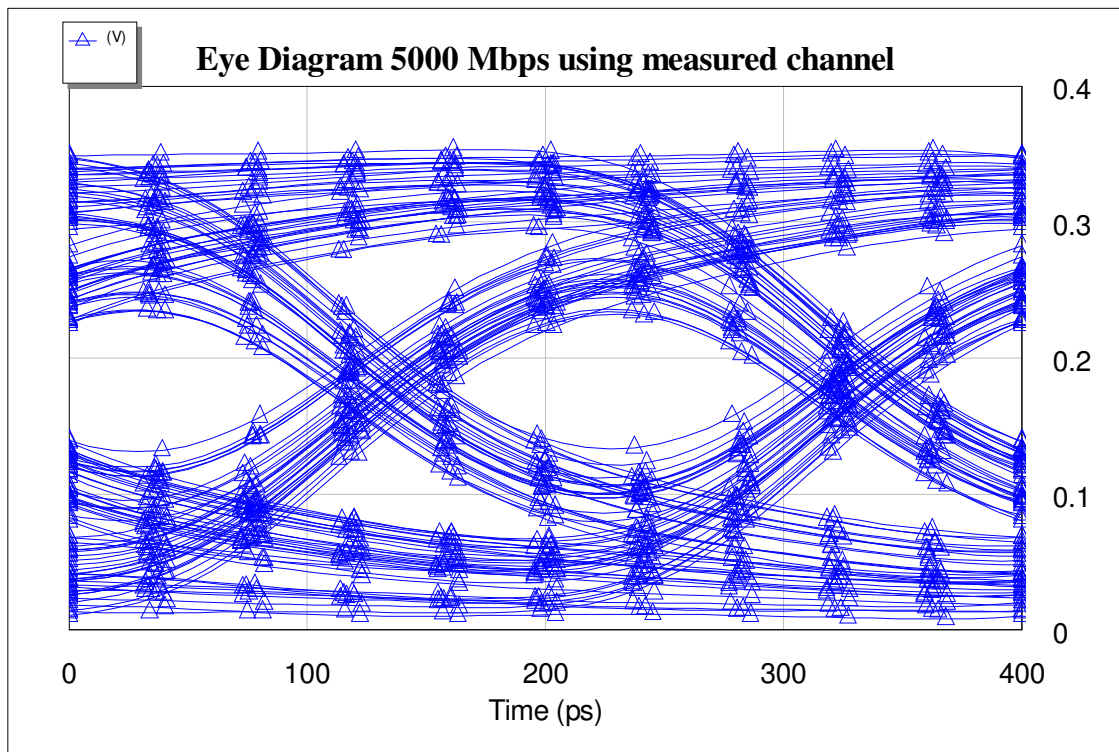


Figure 23-- Harmonic Balance simulation of AWR model at 6.5 Gbps

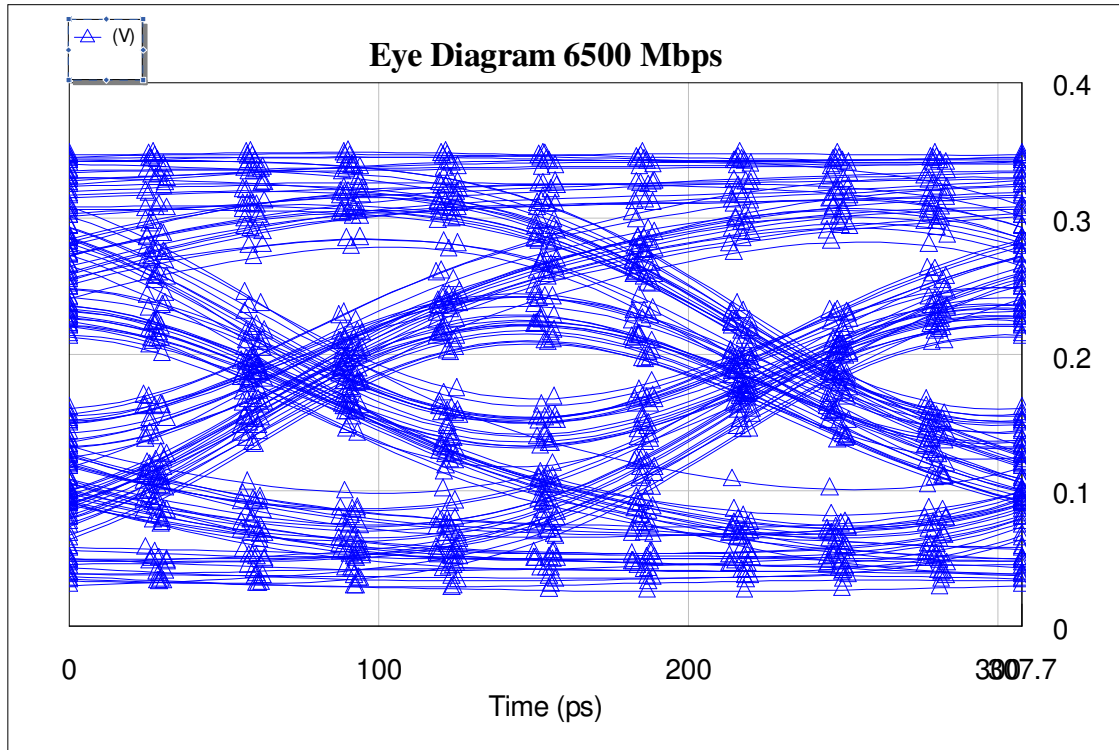
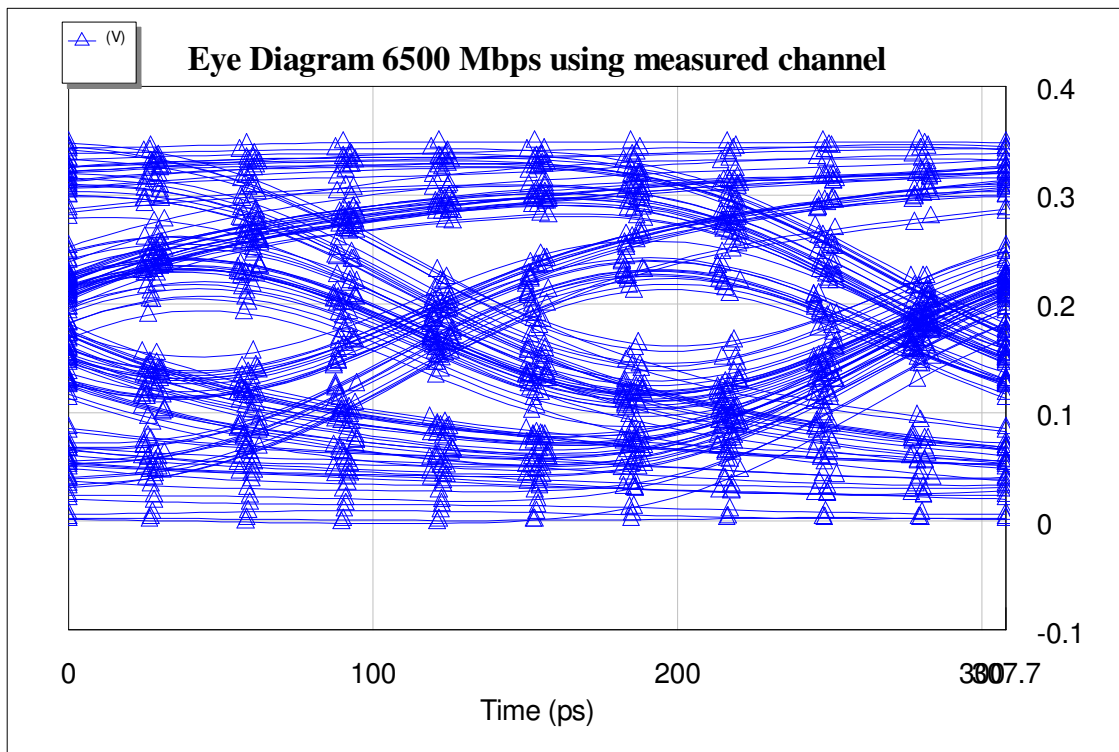


Figure 24 -- Harmonic Balance of measured channel performance



HSPICE Simulations

The last phase of simulation was to incorporate HSPICE MGT models of the V4 transmitter and receiver into the backplane simulation. Here the entire channel shown in Figure 17 is inserted between the transmitter and receiver. The circuit model of MGT simulation is shown in Figure 25.

Analyzing the circuit in the time domain gives the ability to monitor all of the nodes in the MGT Tx-Rx path that are not normally visible in a running system. This allows the designer to fine tune the pre-emphasis and receiver equalization *before* getting into the lab. The accuracy of the backplane channel model will affect the HSPICE simulation but a very tight correlation between our simulated channel and measured channel has been shown.

Figure 25 -- HSPICE Circuit model of V4 MGT

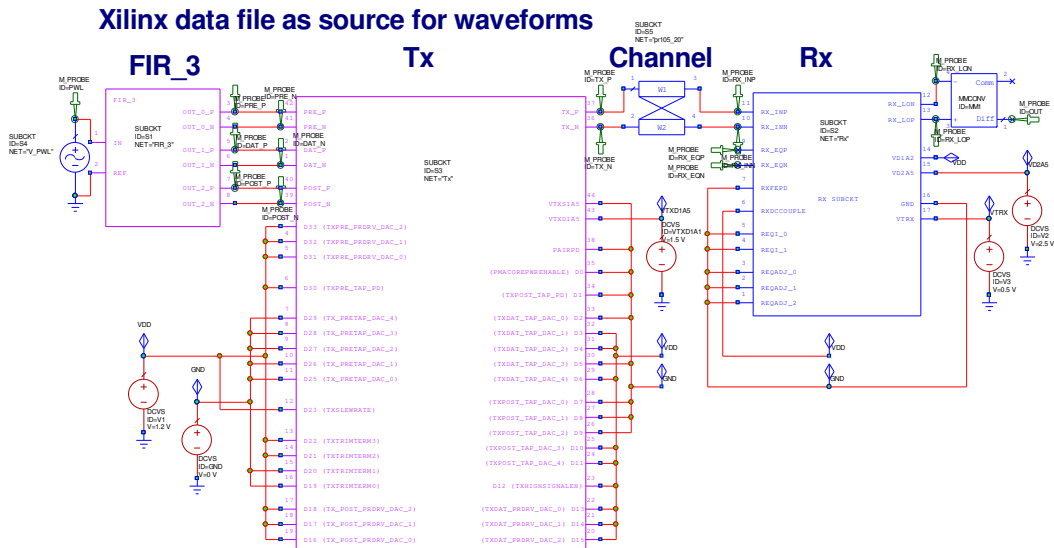
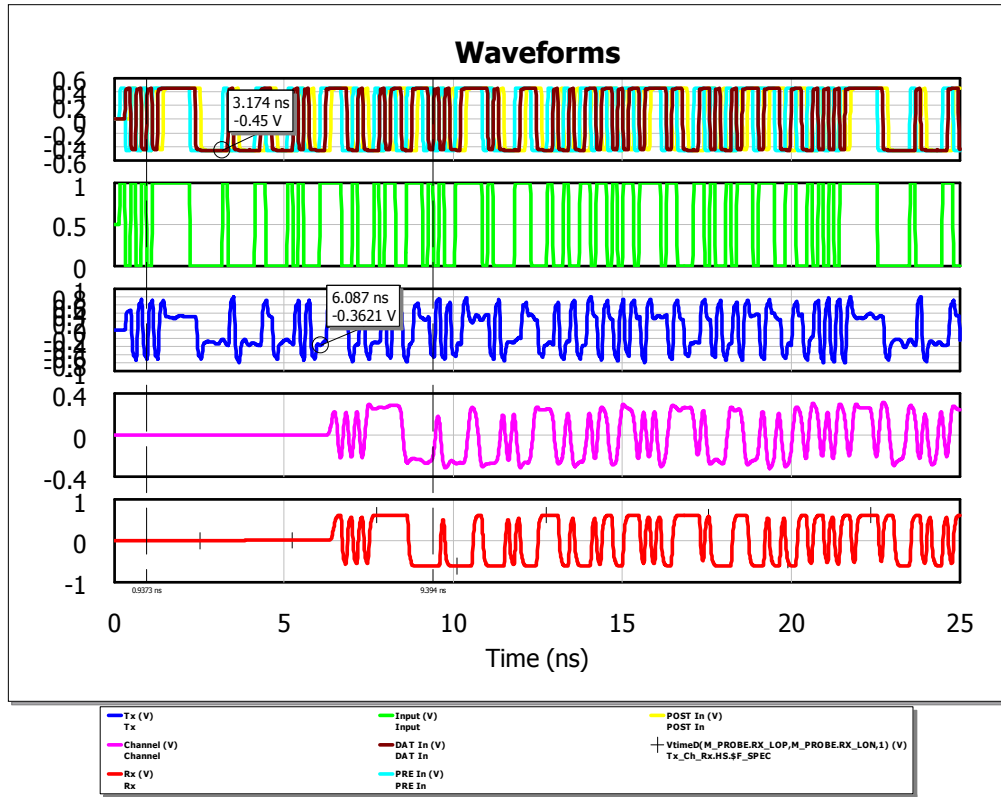


Figure 26 -- HSPICE node measurements



In the above simulation the source is a pulse train defined by Xilinx for the channel. This source is replaced with a PRBS generator next to examine the channel eye. Figure 28 shows the resultant eye diagram. Here eye closure can be seen which indicates a change to pre-emphasis might be needed. This eye is measured *before* the receiver. Additional receiver equalization can and is applied which results in a working channel.

Figure 27 -- PRBS pattern checking circuit

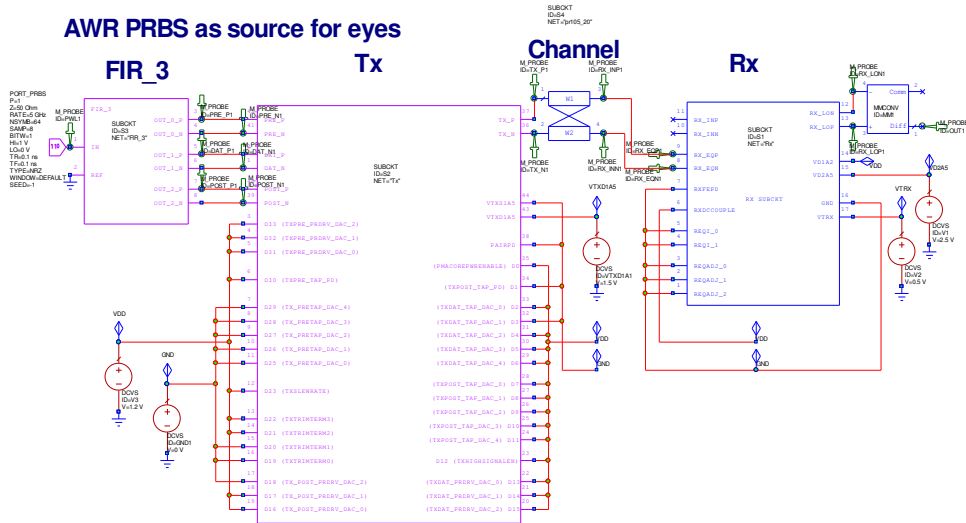
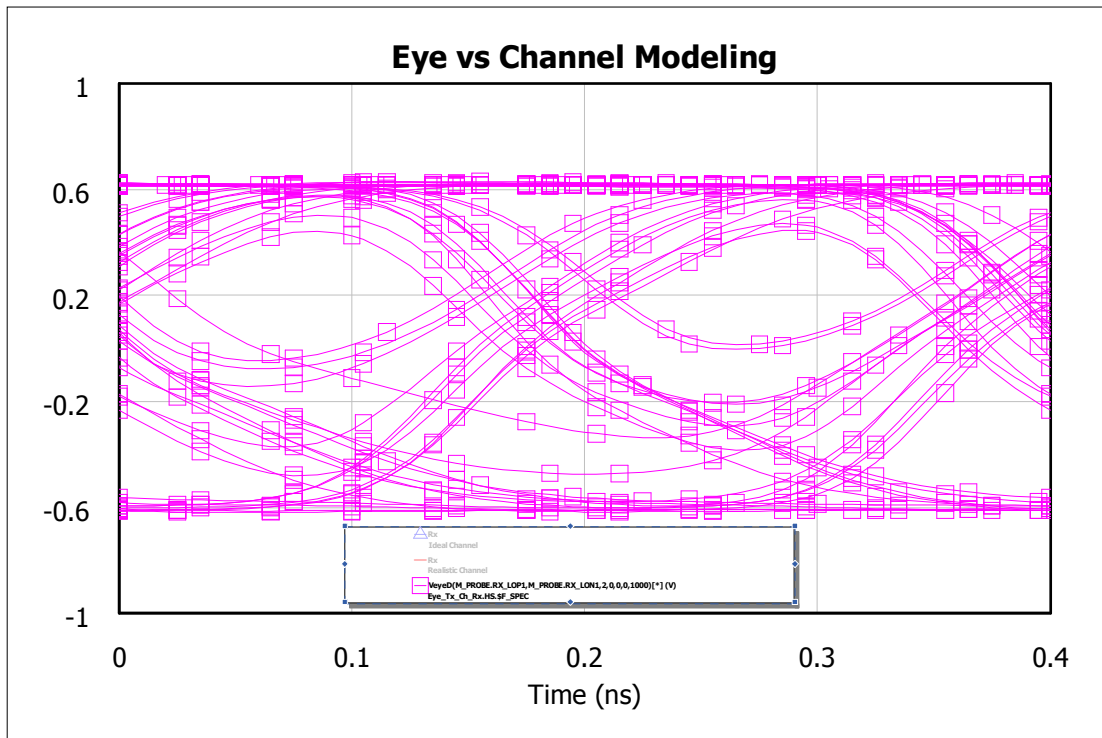


Figure 28 -- PRBS eye diagram from HSPICE



Conclusions

Backplanes are the central piece of any industrial system or telecommunications platform. Their design can predict the lifetime of the equipment and the success of the equipment. For this reason the design of the backplane has to be right the first time and guessing your way to success will ensure failure.

There are number of design decisions that must be made prior to routing a backplane. Choosing the materials, the connectors, and your fabricator are all key. Developing strong relationships up front with these suppliers is a *necessary* requirement.

Simulation has taken a key role in the development of backplane design. There are number of tools available to comprehensively simulate the backplane channel. Xilinx chose AWR and found the simulation results matched very closely with the measured results.

Developing a strategy for simulation and verification is necessary early on. It is very important to be able to study and measure the channel both actively and passively. And sharing your verification strategy with your connector and backplane fabricators is very important as well if there are any issues discovered. Having this agreed methodology in place before constructing the backplane will save much grief in the long run.

Xilinx offers complete HSPICE models which will allows designers to fully investigate the MGT performance across a channel before the product is built.

Contact your local Xilinx FAE for support of these models and to review your channel design with Xilinx MGT IO Specialists.