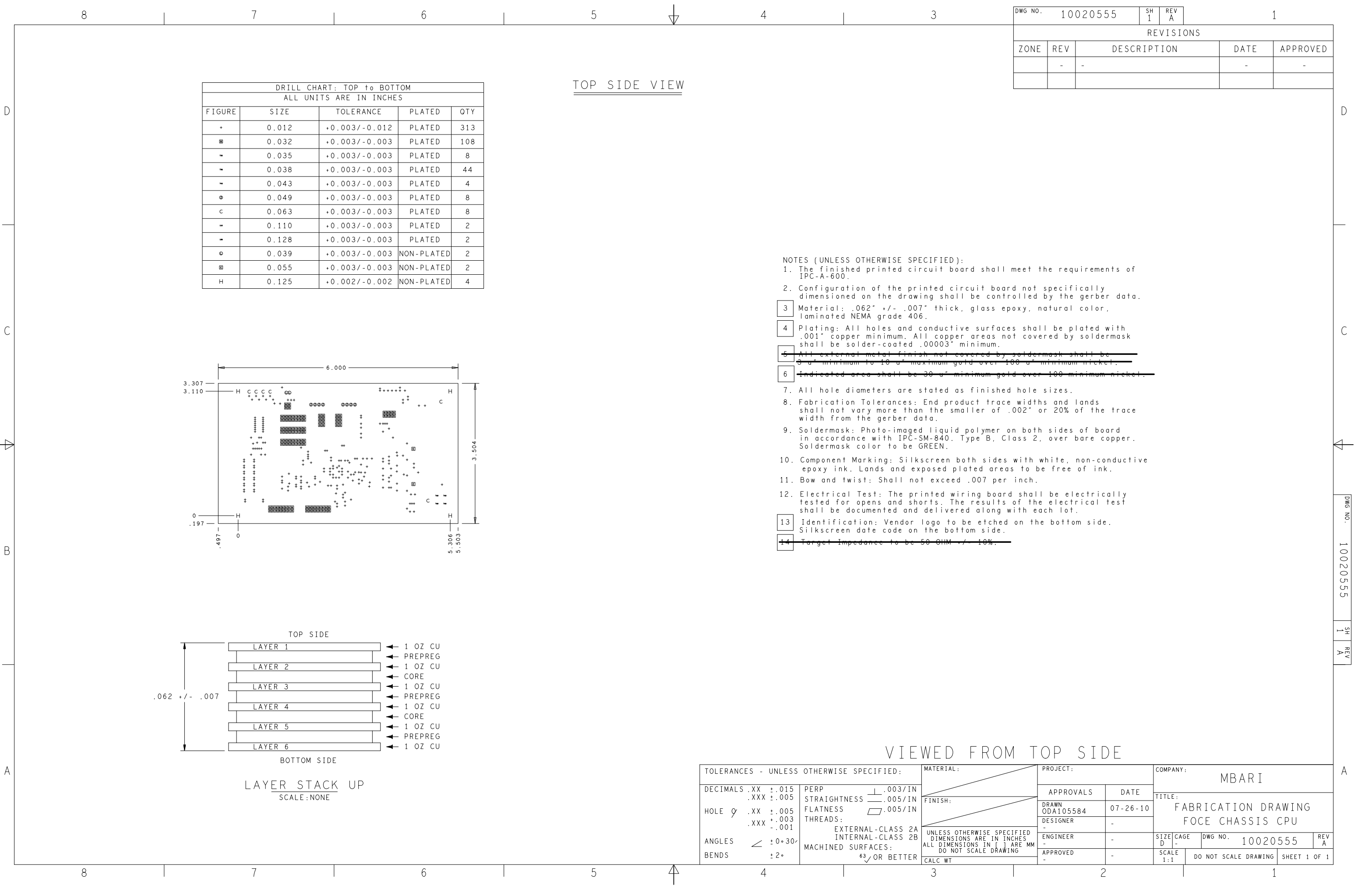
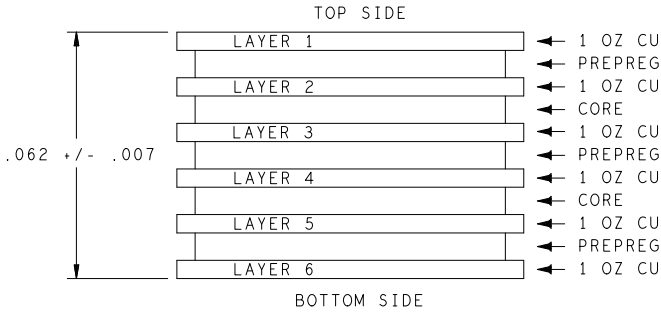




DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN INCHES				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
+	0.012	+0.003/-0.012	PLATED	313
⊞	0.032	+0.003/-0.003	PLATED	108
⊞	0.035	+0.003/-0.003	PLATED	8
⊞	0.038	+0.003/-0.003	PLATED	44
⊞	0.043	+0.003/-0.003	PLATED	4
⊞	0.049	+0.003/-0.003	PLATED	8
c	0.063	+0.003/-0.003	PLATED	8
⊞	0.110	+0.003/-0.003	PLATED	2
⊞	0.128	+0.003/-0.003	PLATED	2
⊞	0.039	+0.003/-0.003	NON-PLATED	2
⊞	0.055	+0.003/-0.003	NON-PLATED	2
H	0.125	+0.002/-0.002	NON-PLATED	4

TOP SIDE VIEW

- NOTES (UNLESS OTHERWISE SPECIFIED):
- The finished printed circuit board shall meet the requirements of IPC-A-600.
 - Configuration of the printed circuit board not specifically dimensioned on the drawing shall be controlled by the gerber data.
 - Material: .062" +/- .007" thick, glass epoxy, natural color, laminated NEMA grade 406.
 - Plating: All holes and conductive surfaces shall be plated with .001" copper minimum. All copper areas not covered by soldermask shall be solder-coated .00003" minimum.
 - All external metal finish not covered by soldermask shall be 30 u" minimum to 100 u" maximum gold over 100 u" minimum nickel.
 - Indicated area shall be 30 u" minimum gold over 100 minimum nickel.
 - All hole diameters are stated as finished hole sizes.
 - Fabrication Tolerances: End product trace widths and lands shall not vary more than the smaller of .002" or 20% of the trace width from the gerber data.
 - Soldermask: Photo-imaged liquid polymer on both sides of board in accordance with IPC-SM-840, Type B, Class 2, over bare copper. Soldermask color to be GREEN.
 - Component Marking: Silkscreen both sides with white, non-conductive epoxy ink. Lands and exposed plated areas to be free of ink.
 - Bow and twist: Shall not exceed .007 per inch.
 - Electrical Test: The printed wiring board shall be electrically tested for opens and shorts. The results of the electrical test shall be documented and delivered along with each lot.
 - Identification: Vendor logo to be etched on the bottom side. Silkscreen date code on the bottom side.
 - Target Impedance to be 50 OHM +/- 10%.



LAYER STACK UP
SCALE: NONE

VIEWED FROM TOP SIDE

TOLERANCES - UNLESS OTHERWISE SPECIFIED:				MATERIAL:		PROJECT:		COMPANY: MBARI					
DECIMALS .XX ±.015 .XXX ±.005		PERP  .003/IN STRAIGHTNESS  .005/IN FLATNESS  .005/IN THREADS: EXTERNAL-CLASS 2A INTERNAL-CLASS 2B MACHINED SURFACES: 63✓OR BETTER				APPROVALS		DATE		TITLE: FABRICATION DRAWING FOCE CHASSIS CPU			
HOLE  .XX ±.005 .XXX ±.003 - .001		FINISH:		DRAWN ODA105584		07-26-10							
ANGLES  ± 0-30° BENDS ± 2°				DESIGNER		-							
		ENGINEER		-		SIZE D		CAGE		DWG NO. 10020555		REV A	
				APPROVED		-		SCALE 1:1		DO NOT SCALE DRAWING		SHEET 1 OF 1	
		CALC WT											