Keywords: voltage references, voltage reference, DAC reference, three terminal reference, reference accuracy, DAC, digital to analog converter, digital to analog convertor, DAC design examples, error budget analysis

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APPLICATION NOTE 754

Selecting the Right Series Voltage Reference for Absolute-Accuracy Voltage-Output DAC Designs

Abstract: This article provides an in depth analysis, procedure, and selection tables for selecting the optimum series voltage reference for voltage output DACs. It covers all of the important parameters such as: input supply voltage, reference output voltage, initial accuracy, line and load regulation, stability, and noise. In addition four common design examples are given.

When designing a system that includes a digital-to-analogconverter (DAC) and an external voltage reference, the voltage-referencespecifications are as important as the specifications of the DAC itself.This article explores some of the issues involved with selecting external,three-terminal series voltage references for voltage-output DACs. Examplesof DAC system designs are used to illustrate the various trade-offs whenoptimizing for cost, accuracy, or power.

A Few Words about Voltage References

The main focus of this article is Maxim's three-terminal, series, bandgap voltage references, although buried-zener references are discussed as well. Two-terminal, shunt references are not covered, because three-terminal, series devices are now available at competitive prices and with low quiescent current that is virtually constant versus input voltage.

The MAX6006-MAX6009 two-terminal shunt-reference family is worth considering for ultra-low-power applications, as they can generate 1.25V, 2.048V, 2.5V, or 3V with an operating current of only 1µA. Maxim also offers a family of low-cost, industry-standard LM4040 shunt references.

Zener-based references receive light treatment primarily because of their high input-voltage requirement (which limits their applicability in systems with lower supply voltages). In spite of this narrowing of focus, many topics covered in this article are applicable to other reference types. For example, the reference-voltage change on a shunt reference caused by varying bias currents is analogous to the load regulation of a series reference, and the effect on the DAC performance can be analyzed in a similar manner.

Figure 1 depicts the connection between a three-terminal, series voltage reference (the MAX6325) and a DAC (the MAX5170) for a typical design. In this case, an external capacitor is shown between the reference and the DAC, but it can usually be eliminated if space is limited and if the DAC does not have rapid power supply or output transient switching. The figure also shows a power-supply filtering input capacitor and a broadband noise-reduction capacitor, but both of these capacitors are also optional. Finally, the MAX6325 voltage reference has a TRIM pin that allows the end user to optionally trim out the initial error with an external potentiometer.

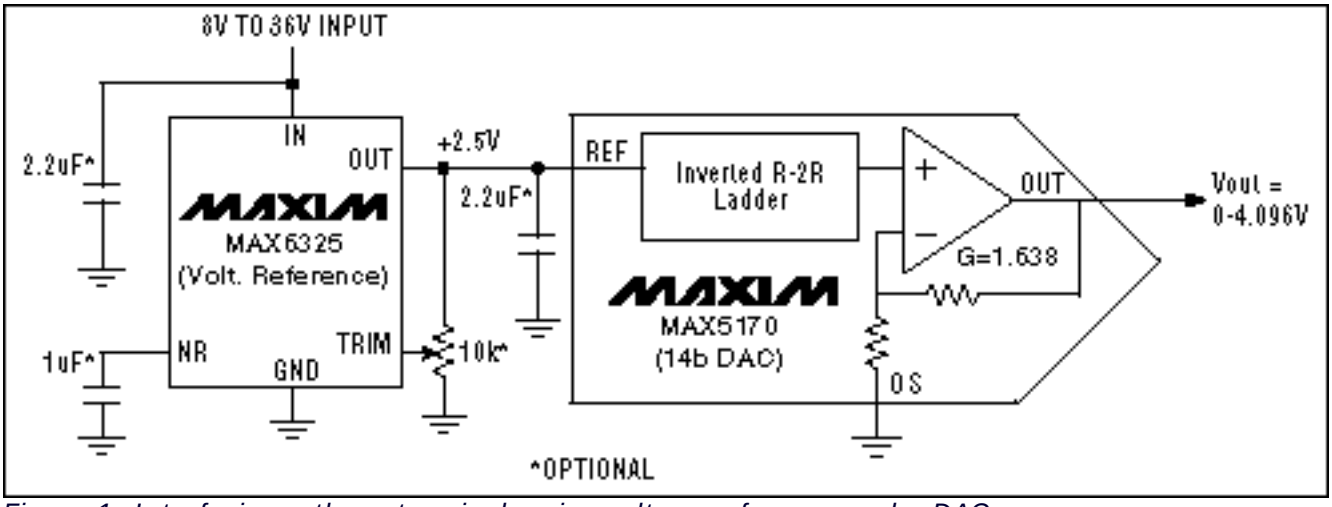

Figure 1. Interfacing a three-terminal series voltage reference and a DAC.

Definitions of Voltage-Reference Specifications

In addition to cost and packaging, several (but not all) specifications will be covered in the discussions on voltage-reference selection. These specifications are described in detail in the references listed at the end of the article, so they will be only briefly summarized here. What follow are definitions of the specifications:

Input Supply Voltage: Power-supply input voltage to the reference. Limited on the upper end by the silicon process used for the reference and on the bottom end by the reference output and dropout voltages:

$$V_{IN(MIN)} = V_{REF} + V_{DROPOUT}$$

Reference Output Voltage: Regulated voltage used at the DAC reference input.

Initial Accuracy: Accuracy is a slight misnomer, as it actually represents the initial output-voltage error. Specified in % or mV at 25°C. Some fixed-voltage and any adjustable references can be trimmed to improve accuracy.

Reference Output Current: The available load current that the voltage reference can source to the DAC reference input. All of the references covered in this article can also sink current, but not as well.

Reference-Load Regulation: Incremental change in reference output voltage for a DC change in reference output current. Specified in µV/µA or equivalently mV/mA, mV (over the entire output-current range), ppm/mA, or %/mA.

Input-Line Regulation: Incremental change in reference output voltage for a DC change in input supply voltage. Specified in µV/V.

Output-Voltage Temperature Coefficient (Tempco): Change in reference output voltage for a given change in temperature. Specified in ppm/°C. Maxim uses the box method, where the maximum reference output fractional voltage change is divided by the maximum operating-temperature range:

$$TCV_{OUT} = 10^6 \times | \Delta V_{REF(max)} / V_{REF} | / (T_{MAX}-T_{MIN})$$

Output-Voltage Temperature Hysteresis: Change in reference output voltage at +25°C after a temperature cycle (T_{MIN} to T_{MAX}) is applied. Specified as a ratio of voltages expressed in ppm.

$$TEMPHYST = 10^6 \times | \Delta V_{REF} / V_{REF} |$$, where $\Delta V_{REF} = V_{REF}$ before ΔT cycle minus V_{REF} after ΔT cycle.

Output-Voltage Long-Term Stability: Change in reference output voltage versus time. Specified in ppm/1000 hours. Cumulative drift beyond a 1000-hour interval is not specified, but it is usually much lower than the initial drift, which can itself be improved by PCB-level burn-in.

Output Noise Voltage: Voltage noise at the reference output. The 1/f component is specified in µVp-p over a 0.1Hz to 10Hz bandwidth, and the wideband noise is usually specified in μV_{RMS} over a 10Hz to 10kHz bandwidth.

Capacitive-Load Stability Range: Range of capacitive loads (includes user-supplied capacitors, the capacitance presented by the load, and stray capacitance) that the reference can tolerate at its output. External capacitors are needed only to limit large loads or supply transients, and can be eliminated in many designs to save board space. A few references have pins where a compensation capacitor (the MAX872) or a noise-reduction capacitor (the MAX6325) can be added to improve performance.

DAC Considerations

Only buffered-voltage-output DACs are discussed, as the key points are easier to illustrate with this architecture. Current-output DACs are typically used in a multiplying configuration (MDAC) to provide variable gain, and they usually require external op amps to generate a voltage output.

All of the Maxim voltage-output DACs considered in this article use an inverted R-2R architecture. From the reference-voltage standpoint, the main characteristic of this DAC architecture is the varying DAC reference input resistance versus DAC code. Care must be taken to ensure that the voltage reference can source enough current at the DAC's minimum reference input resistance and has sufficient load regulation as the DAC codes change. A 4-bit example, along with its normalized reference input current, is shown in **Figure 2**. Note that the reference current at DAC code 0 is not shown in the plot, as all of the switches connected to the reference are open and virtually no reference current flows. Two other DAC specifications important to voltage-reference selection are *reference-input-voltage range* and *DAC output gain.*

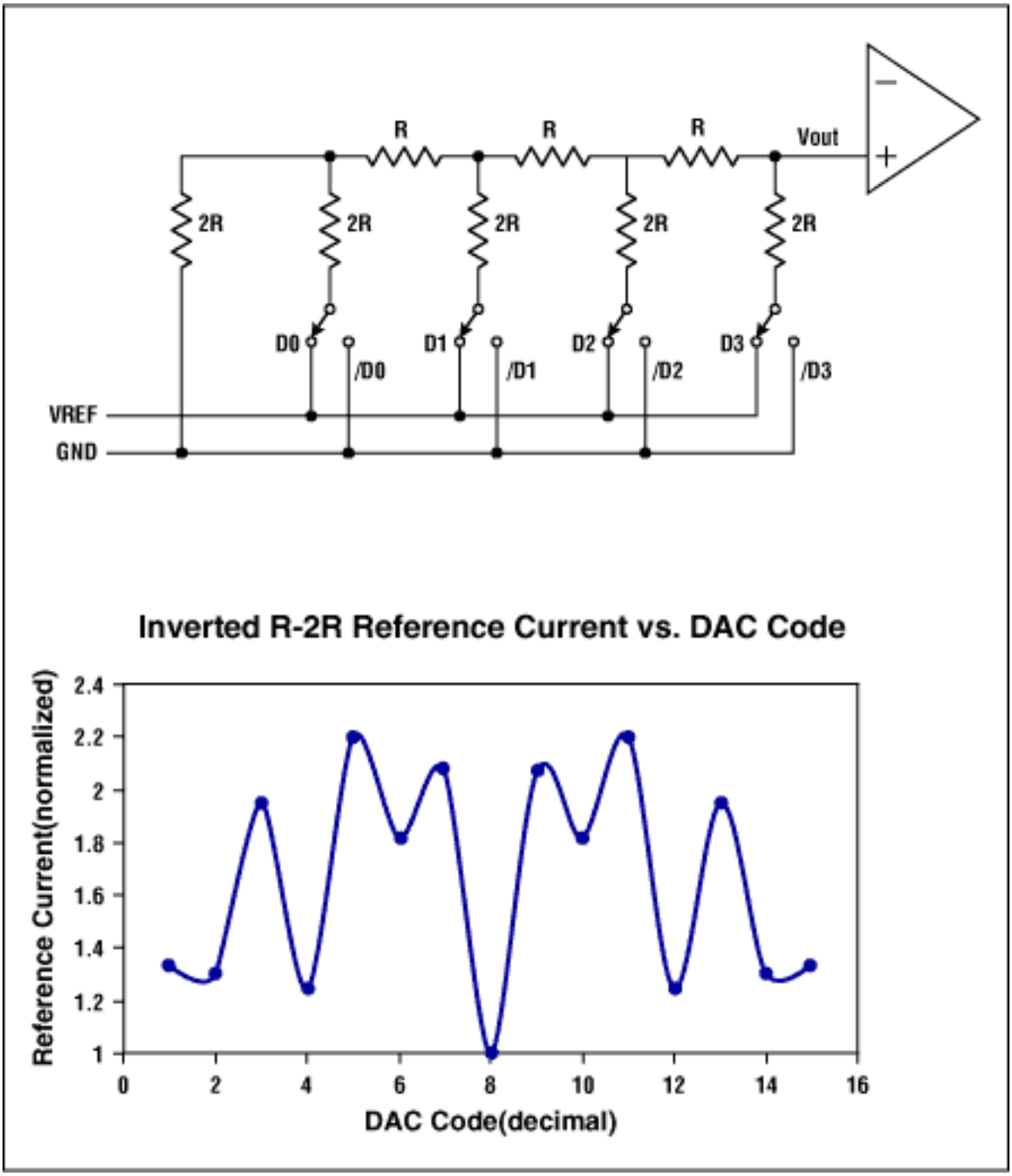

Figure 2. Inverted R-2R architecture and reference-input-current variation (4-bit).

Output Error and Accuracy Definitions

We define *output error* as the deviation from an ideal output voltage that would be provided by a perfect voltage reference and DAC. It's important to note that we are addressing absolute accuracy in this article, meaning that everything is referenced to an ideal DAC output-voltage range. For example, a 12-bit DAC code 4095 should produce an output of 4.095V with a reference voltage of 4.096V; any deviation from this is an error. This is in contrast to relative accuracy, where the full-scale output is defined more by the application than by an absolute voltage. For example, in a ratiometric system where an ADC and a DAC with equal resolution share a reference, it may not matter (within reason) what the actual reference voltage is, as long as the DAC-output and ADC-input voltages are nearly equivalent for a given digital code.

Output error is often specified as a one-sided value (in LSBs at the DAC resolution), but it actually implies a double-sided error (**Figure 3**). For example, a 12-bit DAC with a 4.096V output range has an ideal LSB step size of 4.096V/4096 = 1mV. If the specified output error in this case is 4LSBs at 12-bit resolution, this means the

DAC output at any code could be ±4LSBs (or ±4mV) from the ideal value. We define accuracy in terms of how many actual bits we have at our disposal to reach a desired output voltage with at most 1LSB of error:

$$\text{Accuracy} = \text{DAC Resolution} - \log_2(\text{Error})$$

In our example, we effectively have 10 bits (12 - $\log_2(4)$) of accuracy, because we can only get to within 1LSB at 10-bit resolution (±4mV = ±4/4096 = ±1/1024) of any given ideal DAC output value.

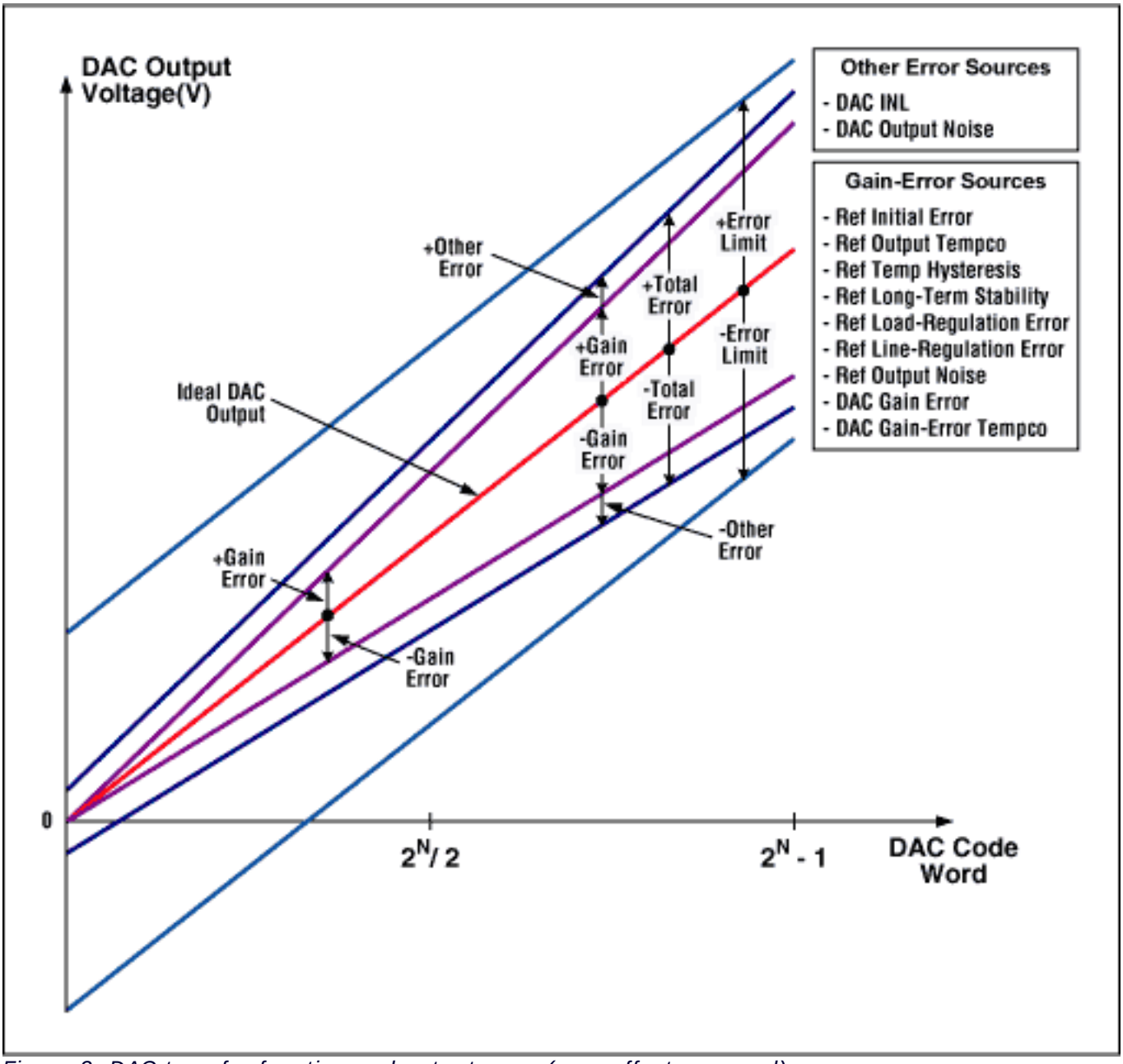

Figure 3. DAC transfer function and output error (zero offset assumed).

There are several sources that contribute to output error, but some (such as DAC offset) are ignored because they are not relevant to the reference-voltage selection process. Voltage-reference error sources that are considered include *initial error, tempco, temperature hysteresis, long-term stability, load and line regulation,* and *output noise.* DAC error sources include *INL, gain error, gain-error tempco,* and *output noise.*

Although the target error applies over the entire DAC code range, most of the error sources mentioned above cause an effective gain-error variation that is largest near the full-scale (highest DAC codes) of the transfer function (Figure 3). Gain errors are reduced with decreasing DAC code value; these errors are halved at midscale, and they virtually disappear near code zero, where offset error dominates. Error sources that do not

exclusively affect the gain error and apply equally over most of the DAC code range include DAC INL and output noise.

INL is typically defined using one of two methods: *absolute linearity* or *end-point linearity.* Absolute linearity compares the DAC linearity to the ideal transfer-function linearity. End-point linearity uses the two measured end points to define the linearity (a straight line is drawn between these points), and all other points are compared to this line. In either case, INL should be included in the error analysis. In the latter case, the DAC INL error is zero at the end points, but can be present at DAC code words just inside these values. As an example, for a 12-bit DAC with INL defined between the end points of 0V and 4.095V (full-scale), the INL specification applies to DAC codes near 0 and 4095. For maximum error calculations, it is reasonable to add the DAC's INL and noise-induced output errors to the previously mentioned gain errors that are most severe near code 4095.

DAC Design Examples

To illustrate the steps involved with voltage-reference selection for DACs, a few design examples were created to cover a range of applications (Table 1). Only 10-, 12-, and 14-bit DAC designs are included in these examples, because they are the most instructive. The design steps are broken into individual sections by design examples (see Design A, Design B, and so forth).

Table 1. Requirements for DAC Design Examples

Parameter	Design A	Design B	Design C	Design D
Main Design Objectives	Low cost, loose accuracy	High absolute accuracy and precision	One-time calibrated, low drift	Low voltage, battery powered, moderate accuracy
Example Application	Consumer audio device	Lab instrument	Digital offset and gain adjustment	Portable instrument
DAC	MAX5304, 10-bit single	MAX5170, 14-bit single	MAX5154, 12-bit dual	MAX5176, 12-bit single
Minimum Reference Input Resistance	18kΩ	18kΩ	7kΩ (14kΩ|| 14kΩ shared reference inputs)	18kΩ
Output Voltage	Range = 0 -2.5V	Range = 0 - 4.096V	Range = 0 - 4.000V	Range = 0 - 2.048V
DAC Output	Force/sense	Fixed gain = 1.638	Fixed gain = 2	Fixed gain = 1.638
Power Supply	5V(varying) 4.5V min 5.5V max	5V(constant) 4.95V min +12V available	5V(constant) 4.75V min 5.25V max	3V(varying V_{BATT}) 2.7V min 3.6V max
Temperature Range	0°C to 70°C (commercial)	0°C to 70°C (commercial)	-40°C to 85°C (extended)	15°C to 45°C (< commercial)
Signal BW	10Hz to 10kHz	DC to 1kHz	DC to 10Hz	DC to 10Hz
DAC Calibration	None	Burn-in + annual (gain and offset)	One-time factory (gain and offset)	None
Maximum Error Target	16LSB @ 10 bits (6-bit accuracy)	2LSB @ 14 bits (13-bit accuracy)	4LSB @ 12 bits (10-bit accuracy)	8LSB @ 12 bits (9-bit accuracy)

Step 1: Voltage Ranges and Reference-Voltage Determination

The first consideration when selecting a voltage reference for a DAC application is to evaluate the supply-voltage and the DAC output-voltage ranges (Table 2). To simplify the design examples described above, DACs have already been chosen, so their output gain is not a variable we will trade off as in a real design.

Table 2. Voltage-Related Parameters for DAC Design Examples

Parameter	Design A	Design B	Design C	Design D
Main Design Objectives	Low cost, loose accuracy	High absolute accuracy and precision	One-time calibrated, low drift	Low voltage, battery powered, moderate accuracy
Example Application	Consumer audio device	Lab instrument	Digital offset and gain adjustment	Portable instrument
Output Voltage	Range = 0 - 2.5V	Range = 0 - 4.096V	Range = 0 - 4.096V	Range = 0 - 2.048V
Power Supply	5V(varying) 4.5V min 5.5V max	5V(constant) 4.95V min +12V available	5V(constant) 4.75V min 5.25V max	3V(varying V_{BATT}) 2.7V min 3.6V max
Reference Voltage and DAC Gain Options for Desired Output Voltage	2.5V (gain = 1) * 2.048V (gain = 1.221) 1.25V (gain = 2)	2.5V (gain = 1.638)* 2.048V (gain = 2) 1.25V (gain = 3.277) 3.0V (gain = 1.365)	2.048V (gain = 2) * 1.25V (gain = 3.277) 3.0V (gain = 1.365)	1.25V (gain = 1.638)*
Dropout Voltage	2.00V	9.5V	2.70V	1.45V

*Reference voltage and DAC gain chosen for each design example

Design A: Low Cost, Loose Accuracy

For the Design-A example, VDD is 5V and the output range is 0-2.5V, so a 2.5V reference is used and the MAX5304 force/sense output is set to unity gain (OUT and FB pins shorted). A lower voltage reference could be used with a higher, externally set gain, but we have opted to save the two resistors for this low-cost design.

Design B: High Absolute Accuracy and Precision

A 2.5V reference is chosen for the Design-B example, as the MAX5170 gain is fixed at 1.638 and a final output-voltage range of 0-4.096V is required. If a lower reference voltage is desired for Design B, a MAX5171 DAC could be used and its output force/sense gain could be set higher than 1.638 with external resistors, as shown in **Figure 4**. Note that the minimum VDD level is 4.95V, so the highest reference voltage we could use is 4.95V - 1.4V = 3.55V, as the DAC reference input is limited to (VDD - 1.4V)*.

*This limit applies to all DACs mentioned in this article.

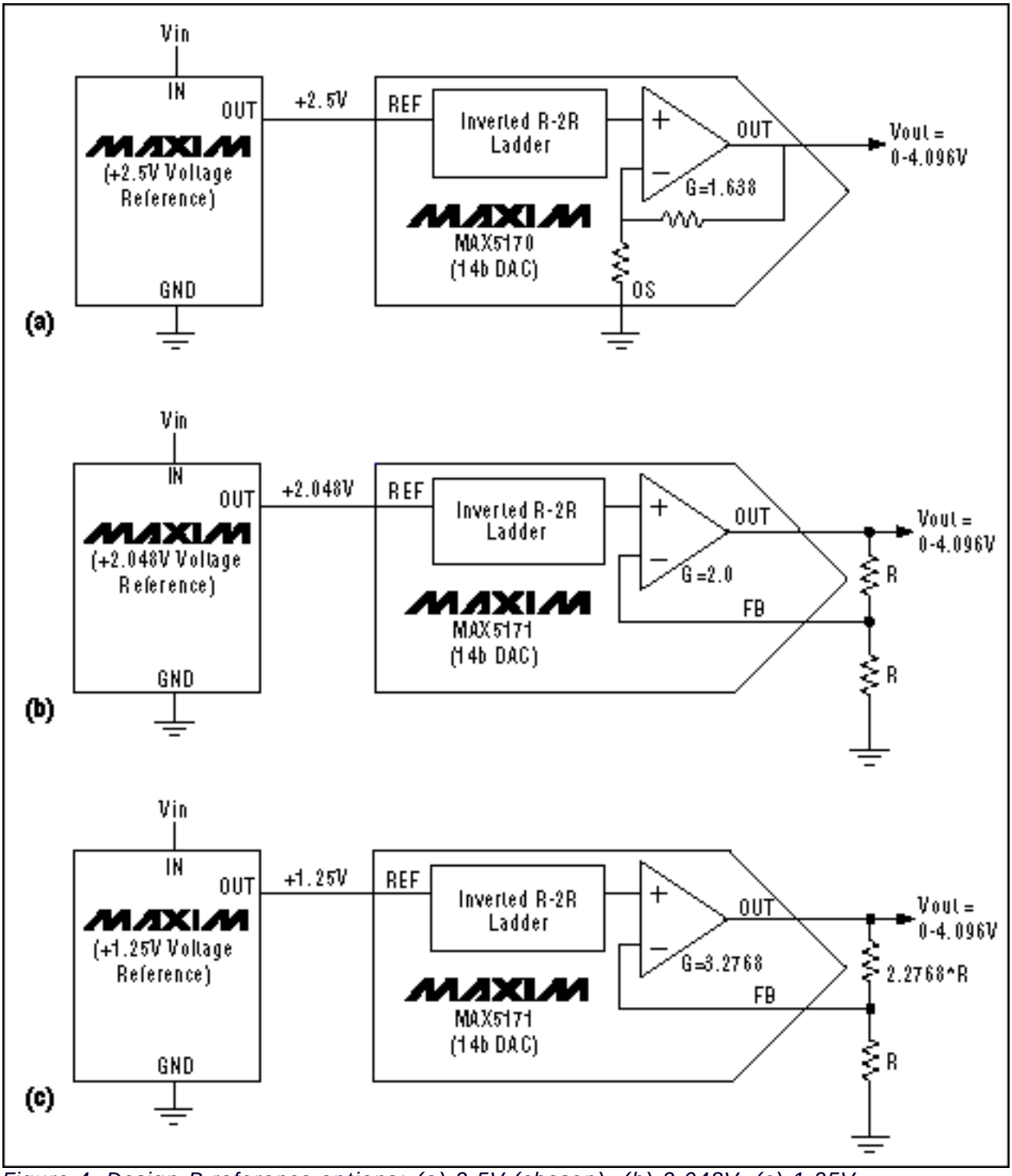

Figure 4. Design-B reference options: (a) 2.5V (chosen), (b) 2.048V, (c) 1.25V.

Design C: One-Time Calibrated, Low Drift

In the Design-C example, the MAX5154 has a fixed gain of 2, so a 2.048V reference provides a nominal 4.096V output at full-scale. This voltage must exceed our 4.000V design requirement, so that we can use a gain calibration to scale the voltage down to the 0V to 4V range. This design also has other reference-voltage options if the MAX5156 force/sense DAC is used. Note that the reference-input upper-limit voltage is 4.75V - 1.4V = 3.35V.

Design D: Low Voltage, Battery Powered, Moderate Accuracy

The minimum VDD is 2.7V in the Design-D example, so the largest reference voltage that could be used is 2.7V - 1.4V = 1.3V. For this example, a 1.25V reference satisfies the 0V to 2.048V output range, as the MAX5176 gain is 1.638. It's important that the worst-case reference voltage, including all error terms, remains below 1.3V, or the specification for the DAC reference input voltage will be exceeded.

Approximate dropout voltages were calculated for each of the design examples (Table 2). All of these voltages are well above the 200mV (or lower) dropout voltages typical of Maxim's voltage references. Because the upper reference input voltage of most Maxim DACs is limited to VDD - 1.4V, dropout voltages can normally be ignored with these designs if the DAC and the voltage reference use the same positive supply rail. The dropout voltages are approximate, because they were calculated without any error terms such as initial accuracy, but these errors are small compared to typical dropout voltages and can be ignored.

Step 2: Initial Voltage-Reference Device-Selection Criteria

There are many factors to consider when selecting the optimum reference for each design. To make the procedure manageable, candidate devices will be identified based on the reference voltage determined above, an estimate of required initial accuracy, an approximated temperature coefficient, and the reference output current needed for the chosen DAC (Table 3). Other factors such as cost, quiescent current, packaging, and a quick glimpse at the remaining specifications will be used to select a specific initial device for each design. The remaining specifications will be analyzed in the following section (Step 3) to determine if the devices satisfy the overall accuracy requirements.

Table 3. Initial Device-Selection Considerations

Parameter	Design A	Design B	Design C	Design D
Main Design Objectives	Low cost, loose accuracy	High absolute accuracy and precision	One-time calibrated, low drift	Low voltage, battery powered, moderate accuracy
Example Application	Consumer audio device	Lab instrument	Digital offset and gain adjustment	Portable instrument
DAC Calibration	None	Annual (gain and offset)	One-time factory (gain and offset)	None
Maximum Error Target	16LSB @ 10 bits (6-bit accuracy)	2LSB @ 14 bits (13-bit accuracy)	4LSB @ 12 bits (10-bit accuracy)	16LSB @ 12 bits (8-bit accuracy)
Estimated Initial Accuracy (from Step 2)	0.4% (4LSB @ 10 bits)	Not critical due to gain calibration	Not critical due to gain calibration	0.32% (3200ppm)
Estimated Tempco (from Step 2)	75ppm/°C	2ppm/°C	5ppm/°C	20ppm/°C
Reference Voltage (V_{REF}) (from Step 1)	2.5V	2.5V	2.048V	1.25V
Minimum Reference Input Resistance from Data Sheet (R_{MIN})	18kΩ	18kΩ	7kΩ (14kΩ||14kΩ shared reference inputs)	18kΩ
Maximum Output Current Requirement (V_{REF}/R_{MIN})	140µA max	140µA max	293µA max (dual DACs)	69µA max
Voltage-Reference Candidates (Initial Accuracy, Tempco, Output Current)	**MAX6002** (1%,100ppm/°C, 400µA) **MAX6102*** (0.4%, 75ppm/°C, 5mA) **MAX6125** (1%, 50ppm/°C, 1mA)	**MAX6225A/B** (0.04/0.12%, 2/5ppm/°C,5mA) **MAX6325*** (0.04%, 1ppm/°C, 15mA)	**MAX6162A*/B** (0.1/0.24%, 5/10ppm/°C, 5mA) **MAX6191A/B/C** (0.1/0.24/0.5%, 5/10/25ppm/°C, 500µA)	**MAX6012A/B** (0.32/0.48%, 20/30ppm/°C, 500µA) **MAX6190A*/B/C** (0.16/0.32/0.48%, 5/10/25ppm/°C, 500µA)

*Initial reference selection for each design example

Design A: Low Cost, Loose Accuracy

At first glance, the MAX6002 ($0.39/2500pcs) appears to be an obvious choice for Design A, which requires low cost and fairly loose accuracy. But a further look reveals that the MAX6002 is not a good option. Its combined initial accuracy (1%, which is ~10LSB at 10 bits) and tempco error (70°C × 100ppm/°C = 7000ppm ~ 7LSB at 10 bits) already violate the overall accuracy requirement of Design A (17LSB exceeds the design requirement of 16LSB at 10 bits), even without including the other error terms such as load regulation, noise, and so forth. The MAX6125 also has 1% accuracy, and its 50ppm/°C tempco brings us within the Design-A error limit (~13.5LSB),

but its cost ($0.95/1000pcs) is too high for this application.

The MAX6002 could be used if the accuracy requirement is loosened further or if some type of calibration scheme is implemented, whereas the more expensive MAX6125 could probably meet the requirements without compromise. Assuming the accuracy requirement is rigid, this example illustrates a key trade-off in reference selection for DAC designs: initial component cost (the MAX6125) versus cost of calibration (the MAX6002).

Further study of the Maxim voltage-reference selection table reveals a better option for Design A. If we arbitrarily allocate half of the total error (8LSB at 10 bits ~ 0.8%) to the initial accuracy and half to the tempco (0.8% = 8000ppm/70°C = 114ppm/°C), the MAX6102 ($0.55/2500pcs, 0.4% initial accuracy, 75ppm/°C) surfaces as the best choice. The MAX6102 can source 5mA of current to the load, so it is able to drive the MAX5304 DAC's reference input (2.5V/18 kΩ ~ 140µA max). If the MAX6102 is ruled out when the other error terms are analyzed, the MAX6125 can be reconsidered as a backup alternative.

Design B: High Absolute Accuracy and Precision

Because Design B has such challenging accuracy requirements, the MAX6225 and MAX6325 buried-zener references are the initial candidates because they have such low tempcos, excellent long-term stability, and low noise. These devices also have very good initial accuracy, but this is a moot specification in the case of Design B, as gain errors caused by the DAC and the voltage reference are calibrated out. The MAX6225 and the MAX6335 source 15mA, so driving the MAX5170 DAC reference input (2.5V/18k ~ 140µA max) is not an issue. The MAX6325 is chosen because it has the only tempco (70°C × 1ppm/°C = 70ppm max) that puts us beneath the overall 122ppm accuracy requirement (2LSB @ 14 bits = $2/2^{14}$ = 2/16384 = 1.22 × 10^{-4} = 122ppm) while leaving margin for the other error sources. If we relax the Design-B accuracy requirements slightly, the MAX6225 A-grade device (2ppm/°C max tempco) would allow us to cut the reference cost by more than half.

A 12V supply is conveniently present in the Design-B example, allowing the use of the MAX6325, which needs an input voltage of at least 8V. If 8V (or higher) is not available in the system, the MAX6166 (A grade) or MAX6192 (A grade) bandgap-based references could be considered, but a slight relaxation of the system specifications would be required.

Design C: One-Time Calibrated, Low Drift

The MAX6162 and MAX6191 A-grade devices are considered because of their low tempcos (5ppm/°C max), which are necessary to meet the requirements of Design C:

Total Error Budget is 4LSB at 12 bits = 4 / 4096 ×10^6 = 977ppm

Required Tempco <= 977ppm / (85 - (-40)) °C = 7.8ppm / °C

Available Error Beyond Tempco = 977ppm - 5ppm / °C ×125°C = 352ppm

Note that the MAX6162 and the MAX6191 both have 2mV (977ppm) initial accuracy, but this is not a concern with the 2.048V reference because the output-voltage range is only 0-4.000V and a gain calibration is planned for this design. The MAX6162 (5mA of output current drive) and the MAX6191 (500µA of output current drive) are both capable of driving the 293µA reference input current that results when the two MAX5154 DAC reference pins are tied together (2.048V/[14kΩ||14kΩ]); however, the MAX6162 has more margin if additional loads are connected to the reference output. The MAX6162 does have higher quiescent current than the MAX6191 (120µA versus 35µA max), but this is not a deciding factor as Design C is not power-constrained.

After reviewing the initial specifications, it's clear that either device is probably acceptable. However, the MAX6162 is the first choice due to its higher output current. If further analysis shows the MAX6162 to be marginally unacceptable, the MAX6191 could be considered because it has slightly better load-regulation, temperature-hysteresis, and long-term-stability specifications.

Design D: Low Voltage, Battery Powered, Moderate Accuracy

Following the approaches used in the other examples, the total error for Design D is found to be 3906ppm (10^6 × 16/4096). Over the narrow 15°C to 45°C temperature range, we can tolerate a tempco of at most 130.2ppm/°C (3906ppm/30°C). Using our rule of thumb from Design A to allocate roughly half of the error budget to the tempco (<65ppm/°C), reasonable, conservative reference choices are the MAX6012 (A and B grades are 20ppm/°C and 30ppm/°C, respectively) and the MAX6190 (A, B, and C grades are 5ppm/°C, 10ppm/°C, and 25ppm/°C, respectively). These parts are considered, because they have a maximum quiescent current of 35µA, which is appropriate for the low-power needs of Design D.

The MAX6190 price (C grade is $1.45/1000pcs) is in the same range as the MAX6012 price (B grade is $1.35/2500pcs). Either part will probably work in the application. However, the A-grade MAX6012 is especially attractive, because it is available in a SOT23-3 package, which is ideal for a small, battery-powered, portable instrument.

A quick check of the A-grade MAX6012 reveals the tempco-related error to be 600ppm (30°C × 20ppm/°C). The initial error of 3200ppm (0.32%) also needs to be considered, as there is no trimming planned for this design. The sum of these two errors is 3800ppm out of the possible 3906ppm design limit. With this marginal situation, it's likely that some of the other specifications considered in the next section (Step 3), such as load regulation, temperature hysteresis, and even line regulation (because of the varying battery voltage), will put us beyond 3906ppm. Because the MAX6012 is probably insufficient, we will forego the SOT23-3 package and choose the A-grade MAX6190 as a starting point, as its initial error of 1600ppm and 5ppm/°C leave enough room for the other error terms. Reference output current is not a concern for this design, because the MAX6190 can supply 500µA (>>69µA design requirement).

Step 3: Final Specification Review and Error-Budget Analysis

With the preliminary selection of references complete and backup ICs in place, it's now time to verify the remaining specifications, which include *reference-load regulation, input-line regulation, output-voltage temperature hysteresis, output-voltage long-term stability,* and *output noise voltage.* The key system-level and DAC specifications for each design are also needed for the analysis (Table 4).

Table 4. Important Specifications for Final Analysis

Parameter	Design A	Design B	Design C	Design D
Main Design Objectives	Low cost, loose accuracy	High absolute accuracy and precision	One-time calibrated, low drift	Low voltage, battery powered, moderate accuracy
Example Application	Consumer audio device	Lab instrument	Digital offset and gain adjustment	Portable instrument
DAC	MAX5304, 10-bit single	MAX5170, 14-bit single	MAX5154, 12-bit dual	MAX5176, 12-bit single
DAC Output	Force/sense gain set to 1	Fixed gain = 1.638	Fixed gain = 2	Fixed gain = 1.638
Voltage Reference	MAX6102	MAX6325	MAX6162 A grade	MAX6190 A grade
Reference Voltage	2.5V	2.5V	2.048V	1.25V
Reference Initial Accuracy	0.4% or 4000ppm	Not critical due to gain calibration	Not critical due to gain calibration	0.16% or 1600ppm
Selected Reference Tempco (maximum)	75ppm°C	1ppm/°C	5ppm/°C	5ppm/°C
Reference-Load Regulation	0.9mV/mA	6ppm/mA	0.9mV/mA	0.5µV/µA
Temperature Range	0°C to 70°C (commercial)	0°C to 70°C (commercial)	-40°C to 85°C (extended)	15°C to 45°C (< commercial)
Signal BW	10Hz to 10kHz	DC to 1kHz	DC to 10Hz	DC to 10Hz
DAC Calibration	None	Annual (gain and offset)	One-time factory (gain and offset)	None
Max Error Target	15625ppm (16LSB @ 10 bits)	122ppm (2LSB @ 14 bits)	977ppm (4LSB @ 12 bits)	3906ppm (16LSB @ 12 bits)

Each example is analyzed, focusing on the specifications that apply to that particular design. The results of this analysis, along with the results of the previous section, are summarized in an error budget in Table 5.

It is most convenient to do the error-budget accounting in ppm, although this could be done equivalently in other units such as %, mV, or LSBs. It's important to apply the proper scaling and to use the proper normalization factor to get the correct error values. Reference error terms can be equivalently calculated relative to the reference voltage or the DAC output voltage. For example, if we assume a reference error of 2.5mV (noise, drift, etc.) and a reference voltage of 2.5V, we get the following:

$$\text{Reference Output Error} = 10^6 \times 2.5\text{mV} / 2.5\text{V} = 1000\text{ppm}$$

If we assume that the DAC output amplifier has a gain of 2.0, both the error and the reference voltage are scaled, so we get the same result at the DAC output (5V full-scale range):

$$\text{DAC Output Error} = 10^6 \times (2.5\text{mV} \times 2) / (2.5\text{V} \times 2) = 1000\text{ppm}$$

Table 5. Error-Budget Analysis

Parameter	Design A	Design B	Design C	Design D
Main Design Objectives	Low cost, loose accuracy	High absolute accuracy and precision	One-time calibrated, low drift	Low voltage, battery powered, moderate accuracy
Example Application	Consumer audio device	Lab instrument	Digital offset and gain adjustment	Portable instrument
Reference Initial Error	4000ppm	-	-	1600ppm
Reference/DAC Post- Calibration Error	-	0ppm	244ppm	-
Reference Tempco Error	5250ppm	70ppm	625ppm	150ppm
Reference Temperature Hysteresis	130ppm	20ppm	80ppm	75ppm
Reference Long-Term Stability	100ppm	30ppm	160ppm	100ppm
Reference Load-Regulation Error	50ppm	1ppm	129ppm	28ppm
Reference Line-Regulation Error	120ppm	0ppm	0ppm	58ppm
Reference Output Noise	17ppm	2ppm	5ppm	10ppm
DAC INL	3906ppm	61ppm	122ppm	488ppm
DAC Gain Error	1953ppm	0ppm	-	1953ppm
DAC Gain TC	70ppm	-	500	-
DAC Noise	-	1ppm	-	0ppm
Worst-Case Error	15596ppm	184ppm	1865ppm	4462ppm
Root Sum Square Error	7917ppm	100ppm	874ppm	2580ppm
Target Error	**15625ppm**	**122ppm**	**977ppm**	**3906 ppm**
Worst-Case Margin	29ppm	-62ppm	-888ppm	-556ppm
Root Sum Square Margin	7708ppm	22ppm	103ppm	1326ppm

Design A: Low Cost, Loose Accuracy

No calibration or trimming is planned for Design A, so the MAX6102 initial error of 4000ppm (or 0.4%) directly becomes part of the budget, as does the 5250ppm due to the voltage-reference tempco (70°C × 75ppm/°C). The typical MAX6102 output-voltage temperature-hysteresis specification is also used directly in the error budget (keeping in mind that this is a typical value if we find ourselves with a design having marginal accuracy). For output-voltage long-term stability, we assume twice the MAX6102 1000-hour specification (2 × 50ppm = 100ppm), which is fairly conservative, as it's usually much better after the first 1000 hours. A conservative estimate here at least partially offsets the typical specification used for temperature hysteresis.

To calculate the variation in reference voltage caused by load regulation, we need to know the worst-case range

of currents that the voltage reference supplies to the DAC's reference input. In Step 2, we determined the maximum DAC reference current that the MAX6102 would have to drive: 140µA. The minimum current is close to 0, as the MAX5304 reference input is effectively an open circuit (several GΩ input impedance) when the DAC code value is 0. This means the total output-current variation that the MAX6102 sees is 140µA, and this value should be used for the load-regulation calculation:

Load-Regulation Error = 140µA × 0.9mV / mA = 126µV (max)

= 10^6 × 126µV / 2.5V = 50ppm (max)

In general, it is best to be conservative and use the maximum output current directly for the load-regulation calculation. An exception may be if you're trying to extract the last bit of accuracy from a design and both the maximum and minimum DAC reference input resistance values are well specified. This approach results in a smaller load-regulation error because of the smaller ΔI_{REF}.

Because the power supply is specified as varying for this example, we need to consider the effects of input line regulation on the MAX6102 reference. The power-supply range is specified as 4.5V to 5.5V. From this, a conservative reference-voltage line-regulation calculation is possible:

Line-Regulation Error = (5.5V - 4.5V) × 300µV / V = 300µV (max)

= 10^6 × 300µV / 2.5V = 120ppm (max)

The final voltage-reference-related error term to consider is the effect of reference output-noise voltage. Conveniently, Design A has a signal bandwidth (10Hz to 10kHz) that corresponds to the exact MAX6102 noise voltage bandwidth, so the wideband-noise-voltage specification of $30\mu V_{RMS}$ is used directly (that is, bandwidth scaling is not required). Comparing the load- and line-regulation values (126µV and 300µV, respectively), we can see that noise is not a major contributor in this design. Using crude approximations to get numbers for the error analysis, we can assume an effective peak noise value of ~42µV (30µV ×√2), which corresponds to 17ppm (10^6 × 42µV/2.5V) with the DAC gain of 1. We are trying purposefully to keep the noise calculations simple here; a more detailed analysis can be performed if the relative error of the noise is larger or if the design is marginal. Remember that noise is specified as a typical value when judging design margin.

We will now review the relevant MAX5304 DAC specifications that impact accuracy at or near the upper end of the code range. The DAC INL value of ±4LSB (at 10 bits) is used directly. Treating it as a single-sided quantity, as with the other error terms in our analysis, we arrive at a value of 3906ppm (10^6 × 4/1024). Similarly, the DAC gain error is specified as ±2LSB and results in an error of 1953ppm (10^6 × 2/1024). The final MAX5304 DAC specification to be considered is gain-error tempco, which gives us a typical error of 70ppm (70°C × 1ppm/°C). The DAC output noise is not specified for the MAX5304, so it is ignored, most likely without adverse consequences in this 6-bit-accurate system.

When all of the error sources are added together, we obtain a worst-case error of 15596ppm, which just barely meets our target-error specification of 15625ppm. When confronted with this marginal situation, we can rationalize that we will probably never see an error of this magnitude, because it assumes worst-case conditions for most parameters. The root sum square (RSS) approach gives an error of 7917ppm, which is valid if the errors are uncorrelated. Some error sources may be correlated, so the truth probably lies somewhere between these two numbers. But regardless of the approach, the Design-A requirements have been met.

Design B: High Accuracy and Precision

The initial error of the A-grade MAX6225 is 0.04% or 400ppm, which exceeds Design B's entire 122ppm error budget. Because this application has gain calibration, virtually all of this reference initial error can be removed, assuming the calibration equipment has sufficient (~1µV) accuracy and the trim circuit has enough precision. The tempco contribution is calculated as 70ppm (70°C × 1ppm/°C), and the typical temperature hysteresis value of 20ppm is used directly. The long-term stability specification of 30ppm is also used rather than a more conservative number, because the instrument in this application has an initial burn-in as well as an annual calibration.

Applying the same assumptions that were used in Design A, we find Design B's reference output current

variation to be 140µA (coincidentally, the same number as in Design A). This leads to the following load-regulation-error calculation:

Load-Regulation Error = 140µA × 6ppm / mA ~= 1ppm (max)

The power supply is specified as being constant in this application, so the line regulation is assumed to be 0ppm. Note that it would be <1ppm even if the power supply weren't constant, as long as it remained within the specified 4.95V to 5.05V range, because the MAX6325 line-regulation specification is 7ppm/V max.

Because the bandwidth for Design B is specified as DC to 1kHz, we need to consider both the 1.5µVp-p low-frequency (1/f) noise and the 2.8μV_{RMS} broadband noise specified from 0.1Hz to 10Hz and 10Hz to 1kHz, respectively. Using the same crude RMS to peak approximation as Design A, and adding the two peak noise terms together, we get a total noise estimate of 2ppm at the reference output ([[0.75µV + 2.8μV_{RMS} × √2]/2.5V] × 10^6). Notice that this is the same value we would obtain if we calculated it at the DAC output, because the equation would be multiplied by 1.638/1.638 to rescale everything to 4.096V. It's worth mentioning that the peak-noise-sum method used here is fairly conservative, yet the total error contribution is still relatively small. An RSS approach is probably more accurate, because the two noise sources are most likely uncorrelated, but this smaller value would be even more "in the noise" (pun intended) compared to the peak-value approach.

All that remains for the Design-B analysis is to include the DAC error terms. The INL for the A-grade MAX5170 DAC is specified as ±1LSB, which is 61ppm and exactly half of our 122ppm error budget of ±2LSB at 14 bits. The DAC gain error is specified as ±8LSB worst-case, but this error is removed completely by the gain calibration mentioned earlier. The calibration works as follows: The DAC is set to a digital code where the ideal output voltage is known (for example, decimal DAC code 16380 should produce precisely 4.095V at the output). The reference voltage is then trimmed until the DAC output voltage is at this exact value, even if the reference voltage itself is not 2.500V. The MAX5170 DAC does not list a gain tempco, although the gain error is specified over the operating-temperature range. Because the gain error is calibrated out at only one temperature, Design B should be tested to ensure that the gain does not drift excessively over temperature. The final consideration is the MAX5170 DAC output noise, whose typical peak noise is roughly estimated as 1ppm ([10^6 × √(1000Hz × π/2) × 80nV_{RMS}/√Hz × √2]/4.096V).

In the end, the final worst-case accuracy is 184ppm (~ ±3LSB at 14 bits), which doesn't quite meet our accuracy target of 122ppm, whereas the RSS accuracy is acceptable at 100ppm. Based on these numbers, we consider the design a success, because it has illustrated the important points and is close to the target accuracy with several conservative assumptions. In a real-world application, this design could be accepted as is, or the accuracy requirements could be loosened slightly. Alternatively, a more expensive reference could be used if this design were not acceptable.

Design C: One-Time Calibrated, Low Drift

The initial error of the A-grade MAX6162 is 0.1%, which consumes the entire Design-C error budget of 977ppm. However, like Design B, this is (at least partially) calibrated out. Note that the uncalibrated +4.096V MAX5154 DAC full-scale output voltage exceeds the required +4.000V output range, and the DAC has 1mV resolution even though only ±4mV of accuracy is required. Therefore, it is possible to do a "digital calibration" on the DAC input digital codes to remove some of the reference's initial error and the DAC's gain error.

The digital gain calibration is best demonstrated with an example: Assume the DAC output voltage needs to be at the full-scale value of 4.000V, but the ideal decimal DAC code of 4000 results in a measured output of only 3.997V due to various errors in the system. Using digital calibration, a correction value is added to the DAC code to produce the desired result. In this example, when the DAC output voltage of 4.000V is required, a corrected DAC code of 4003 is used instead of 4000. This gain calibration is scaled linearly across the DAC codes, so it has little effect at the lower codes and more impact on the upper codes.

The digital gain calibration accuracy is limited by the 12-bit resolution of the DAC, so the best we can hope for is ~ ±1mV or 244ppm (10^6 × 1mV/4.096V) of error after the calibration has been applied. Note that the accuracy is calculated on a 4.096V scale in this example to maintain consistency, but it could be calculated relative to the +4.000V output range if required by the application, and the error would be slightly higher.

If the required output range in this example were 4.096V, there are other options that could be used to always bias the uncalibrated DAC output voltage above 4.096V, so that the digital gain calibration scheme described in this example could be employed. Such options include the following:

- Using an adjustable reference whose output is always above 4.096V when all circuit tolerances are considered
- Using a force/sense DAC with the gain set slightly higher than necessary
- Adding an output buffer with gain

The MAX6162 reference tempco error is calculated as 625ppm (125°C × 5ppm/°C), and the typical temperature hysteresis value of 80ppm is used directly. The long-term-stability specification is doubled to a more conservative 160ppm, because no burn-in is specified for the application and it is never calibrated once it leaves the factory.

We find Design C's worst-case reference output current variation to be 293µA (2.5V/[14kΩ||14kΩ], remember there are two DACs driven by the reference), which is used directly in the load-regulation calculation:

Load-Regulation Error = 293µA × 0.9mV / mA = 264µV (max)

= 10^6 × 264µV / 2.048V = 129ppm (max)

Because reference-load regulation is proportional to the reference output voltage, it can be calculated at either the voltage reference (264µV/2.048V) or the DAC output ((2 × 264µV)/(2 × 2.048V)).

The power supply is constant in this application, so the line regulation is assumed to be 0ppm. With the bandwidth for Design C specified as 0.1Hz to 10Hz, we use half of the 22µVp-p low-frequency (1/f) noise specification (peak value) to arrive at a noise contribution of 5ppm at the reference output (10^6 × (22µV/2)/2.048V)). As mentioned previously, we get the same 5ppm answer if the calculation is referred to the DAC output, because the equation is just multiplied by 2.0/2.0.

Moving on to the MAX5154 DAC error terms, the A-grade INL is ±0.5LSB, which is 122ppm on the 12-bit scale. The DAC gain error is ±3LSB(244ppm), but it is ignored because it was already accounted for in the digital reference/DAC gain calibration mentioned earlier in this step and we don't want to count it twice. The MAX5154 gain-error tempco has a typical value of 4ppm/°C, which gives us a total of 500ppm (125°C × 4ppm/°C). The DAC output noise is not specified for the MAX5154, so it is ignored. We recognize that this could present a problem, but our experience with Design B indicates that DAC noise is usually a relatively small contributor to the total error. Measurements can be performed to confirm this assumption.

The worst-case error for Design C is calculated as 1865ppm, and the RSS error is 874ppm. With a target-error specification of 977ppm, the current design is marginally acceptable at best, especially given that some typical values were used and the DAC output noise was not considered. The details of Design C will not be rehashed here, because the important points have already been covered. However, some options for improvement are as follows:

- Use the MAX6191 instead of the MAX6162, because it has better load regulation (0.55µV/µA versus 0.9mV/mA), temperature hysteresis (75ppm versus 80ppm), and long-term stability (50ppm versus 80ppm). The end result would be a 1750ppm worst-case error and an 858ppm RSS error, which is a net change of 115ppm and 16ppm, respectively. This is a slight improvement, but may not be enough.
- Re-examine the overall system-accuracy specifications to determine if any parameters can be relaxed. The existing design could be the best choice in terms of accuracy versus cost.
- Reduce the temperature range if the entire extended range is not needed. For example, if the range can be reduced from -40°C to +85°C down to -10°C to +75°C, the worst-case error drops to 1505ppm and the RSS error becomes 648ppm. This is because much of the error budget is consumed by the reference tempco (625ppm) and the DAC gain error tempco (500ppm). Although only one of these error terms is below the 977ppm target, the comfort level is increased considerably compared to the original MAX5154/MAX6162 design.
- If an 8V or greater supply is available, consider the MAX6241 4.096V reference and the MAX5156 DAC (the force/sense version of the MAX5154) set to unity gain. This combination is slightly more expensive, but it produces an approximate worst-case error of 956ppm and an RSS error of 576ppm, both of which

are under the 977ppm total-error target.
- Consider other DACs that have typical gain tempcos as low as 1ppm/°C.

Design D: Low Voltage, Battery Powered, Moderate Accuracy

No calibration or trimming is planned for Design D, so the A-grade MAX6190 initial error of 1600ppm (10^6 × 2mV/1.25V) is used directly in the error budget, along with 150ppm (30°C × 5ppm/°C) for the tempco error. The 75ppm temperature hysteresis is also used directly, but the risk of using this typical specification is at least partially offset by the reduced operating-temperature range (15°C to 45°C). Once again, the 1000-hour long-term stability is doubled to 100ppm as a conservative estimate of the drift, as there is no burn-in in this application.

The load-regulation error is again calculated from the assumed worst-case MAX5176 DAC reference input current of 69µA:

Load-Regulation Error = 69µA × 0.5µV / µA = 34.5µV (max)

= 10^6 × 34.5µV / 1.25V = 28ppm (max)

The power supply varies between 2.7V and 3.6V in this design, so the MAX6190 line-regulation specification of 80µV/V (max) must be included in the analysis:

Line-Regulation Error = (3.6V - 2.7V) × 80µV / V = 72µV (max)

= 10^6 × 72µV / 1.25V = 58ppm (max)

As with Design C, the bandwidth for Design D is specified as 0.1Hz to 10Hz, so we use half of the 25µVp-p low-frequency (1/f) noise specification to arrive at a peak noise contribution of 10ppm at the reference output (10^6 × [12.5µV/1.25V]). We expect the same 10ppm-reference-induced noise term at the DAC output, because the reference voltage and noise see the same DAC gain.

Focusing now on the MAX5176 DAC error terms, the A-grade INL is ±2LSB, which is 488ppm on the 12-bit scale. The DAC worst-case gain error of +/-8LSB with a 5kΩ load translates to 1953ppm at 12 bits. Like the MAX5170 in Design B, the MAX5176 does not specify a gain-error tempco. This is not a concern in Design D, because it is not a low-drift design calibrated at one temperature and the maximum DAC gain error is specified over the entire operating-temperature range. The final consideration is the MAX5176's DAC output noise, whose estimated typical peak value is assumed to be negligible ([10^6 × (√10Hz × π/2) × 80nV_{RMS}/√Hz × √2]/2.048V) ~ = 0.22ppm).

As with Designs B and C, the worst-case error of 4462ppm exceeds the 3906ppm target error, whereas the 2580ppm RSS error is well below the target. Based on these numbers, Design D is considered to be successful, because it comfortably meets the requirements from an RSS standpoint and has demonstrated the important design concepts. If further improvement is desired, alternative DACs should be considered first, because the MAX6190 is the best low-power voltage reference available with an output below 1.3V (caused by the VDD - 1.4V limitation on DAC reference inputs) and such low quiescent current (35µA).

DAC Voltage-Reference Design Summary

This article has demonstrated a design procedure for DAC voltage-reference selection involving the following steps:

Step 1. Voltage Ranges and Reference-Voltage Determination: The power-supply voltage and the DAC output-voltage range were used to determine viable reference-voltage and DAC gain options.

Step 2. Initial Voltage-Reference Device-Selection Criteria: Candidate voltage references were considered, focusing on reference voltage (determined in Step 1), initial accuracy, tempco, and reference output current. From these candidates, an initial device was selected.

Step 3. Final Specification Review and Error-Budget Analysis: The selected voltage-reference and DAC

candidates were evaluated using an error-budget approach to see if they met the design's overall accuracy requirements. To meet the design goals, iteration between Steps 2 and 3 may be required.

When following the design procedure described above, it's convenient to do the error analysis in ppm and to understand how it relates to other system-accuracy and error measures (Table 6).

Table 6. Accuracy and Error Ranges

± LSB Accuracy (Bits)	±1LSB Error (ppm)	±1LSB Error (%)	16-Bit Error (LSB)	14-Bit Error (LSB)	12-Bit Error (LSB)	10-Bit Error (LSB)	8-Bit Error (LSB)	6-Bit Error (LSB)
16	15	0.0015	1	0.25	<0.25	<0.25	<0.25	<0.25
15	31	0.0031	2	0.5	<0.25	<0.25	<0.25	<0.25
14	61	0.0061	4	1	0.25	<0.25	<0.25	<0.25
13	122	0.0122	8	2	0.5	<0.25	<0.25	<0.25
12	244	0.0244	16	4	1	0.25	<0.25	<0.25
11	488	0.0488	32	8	2	0.5	<0.25	<0.25
10	977	0.0977	64	16	4	1	0.25	<0.25
9	1953	0.1953	128	32	8	2	0.5	<0.25
8	3906	0.3906	256	64	16	4	1	0.25
7	7812	0.7812	512	128	32	8	2	0.5
6	15625	1.5625	1024	256	64	16	4	1
5	31250	3.1250	2048	512	128	32	8	2
4	62500	6.2500	4096	1024	256	64	16	4

The following tables show existing Maxim three-terminal, series voltage references, along with the specifications used in the design procedure. Specifications that contribute to error are expressed in ppm to ease computations and to allow an apples-to-apples comparison between voltage references. Voltage references of 3V and below (1.2V, 1.25V, 2.048V, 2.5V, and 3.0V) are shown in Table 7, and those above 3V (4.096V, 4.5V, 5V, 10V) are included with the adjustable references in Table 8. For convenience, the devices in both tables are grouped together by reference voltage and listed roughly in order of increasing price.

Table 7. Maxim Series Voltage References and Key Specifications (VREF <= 3.0V)

Voltage References	V_{OUT}(V)	Max Initial Accuracy (ppm)	Max Tempco (ppm/°C)	Typ Temp Hysteresis (ppm)	Typ Long-Term Stability (ppm)	Max Sourcing Load Reg (ppm/µA)	Max Line Reg (ppm/V)	Typ LF/HF Peak Output Noise (ppm)
MAX6120	1.20	10,000	100	N/S	N/S	0.83	25	4/167
MAX6520	1.20	10,000	50	N/S	N/S	0.83	25	4/167
MAX6001	1.25	10,000	100	130	50	0.64	96	10/74
MAX6101	1.25	4000	75	130	50	0.72	72	5/17
MAX6012	1.25	3200-4800	15-30	130	50	0.40	64	10/74
MAX6190	1.25	1600-4800	5-25	75	50	0.4	64	10/74
MAX6061	1.25	4000-5600	20-30	130	62	0.72	200	5/17
MAX6161	1.25	1600-3200	5-10	80	80	0.72	48	8/17
MAX6021	2.048	2400- 3900	15-30	130	50	0.27	49	10/73
MAX6191	2.048	1000-4800	5-25	75	50	0.27	49	10/73
MAX6062	2.048	2400-3900	20-30	130	62	0.44	63	5/17
MAX6162	2.048	1000-2400	5-10	80	80	0.44	63	5/15
MAX6002	2.5	10,000	100	130	50	0.36	80	12/71
MAX6102	2.5	4000	75	130	50	0.36	120	5/17
MAX6125	2.5	10,000	50	N/S	N/S	0.40	20	5/140
MAX6025	2.5	2000-4000	15-30	130	50	0.24	56	12/71
MAX6192	2.5	800-4000	5-25	75	50	0.24	56	12/71
MAX6066	2.5	2000-4000	20-30	130	62	0.36	88	5/17
MAX873	2.5	600-5600	7-20	N/S	20	0.02	6	3/8
MAX6166	2.5	800-2000	5-10	80	80	0.36	88	5/17
MAX872	2.5	2000	40	N/S	N/S	0.24	120	12/N/S
MAX6225	2.5	400-1200	2-8	20	20	0.015	5-45	0.3/0.7
MX580	2.5	4000-30000	10-85	N/S	10	0.4	16-94	12/N/S
MAX6325	2.5	400	1-2.5	20	30	0.015	5-45	0.3/0.7
MAX6003	3.0	10,000	100	130	50	0.30	73	13/71
MAX6103	3.0	4000	75	130	50	0.30	133	6/19
MAX6030	3.0	2000-4000	15-30	130	50	0.2	50	13/71
MAX6193	3.0	700-3300	5-25	75	50	0.20	50	13/71
MAX6063	3.0	2000-4000	20-30	130	62	0.3	100	6/19
MAX6163	3.0	700-1700	5-10	80	80	0.30	100	6/19

LF = Low frequency
HF = High frequency
N/S = Not specified

Table 8. Maxim Series Voltage References and Key Specifications (VREF > 3.0V and Adj)

Voltage References	V_{OUT} (V)	Max Initial Accuracy (ppm)	Max Tempco (ppm/°C)	Typ Temp Hysteresis (ppm)	Typ Long-Term Stability (ppm)	Max Sourcing Load Reg (ppm/µA)	Max Line Reg (ppm/V)	Typ LF/HF Peak Output Noise (ppm)
MAX6004	4.096	10,000	100	130	50	0.24	59	12/69
MAX6104	4.096	4000	75	130	50	0.22	105	6/17
MAX6141	4.096	10,700	50	N/S	N/S	0.39	12	3/85
MAX6041	4.096	2000-3900	15-30	130	50	0.17	39	12/69
MAX6198	4.096	500-2400	5-25	75	50	0.17	39	12/69
MAX6064	4.096	2000-3900	20-30	130	62	0.22	73	6/17
MAX6164	4.096	500-1200	5-10	80	80	0.22	73	6/17
MAX874	4.096	2000	40	N/S	N/S	0.24	18	11/N/S
MAX6241	4.096	244-1000	2-8	20	20	0.009	5-45	0.3/0.7
MAX6341	4.096	244	1-2.5	20	30	0.009	5-45	0.3/0.7
MAX6145	4.5	10,000	50	N/S	N/S	0.40	11	3/89
MAX6045	4.5	2000-4000	15-30	130	50	0.18	36	12/68
MAX6194	4.5	400-2200	5-25	75	50	0.18	36	12/68
MAX6067	4.5	2000-4000	20-30	130	62	0.20	100	6/17
MAX6167	4.5	400-1100	5-10	80	80	0.20	100	6/17
MAX6005	5.0	1000	100	130	50	0.20	48	12/68
MAX6105	5.0	4000	75	130	50	0.18	110	6/17
REF02	5.0	3000-10000	8.5-250	N/S	N/S	0.10-0.40	100-400	2/N/S
MAX6150	5.0	10,000	50	N/S	N/S	0.40	10	4/90
MAX6050	5.0	2000-4000	15-30	130	50	0.17	32	12/68
MAX6195	5.0	400-2200	5-25	75	50	0.17	32	12/68
MAX6065	5.0	2000-4000	20-30	130	62	0.18	80	6/17
MAX875	5.0	400-2400	7-20	N/S	20	0.02	6	3/8
MAX6165	5.0	400-1000	5-10	80	80	0.18	80	6/17
MAX6250	5.0	200-1000	2-8	20	20	0.009	5-45	0.3/0.7
MAX675	5.0	1400	12-20	N/S	N/S	0.02	100	1.5/N/S
MAX6350	5.0	200	1-2.5	20	30	0.009	5-45	0.3/0.7
REF01	10.0	3000-10000	8.5-65	N/S	N/S	0.08-0.15	100-150	2/N/S
MAX876	10.0	300-2500	7-20	N/S	20	0.02	6	3/8
MX581	10.0	500-3000	10-30	N/S	25	0.05	20-50	2.5/N/S
MAX674	10.0	1500	12-20	N/S	N/S	0.02	100	1.5/N/S
MAX6160	Adj	10,000	100	N/S	N/S	0.40	20	3/100
MX584	2.5-10	1000-3000	15-30	N/S	25	0.03 typ	20-50	10/N/S

LF = Low frequency
HF = High frequency
N/S = Not specified

Some voltage references are available as a family of parts with different output reference voltages. It's important to note that, within a given family, some specifications in the data sheet can get worse for devices with increasing output voltage. However, when these specifications are viewed relative to the reference voltage, they can remain constant or even improve with increasing voltage. One example is output noise voltage, which generally increases with output voltage because of the higher internal reference gain needed to amplify the ~1.25V bandgap voltage. Although the noise voltage is higher, the reference voltage is also proportionally higher; thus, relative noise measures, such as the ppm results in the tables above, are roughly constant. Another example is the load- and line-regulation specifications (µV/µA and µV/V, respectively), which usually worsen in absolute terms with increasing output voltage. When viewed relative to the reference voltage (in ppm/µA and ppm/V), these specifications normally remain flat or actually improve with increasing output voltage.

Key Points

These are the key points in this article:

- The system designer often has multiple reference-voltage and DAC gain choices to satisfy a given DAC output-voltage range.
- Consider *all* error sources, not just initial error (which is important in some designs but not critical for others, such as those with gain calibration).
- Reference and DAC tempcos can be major error contributors. Check the actual required operating-temperature range, because slight reductions can decrease the error contribution from these parameters significantly.
- A common trade-off is the higher price of a reference with tight initial accuracy versus the trimming cost in product manufacturing.
- Examine the accuracy requirements carefully to make sure they are correct before selecting unnecessary, more expensive components or reworking a design that has marginal performance. It is generally very difficult (and expensive) to achieve a high level of absolute accuracy, especially at 12 bits and above.
- Worst-case or RSS analysis can be used to quantify the error, but it's ultimately up to the designer to determine if a given design is accurate enough.

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