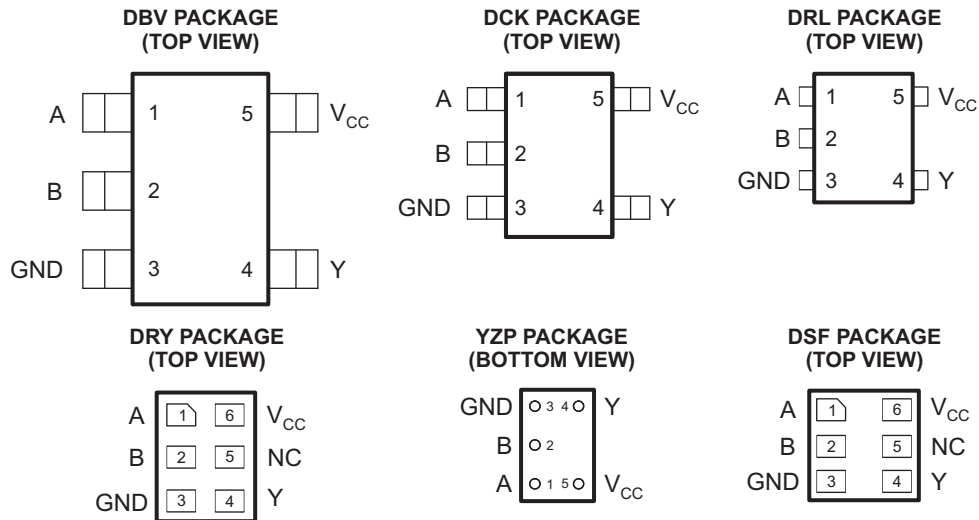


SINGLE 2-INPUT POSITIVE-AND GATE

Check for Samples: [SN74LVC1G08](#)

FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 3.6 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



NC – No internal connection
See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The SN74LVC1G08 performs the Boolean function or $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G08YZPR	__ _CE_
	SON – DSF	Reel of 5000	SN74LVC1G08DSFR	CE
	SON – DRY	Reel of 5000	SN74LVC1G08DRYR	CE
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G08DBVR	C08_
		Reel of 250	SN74LVC1G08DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G08DCKR	CE_
		Reel of 250	SN74LVC1G08DCKT	
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G08DRLR	

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

Table 1. FUNCTION TABLE

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

LOGIC DIAGRAM (POSITIVE LOGIC)

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	6.5	V
V _I	Input voltage range ⁽²⁾	–0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ^{(2) (3)}	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		–50 mA
I _{OK}	Output clamp current	V _O < 0		–50 mA
I _O	Continuous output current			±50 mA
	Continuous current through V _{CC} or GND			±100 mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DBV package		206
		DCK package		252
		DRL package		142
		DRY package		234
		YZP package		132
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		SN74LVC1G08					UNITS
		DBV	DCK	DRL	DRY	YZP	
		5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	207.6	283.1	242.9	438.8	130	°C/W
θ _{JCTop}	Junction-to-case (top) thermal resistance	145.2	92.3	77.5	276.8	54	
θ _{JB}	Junction-to-board thermal resistance	53.5	60.9	77.5	271.7	51	
ψ _{JT}	Junction-to-top characterization parameter	37.5	1.7	9.6	83.8	1	
ψ _{JB}	Junction-to-board characterization parameter	53.1	60.1	77.3	271.4	50	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	–	–	–	–	–	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 3 V to 3.6 V	2	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 3 V to 3.6 V	0.8	
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}	
V _I	Input voltage	0	5.5	V

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions⁽¹⁾ (continued)

		MIN	MAX	UNIT
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65\text{ V}$	–4	mA
		$V_{CC} = 2.3\text{ V}$	–8	
		$V_{CC} = 3\text{ V}$	–16	
		$V_{CC} = 4.5\text{ V}$	–24	
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$	–32	mA
		$V_{CC} = 2.3\text{ V}$	4	
		$V_{CC} = 3\text{ V}$	8	
		$V_{CC} = 4.5\text{ V}$	16	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$	24	ns/V
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	32	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	20	
T_A	Operating free-air temperature	–40	85	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 5.5 V	V _{CC} – 0.1			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.9			
		I _{OH} = –16 mA	3 V	2.4			
		I _{OH} = –24 mA		2.3			
		I _{OH} = –32 mA	4.5 V	3.8			
V _{OL}		I _{OL} = 100 µA	1.65 V to 5.5 V	0.1			V
		I _{OL} = 4 mA	1.65 V	0.45			
		I _{OL} = 8 mA	2.3 V	0.3			
		I _{OL} = 16 mA	3 V	0.4			
		I _{OL} = 24 mA		0.55			
		I _{OL} = 32 mA	4.5 V	0.55			
I _I	A or B inputs	V _I = 5.5 V or GND	0 to 5.5 V	±5			µA
I _{off}		V _I or V _O = 5.5 V	0	±10			µA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V	10			µA
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500			µA
C _i		V _I = V _{CC} or GND	3.3 V	4			pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1.5	7.2	0.7	4.4	0.8	3.6	0.8	3.4	ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

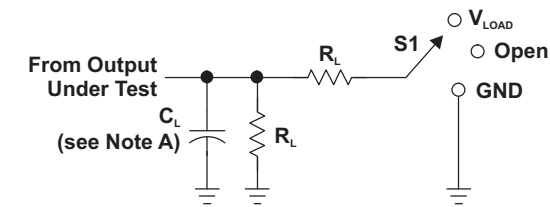
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	2.4	8	1.1	5.5	1	4.5	1	4	ns

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	f = 10 MHz	21	24	26	31	pF

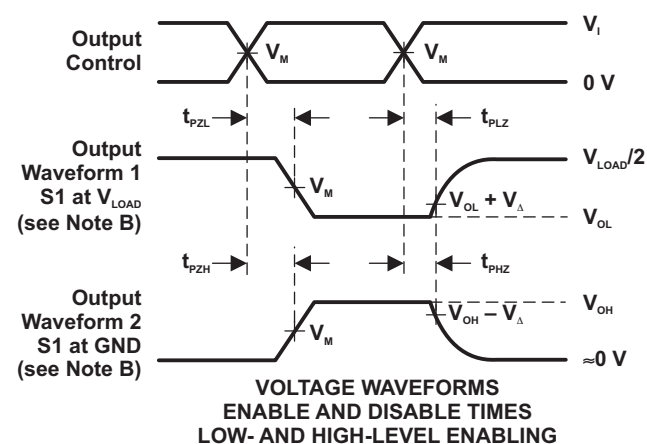
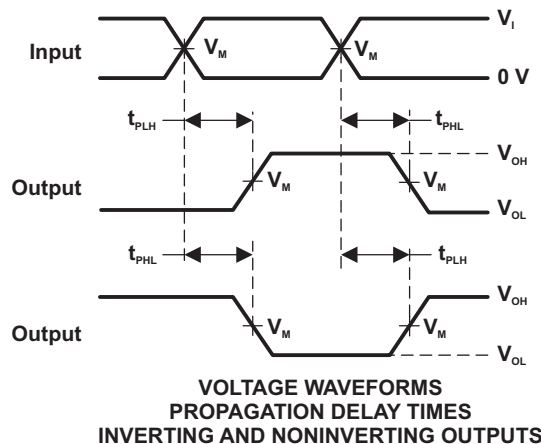
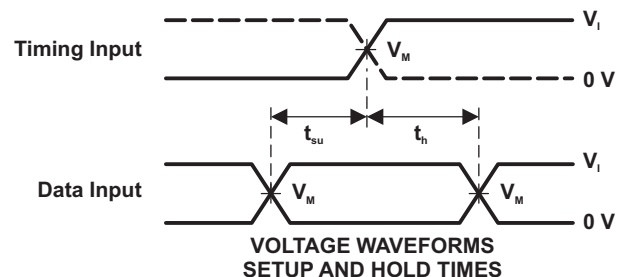
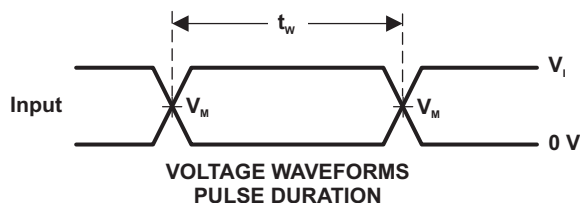
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

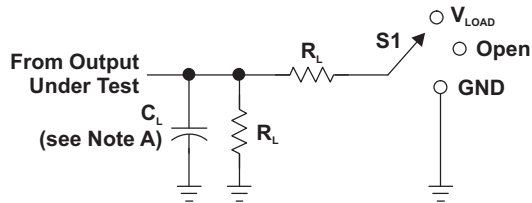
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

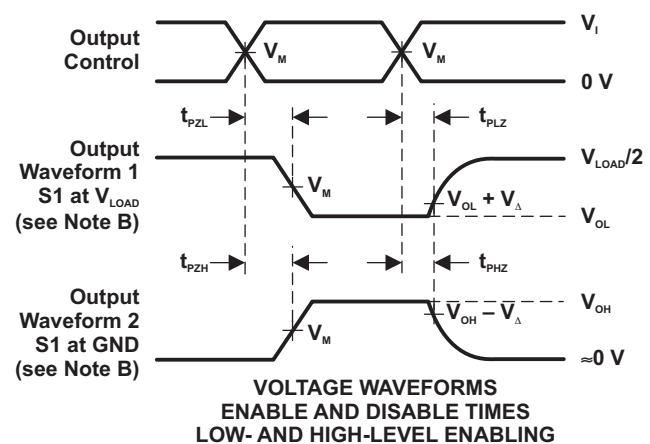
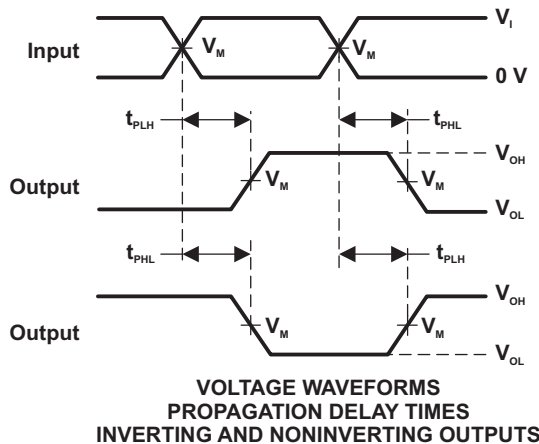
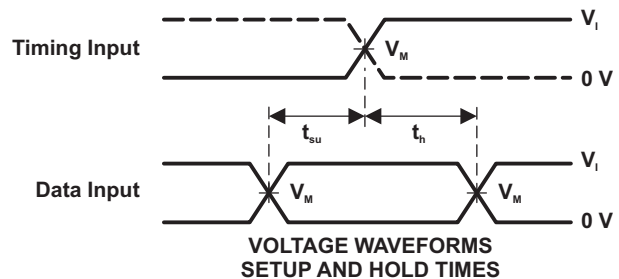
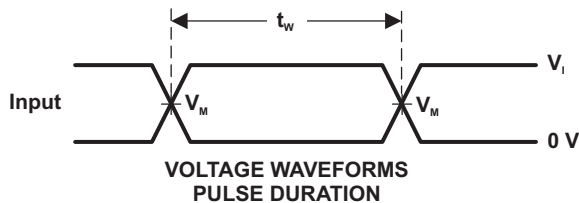
PARAMETER MEASUREMENT INFORMATION (continued)



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_i	t_i/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision T (February 2007) to Revision U	Page
• Added Thermal Information table.	3

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LVC1G08DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G08DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LVC1G08YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G08 :

- Automotive: [SN74LVC1G08-Q1](#)
- Enhanced Product: [SN74LVC1G08-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

-
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G08DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G08DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G08DBVT	SOT-23	DBV	5	250	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G08DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G08DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08DCKT	SC70	DCK	5	250	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74LVC1G08DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G08DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74LVC1G08YZPR	DSBGA	YZP	5	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G08YZPR	DSBGA	YZP	5	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

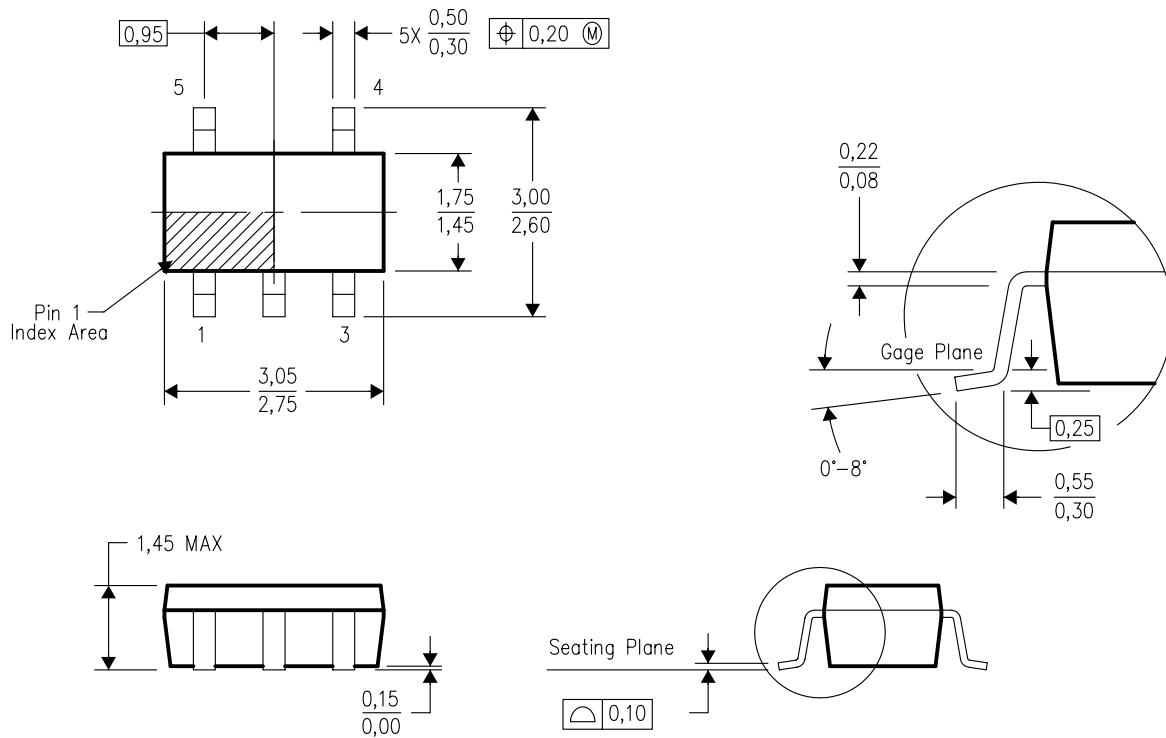


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G08DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G08DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74LVC1G08DBVT	SOT-23	DBV	5	250	205.0	200.0	33.0
SN74LVC1G08DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G08DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G08DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G08DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G08DRYR	SON	DRY	6	5000	203.0	203.0	35.0
SN74LVC1G08DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74LVC1G08YZPR	DSBGA	YZP	5	3000	190.5	212.7	31.8
SN74LVC1G08YZPR	DSBGA	YZP	5	3000	220.0	220.0	34.0

DBV (R-PDSO-G5)

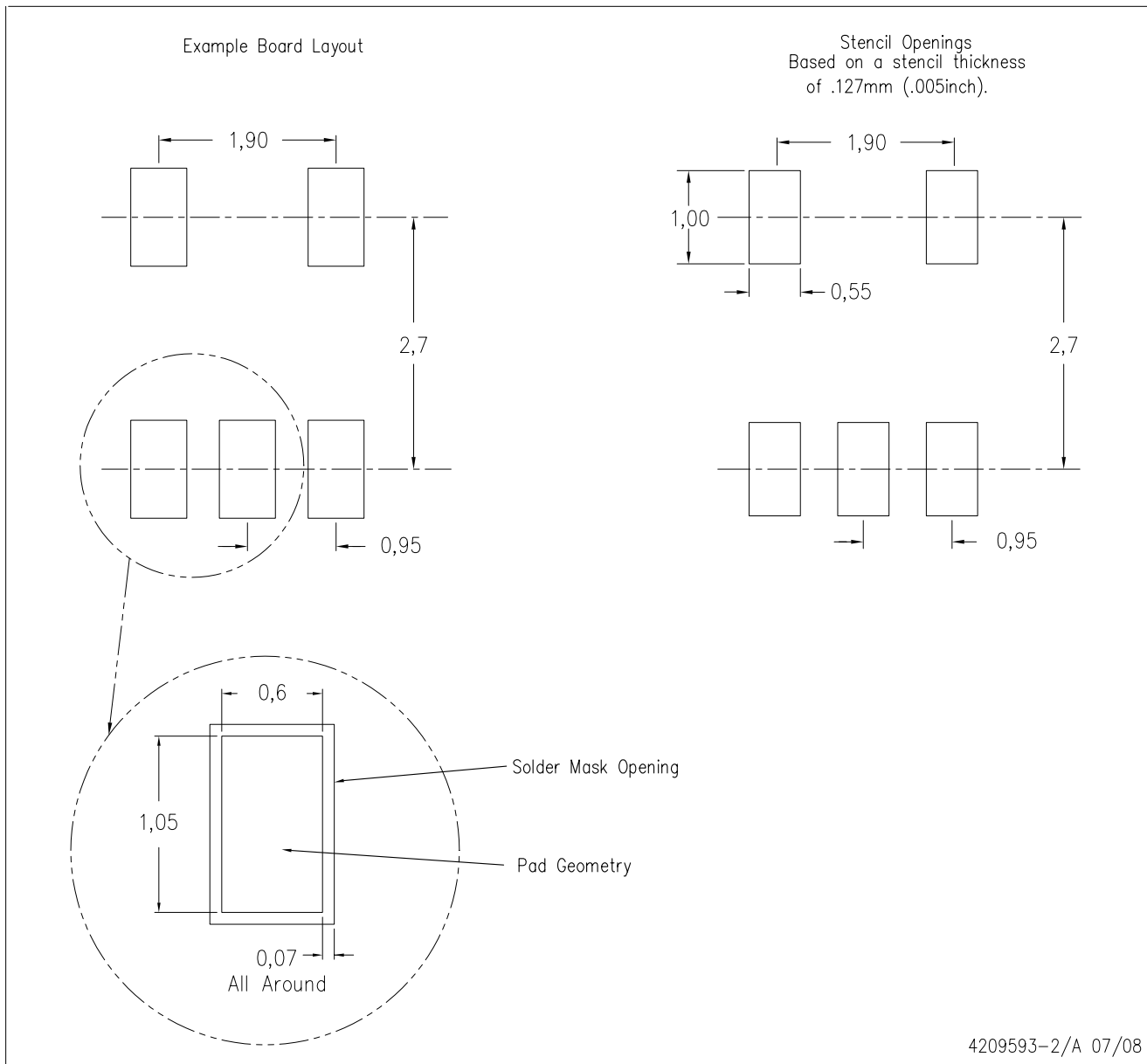
PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

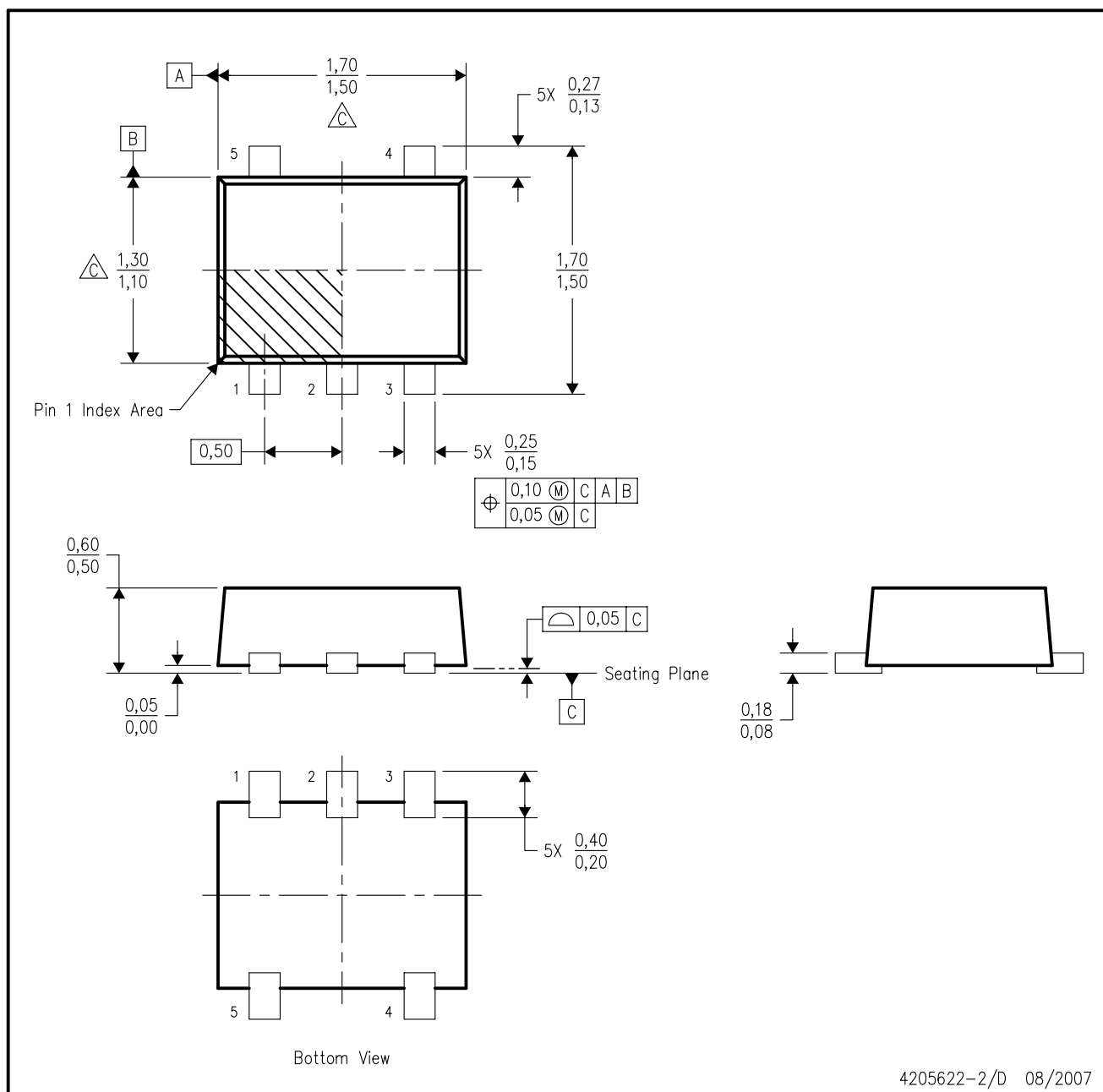
DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

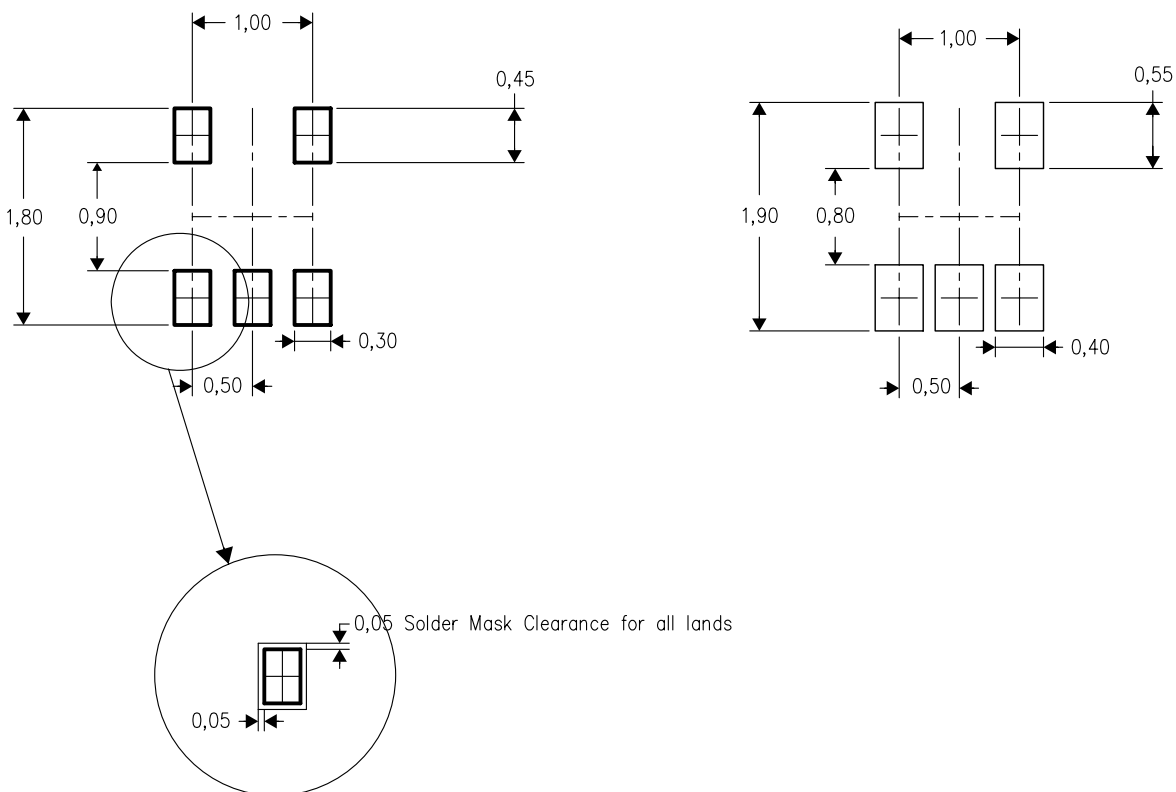
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.



4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

DRL (R-PDSO-N5)

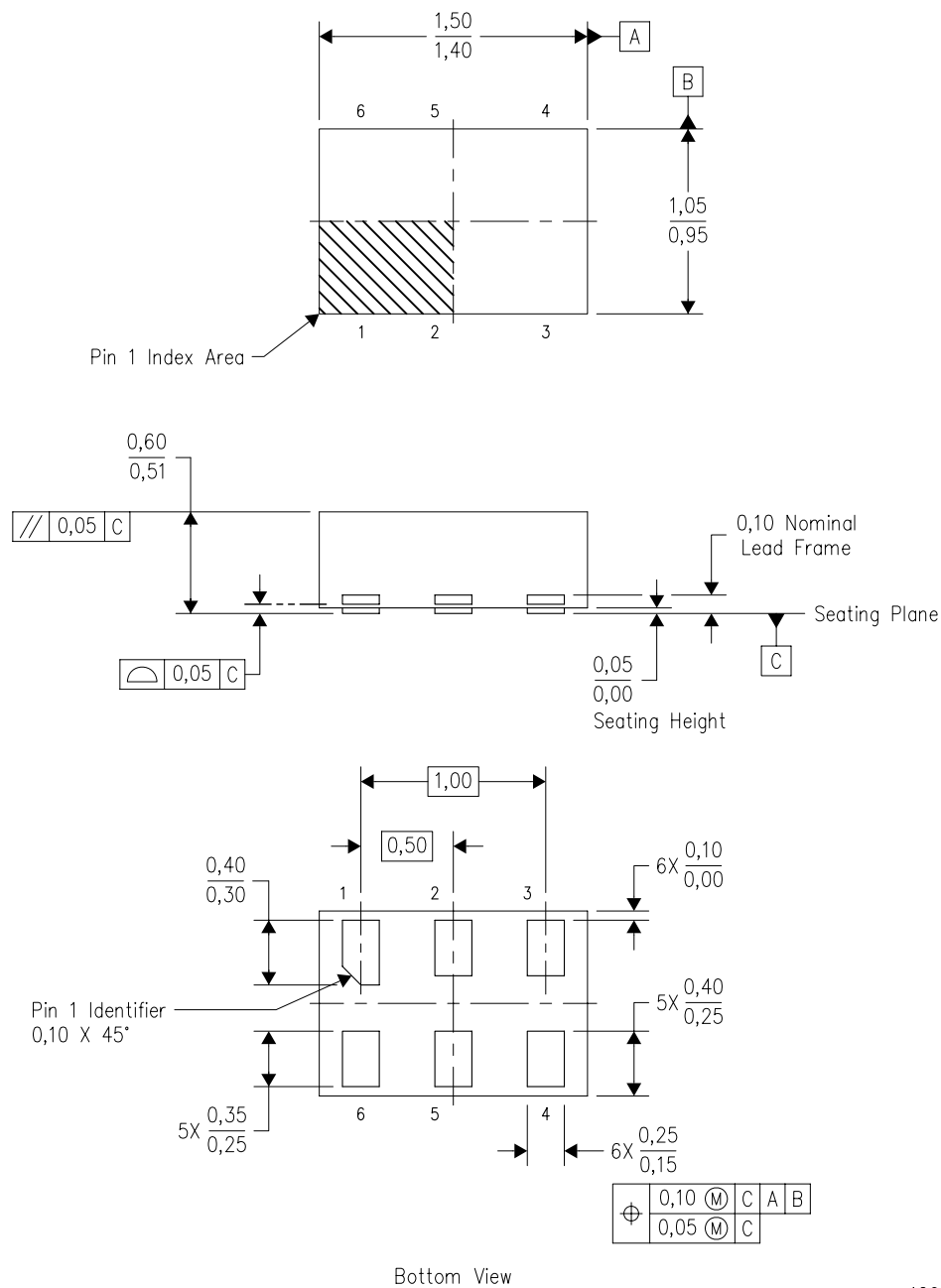


4208207-2/A 09/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

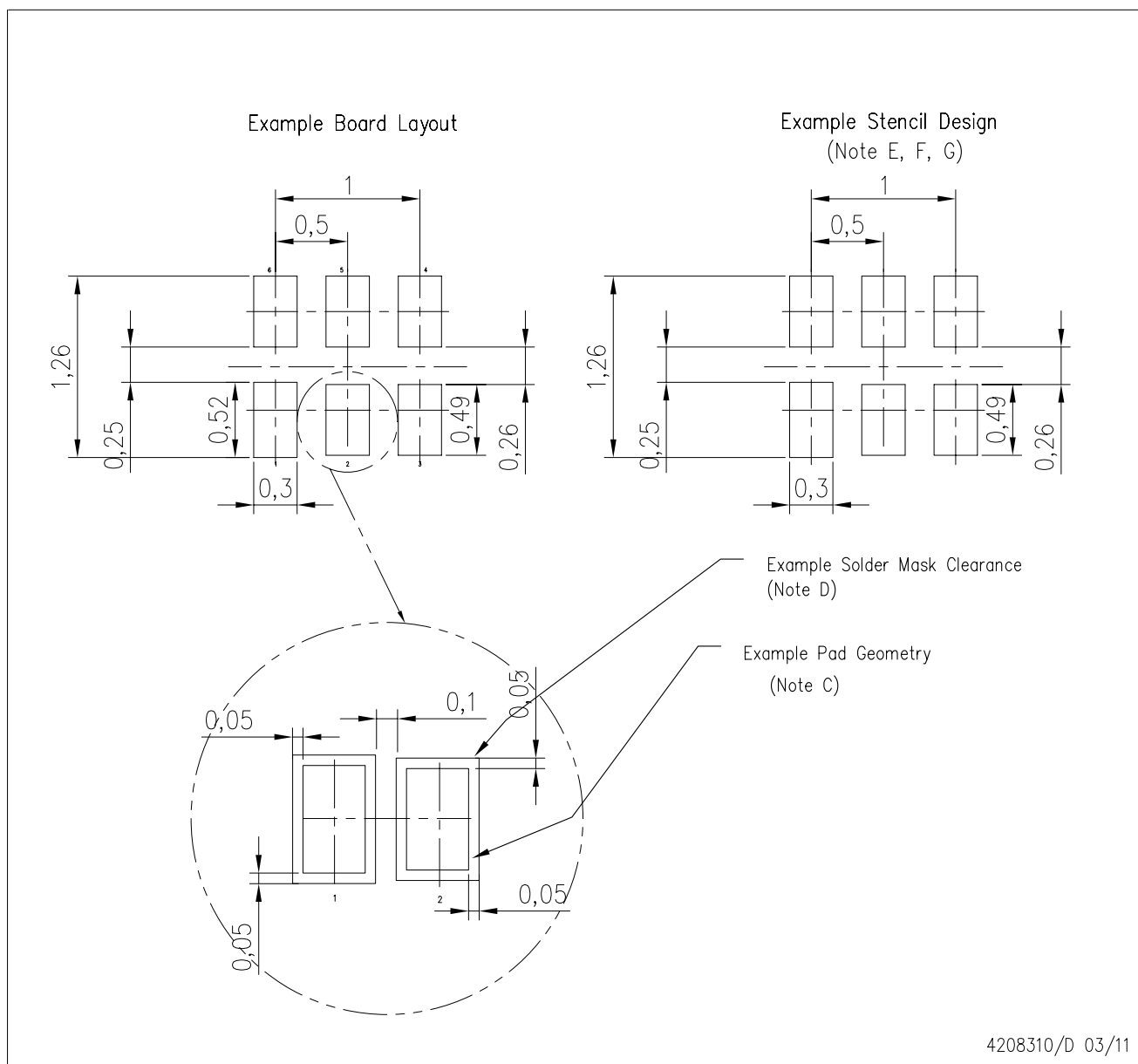


4207181/D 12/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - D. This package complies to JEDEC MO-287 variation UFAD.

DRY (S-PUSON-N6)

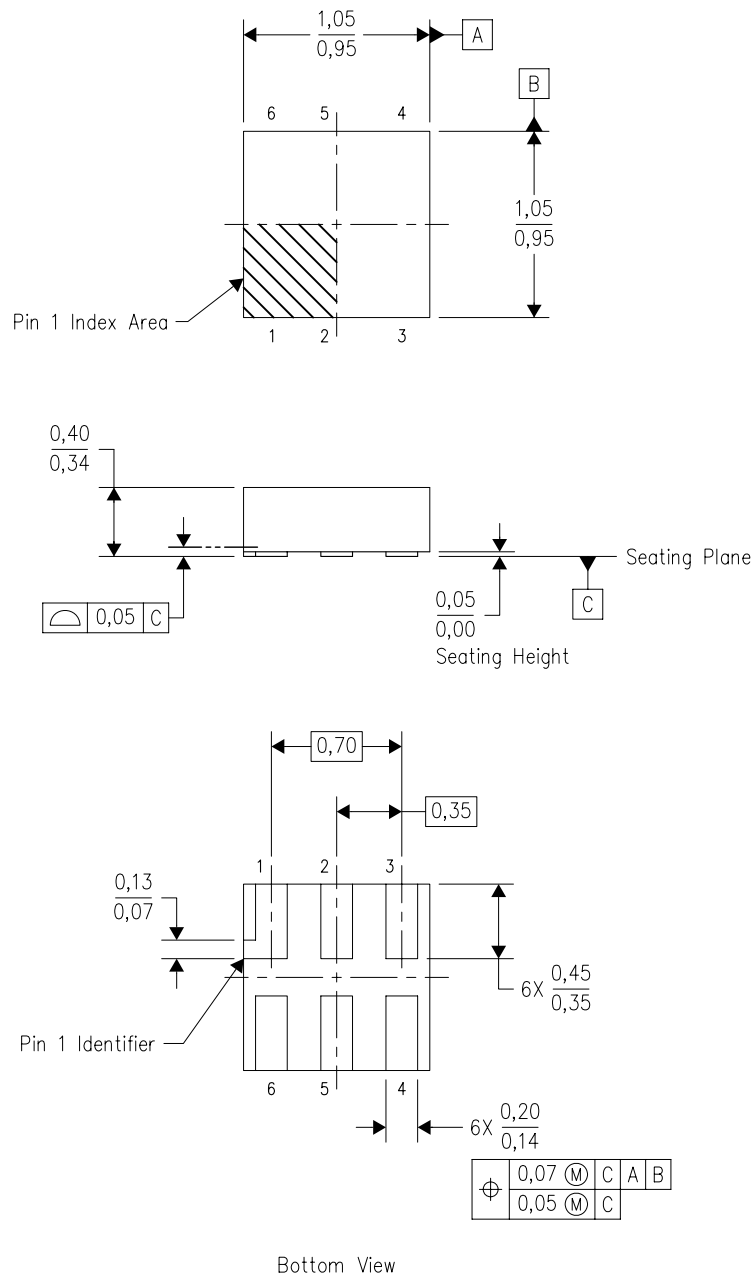
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

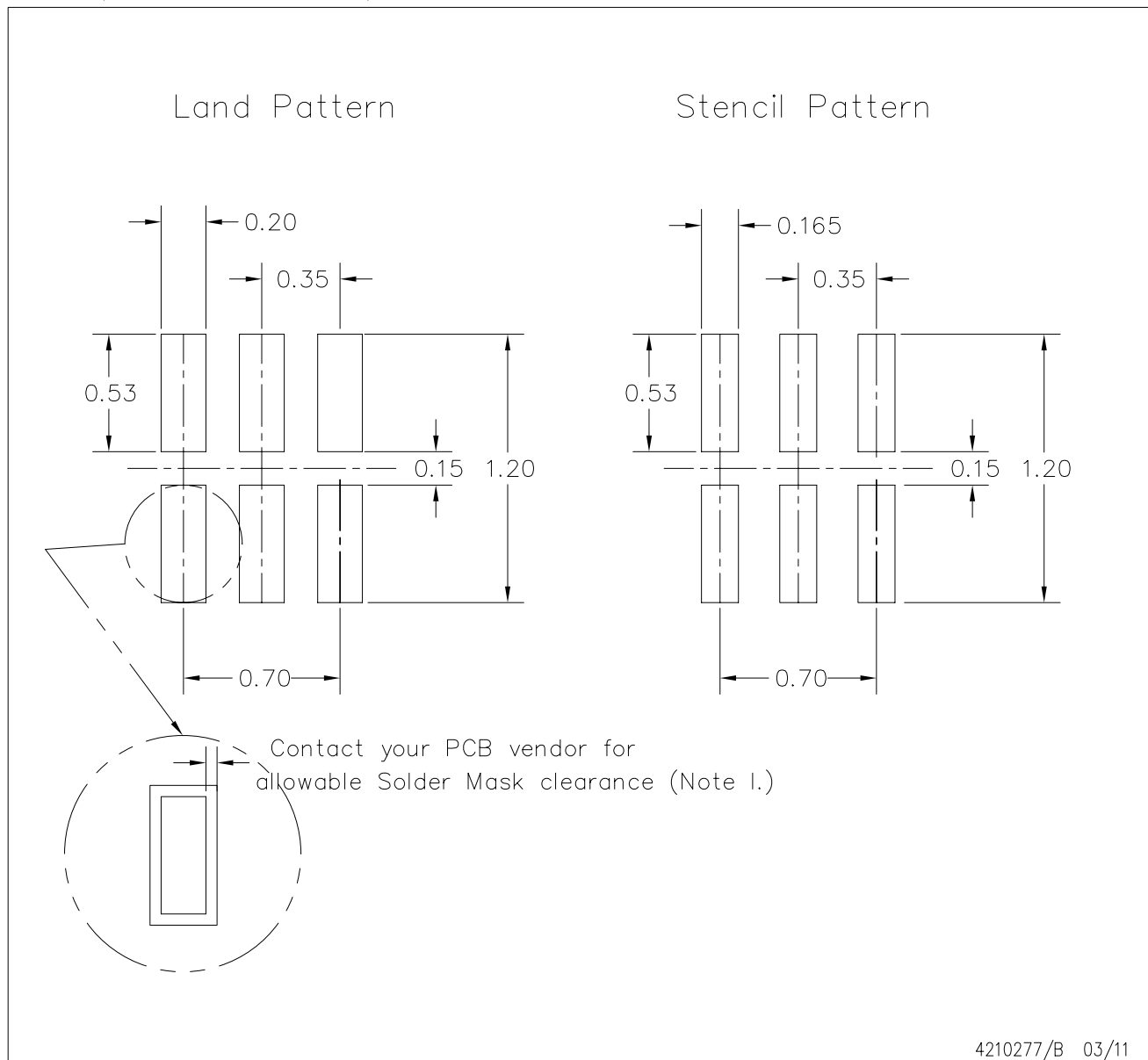


4208186/E 03/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - D. This package complies to JEDEC MO-287 variation X2AAF.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

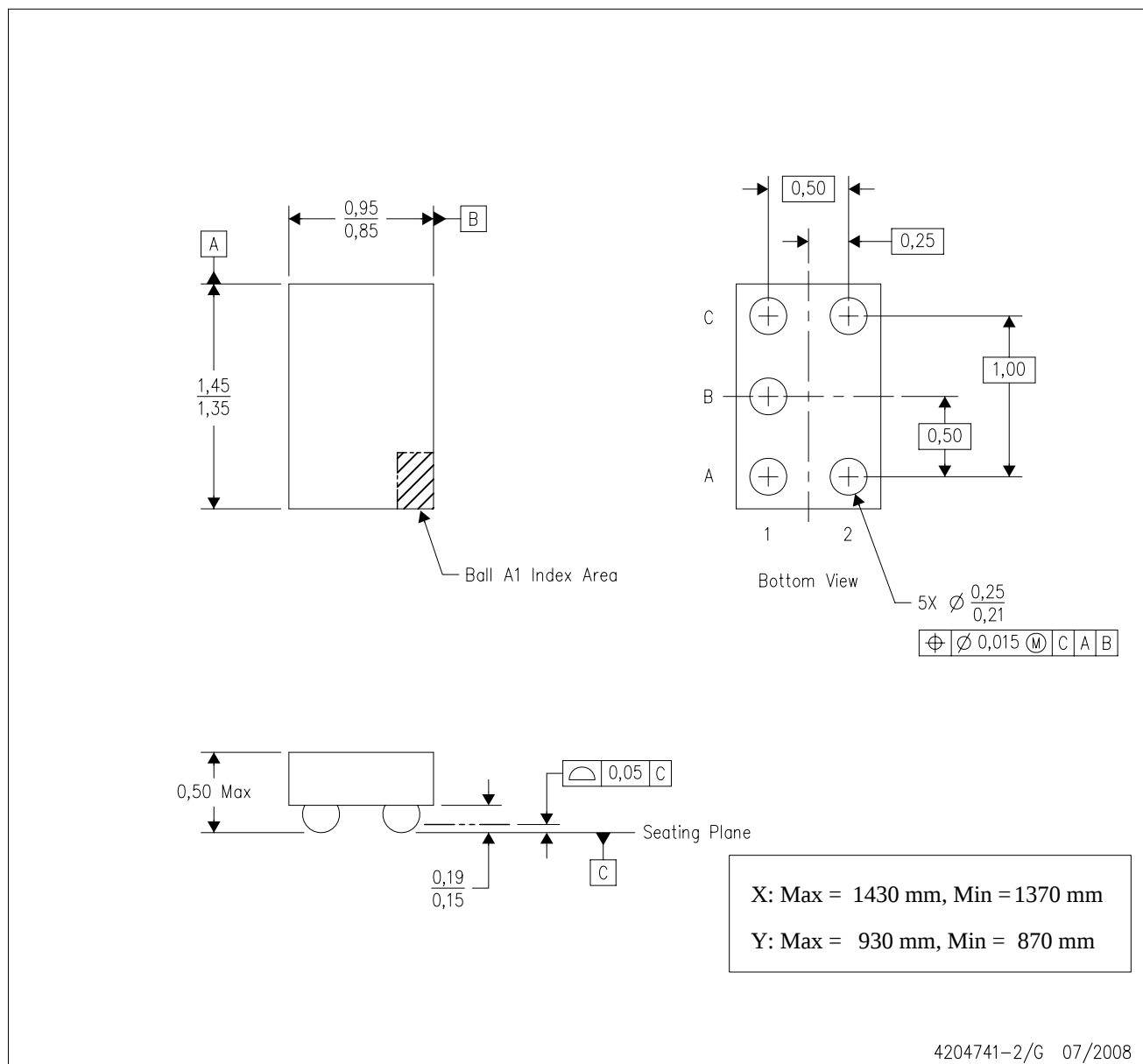


4210277/B 03/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 - Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Over-printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
 - Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 - Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video
Wireless	www.ti.com/wireless-apps

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated