

PIC24FJ64GA104 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ64GA104 family devices that you have received conform functionally to the current Device Data Sheet (DS39951B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ64GA104 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (A2).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICKit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICKit™ 3.
2. From the main menu in MPLAB IDE, select Configure>Select Device, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (Debugger>Select Tool).
4. Perform a "Connect" operation to the device (Debugger>Connect). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ64GA104 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾
		A2
PIC24FJ32GA102	4202h	0002h
PIC24FJ32GA104	420Ah	
PIC24FJ64GA102	4206h	
PIC24FJ64GA104	420Eh	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the "PIC24FJ64GA1/GB0 Families Flash Programming Specification" (DS39934) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾
				A2
Output Compare	Cascaded mode	1.	Cascaded mode does not work as expected.	X
UART	Break Character Generation	2.	Will not generate back-to-back Break characters.	X
Oscillator	Secondary Oscillator Configuration	3.	High-current draw when external signal applied under certain conditions.	X
SPI	Master mode	4.	Spurious transmission and reception of null data on wake-up from Sleep (Master mode).	X
SPI	Master mode	5.	Inaccurate SPITBF flag with high clock divider.	X
Triple (Enhanced) Comparator	—	6.	No interrupt generation with internal band gap reference.	X
Core	Doze Mode	7.	Instruction execution glitches following DOZE bit changes.	X
A/D	—	8.	Disabled voltage references during Debug mode.	X
Interrupts	INTx	9.	External interrupts missed when writing to INTCON2.	X
Oscillator	—	10.	POSCEN bit does not work with Primary + PLL modes	X
A/D Converter	—	11.	Excessive Sleep current when module is enabled.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Output Compare (Cascaded Mode)

When using Cascaded (32-bit) mode, Trigger and Synchronous modes do not work as expected. The even numbered module does not become synchronized to the odd numbered module, resulting in errors in the Most Significant 16 bits of the output. In certain modes, the even numbered module does not generate any output. This behavior is independent of the OCTRIG trigger/sync selection for the even numbered module.

Work around

None.

Affected Silicon Revisions

A2							
X							

2. Module: UART

The UART module will not generate consecutive Break characters. Trying to perform a back-to-back Break character transmission will cause the UART module to transmit the dummy character used to generate the first Break character instead of transmitting the second Break character. Break characters are generated correctly if they are followed by non-Break character transmission.

Work around

None.

Affected Silicon Revisions

A2							
X							

3. Module: Oscillator (Secondary Oscillator Configuration)

Under certain circumstances, applying voltages to the comparator inputs, C2INC and C2IND (SOSCO/RA4 and SOSCI/RB4, respectively), may cause the microcontroller's current draw to increase. This happens only when all of the following conditions are met:

- RA4 and RB4 are configured to function as digital I/O, rather than as Secondary Oscillator pins (SOSCSEL<1:0> = 00);
- the pins are configured as digital inputs (TRIS<4> and TRISB<4> = 1); and
- the voltage applied to the pins approaches 1/2 VDD.

This occurs regardless of the signal source; a comparator input voltage or a digital clock input of sufficient amplitude will have the same result.

Work around

If it is necessary to use RA4 and RB4 as comparator inputs, C2INC and C2IND, program the SOSCSEL Configuration bits (CW3<9:8>) for one of the oscillator modes, rather than digital I/O (SOSCSEL<1:0> = 11 or 01).

Affected Silicon Revisions

A2							
X							

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4. Module: SPI (Master Mode)

When operating in Enhanced Buffer Master mode, the module may transmit two bytes or two words of data, with a value of 0h, immediately upon the microcontroller waking up from Sleep mode. At the same time, the module “receives” two words or two bytes of data, also with the value of 0h.

The transmission of null data occurs even if the Transmit Buffer registers are empty prior to the microcontroller entering Sleep mode. The received null data requires that the receive buffer be read twice to clear the “received” data.

This behavior has not been observed when the module is operating in any other mode.

Work around

When operating in Enhanced Buffer Master mode, disable the module (SPIEN = 0) before entering Sleep mode.

Affected Silicon Revisions

A2							
X							

5. Module: SPI (Master Mode)

When operating in Enhanced Buffer Master mode, the Transmit Buffer Full flag, SPITBF, may be cleared before all data in the FIFO buffer has actually been set. This may result in data being overwritten before it can be sent.

This has only been observed when the SPI clock prescalers are configured for a divider of greater than 1:4.

This behavior has not been observed when the module is operating in any other mode.

Work around

Several options are available:

- If possible, use a total clock prescale factor of 1:4 or less.
- Do not use SPITBF to indicate when new data can be written to the buffer. Instead, use the SPIRBF or SPIBEC flags to track the number of bytes actually transmitted.
- If the SPITBF flag must be used, always wait at least one-half SPI clock cycle before writing to the transmit buffer.

Affected Silicon Revisions

A2							
X							

6. Module: Triple (Enhanced) Comparator

When any of the internal band gap options (VBG, VBG/2 or VBG/6) are selected by the voltage reference module as the comparator's CVREF-input, the comparator may not generate an interrupt when a preprogrammed event is detected.

The CVREF+ input works as previously described.

Work around

If it is necessary to use the internal band gap as a reference, do the following:

1. Enable the comparator's output (CMCON<14> = 1), and map the output to an available remappable output pin.
2. Connect this pin to any other available pin that supports either external interrupt or interrupt-on-change notification.
3. Monitor the second pin for an interrupt event.

Affected Silicon Revisions

A2							
X							

7. Module: Core (Doze Mode)

Operations that immediately follow any manipulations of the DOZE<2:0> or DOZEN bits (CLKDIV<14:11>) may not execute properly. In particular, for instructions that operate on an SFR, data may not be read properly. Also, bits automatically cleared in hardware may not be cleared if the operation occurs during this interval.

Work around

Always insert a NOP instruction before and after either of the following:

- enabling or disabling Doze mode by setting or clearing the DOZEN bit
- before or after changing the DOZE<2:0> bits

Affected Silicon Revisions

A2							
X							

8. Module: A/D Converter

When using PGEC3 and PGED3 to debug an application, all voltage references will be disabled. This includes VREF+, VREF-, AVDD and AVSS. Any A/D conversion will always equal 03FFh.

Work around

Use either PGEC1/PGED1 or PGEC2/PGED2 to debug any A/D functionality.

Affected Silicon Revisions

A2							
X							

9. Module: Interrupts (INTx)

Writing to the INTCON2 register may cause an external interrupt event (inputs on INT0 through INT2) to be missed. This only happens when the interrupt event and the write event occur during the same clock cycle.

Work around

If this cannot be avoided, write the data intended for INTCON2 to any other register in the interrupt block of the SFR (addresses 0080h to 00E0h); then write the data to INTCON2.

Be certain to write the data to a register not being actively used by the application, or to any of the interrupt flag registers, in order to avoid spurious interrupts. For example, if the interrupts controlled by IEC4 are not being used in the application, the code sequence would be:

```
IEC4 = 0x1E;
```

```
INTCON2 = 0x1E;
```

```
IEC4 = 0;
```

It is the user's responsibility to determine an appropriate register for the particular application.

Affected Silicon Revisions

A2							
X							

10. Module: Oscillator

The POSCEN bit (OSCCON<2>) has no effect when a Primary Oscillator with PLL mode is selected (COSC<2:0> = 011). If XTPLL, HSPLL or ECPLL Oscillator mode are selected and the device enters Sleep mode, the Primary Oscillator will be disabled, regardless of the state of the POSCEN bit.

XT, HS and EC Oscillator modes (without the PLL) will continue to operate as expected.

Work around

None.

Affected Silicon Revisions

A2							
X							

11. Module: A/D Converter

The microcontroller's Sleep current may exceed previously published specifications if the A/D module is enabled. IPD may remain increased even if the module is later disabled (AD1CON1<15> = 0).

Work around

In addition to disabling the module through the ADON bit, set the corresponding PMD bit (ADC1MD, PMD1<0>) to power it down completely.

Disabling the A/D module through the PMD register also disables the AD1PCFG registers, which in turn, affects the state of any port pins with analog inputs. Users should consider the effect on I/O ports and other digital peripherals on those ports when ADC1MD is used for power conservation.

Affected Silicon Revisions

A2							
X							

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39951**B**):

Note: Corrections are shown in bold . Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2009)

Initial release of this document; issued for revision A2. Includes silicon issues 1 (Output Compare – Cascaded Mode), 2 (Power-Saving Modes – Sleep Mode) and 3 (UART).

Rev B Document (12/2009)

Deletes silicon issue 2 (Power-Saving Modes – Sleep Mode); subsequent issues re-numbered accordingly.

Adds new silicon issues 3 (Oscillator – Secondary Oscillator Configuration), 4-5 (SPI – Master Mode), 6 (Triple (Enhanced) Comparator) and 7 (Core – Doze Mode) to silicon revision A2.

Rev C Document (8/2010)

Adds new silicon issues 8 (A/D Converter), 9 (Interrupts – INTx), 10 (Oscillator) and 11 (A/D Converter) to silicon revision A2.

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NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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