Extending the SPI bus for long-distance communication

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The serial peripheral interface (SPI) bus is an unbalanced or single-ended serial interface designed for short-distance communication between integrated circuits. Typically, a master device exchanges data with one or multiple slave devices. The data exchange is full-duplex and requires synchronization to an interface clock signal. However, recent trends in the design of industrial data-acquisition systems have not taken this synchronization requirement into account, and distances between the microcontroller and the corresponding analog-to-digital and digital-to-analog converters (ADCs and DACs) can reach 100 m or more.

The impact of the added propagation delay on the data-to-clock synchronicity is often ignored, and interface designs that operate perfectly in the lab environment cease operation when implemented on the factory floor. There can be multiple reasons for the interface malfunction. This article tries to shed light on the major ones, including:

- Lack of synchronization due to large propagation delays of the signal path
- Reduced noise immunity due to long-distance, unbalanced signal paths
- Damaged transceivers due to large ground-potential differences (GPDs)
- Data transmission errors due to unterminated data lines
- Transceiver latch-up and network downtime due to large electrical transients

Synchronicity

An SPI primarily uses three interface lines:

- An interface clock initiated by the master device to ensure synchronous data transfers
- A data line for data sent from the master to a slave
- A data line for data sent from a slave to the master

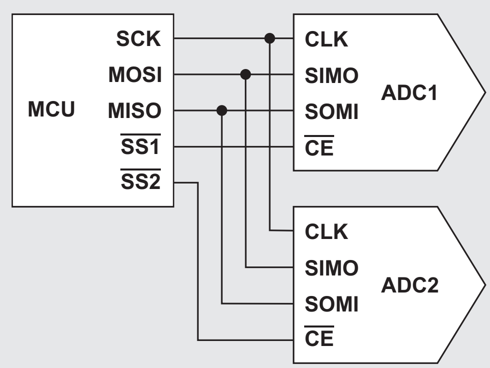
A fourth wire that carries what is known as the slave-select signal is not required for controlling interface flow but is needed for addressing a specific slave out of a range of slave devices. Figure 1a shows a simplified schematic of a microcontroller unit (MCU) operating as the master that controls two data converters representing the slaves.

With byte lengths ranging from 8 to 12 bits and multiples thereof, and data rates ranging from 1 to 20 Mbps, the standard SPI configuration allows for short propagation times and hence only short distances in order to maintain synchronicity between the interface clock and the data transmitted in both directions. Figure 1b shows the interface timing of the first three data bits when the SPI is configured to change data at the rising clock edge and to sample data at the falling clock edge.

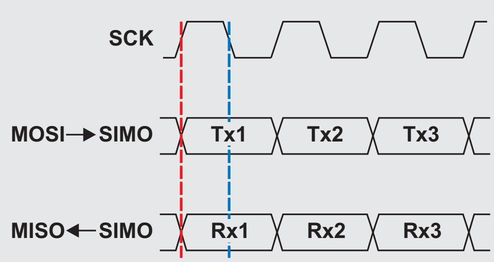
Over long distances, however, the transmission cable introduces significant propagation delay into the signal path. Assuming a typical signal velocity of 5 ns/m, a 100-m cable will cause a propagation delay of 500 ns. Because the data sent from the master to the slave experiences the same delay as the master-initiated interface clock, both will remain in sync across the entire data link. In the opposite direction, however, the slave sends data to the master only when the first clock edge reaches the slave. Furthermore, this data will experience a second delay on its way back to the master, so the slave data will be out of sync by twice the cable's propagation delay.

Of course, communicating across a 100-m cable won't be possible without appropriate line drivers and receivers. These components will further increase the propagation delay by about another 50 ns, for a total of 550 ns. The slave data will therefore lag behind the first clock edge by a total of 1100 ns, or 11 bits when a data rate of 10 Mbps is assumed.

Figure 1. Simplified schematic of an SPI



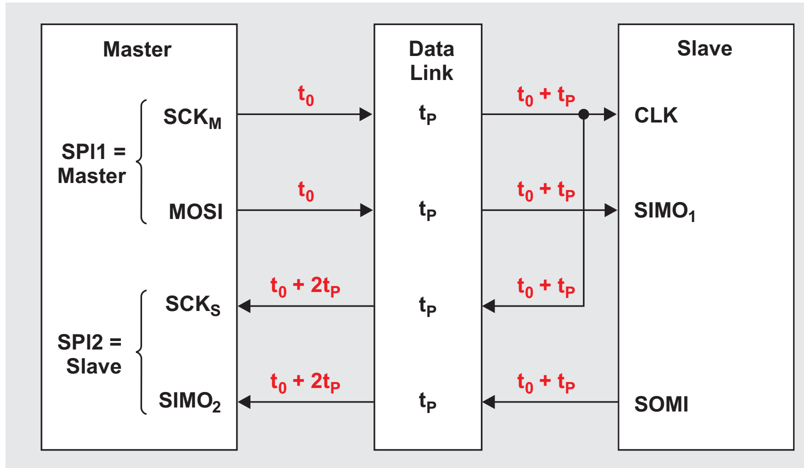
(a) MCU master controlling two slaves



(b) Timing of first three data bits

The only possible solution for restoring synchronicity between the slave data and the interface clock while maintaining a high data rate is to feed the clock signal from the slave back to the master. Figure 2 clarifies the benefit of clock feedback. Here t_0 represents the first rising clock edge, or the start of a data transmission, and t_P is the data-link propagation delay. After traversing the data link, both the master clock (SCK_M) and the master data (MOSI) remain in sync. Feeding back the master clock signal synchronizes the clock with the slave data so that both arrive equally delayed at the master. The only requirement is that the master provide two independent SPI ports, one configured as a master (SPI1) and the other configured as a slave (SPI2). Most modern microcontrollers possess two or more SPI ports, so this requirement poses no problem.

Figure 2. Clock-feedback path restores synchronicity



Nevertheless, implementing a long-distance, SPI-compatible interface in the real world is not a trivial task. Long-distance data links are always subject to external noise sources, ground-potential differences (GPDs), voltage and current surges due to inductive load switching, and often even reflections due to wrong or no termination. The flowing schematic in Figure 3 (see next page) tries to cover all of these aspects by showcasing the various transceiver and protection circuits that can counteract the derogating effects.

Increasing noise immunity

Unbalanced or single-ended drivers and receivers are inadequate for accomplishing a robust data link over long distances, as they are susceptible to common-mode noise. An excellent method to eliminate common-mode noise in a synchronous, full-duplex interface such as an SPI is the use of RS-422 differential driver and receiver circuits in combination with twisted-pair cable.

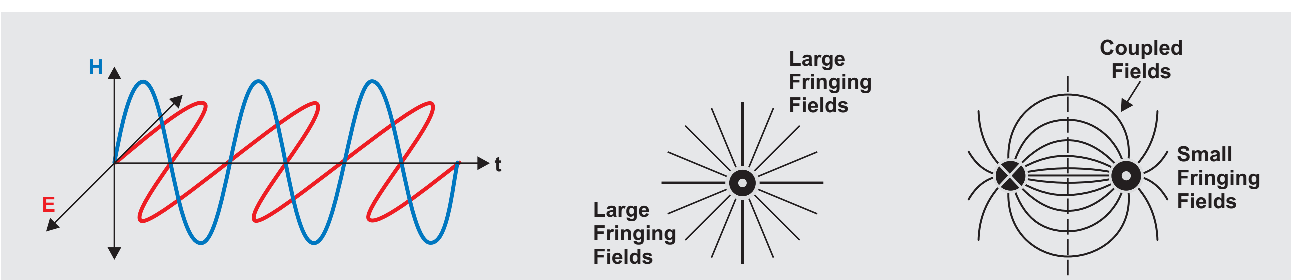
Because the conductors of twisted-pair cable are closely electrically coupled, external noise induced equally into both conductors appears as common-mode noise at the receiver input. Although differential receivers are sensitive to signal differences, they are immune to common-mode signals. The receiver therefore rejects common-mode noise, and signal integrity is maintained.

Another benefit of close electric coupling is that the currents in the two conductors create magnetic fields that cancel each other. The initial transversal electromagnetic (TEM) waves of the two conductors are therefore largely reduced to electric fields that cannot radiate into the environment (see Figure 4). Only the far smaller fringing fields outside the conductor loop can radiate, thus yielding much lower electromagnetic interference (EMI).

Eliminating ground loops and GPDs

While the RS-485 and RS-422 standards specify that a data link without a ground wire can be operated with a GPD of up to ±7 V, it is advisable not to assume that these values

Figure 4. TEM-wave radiation effects

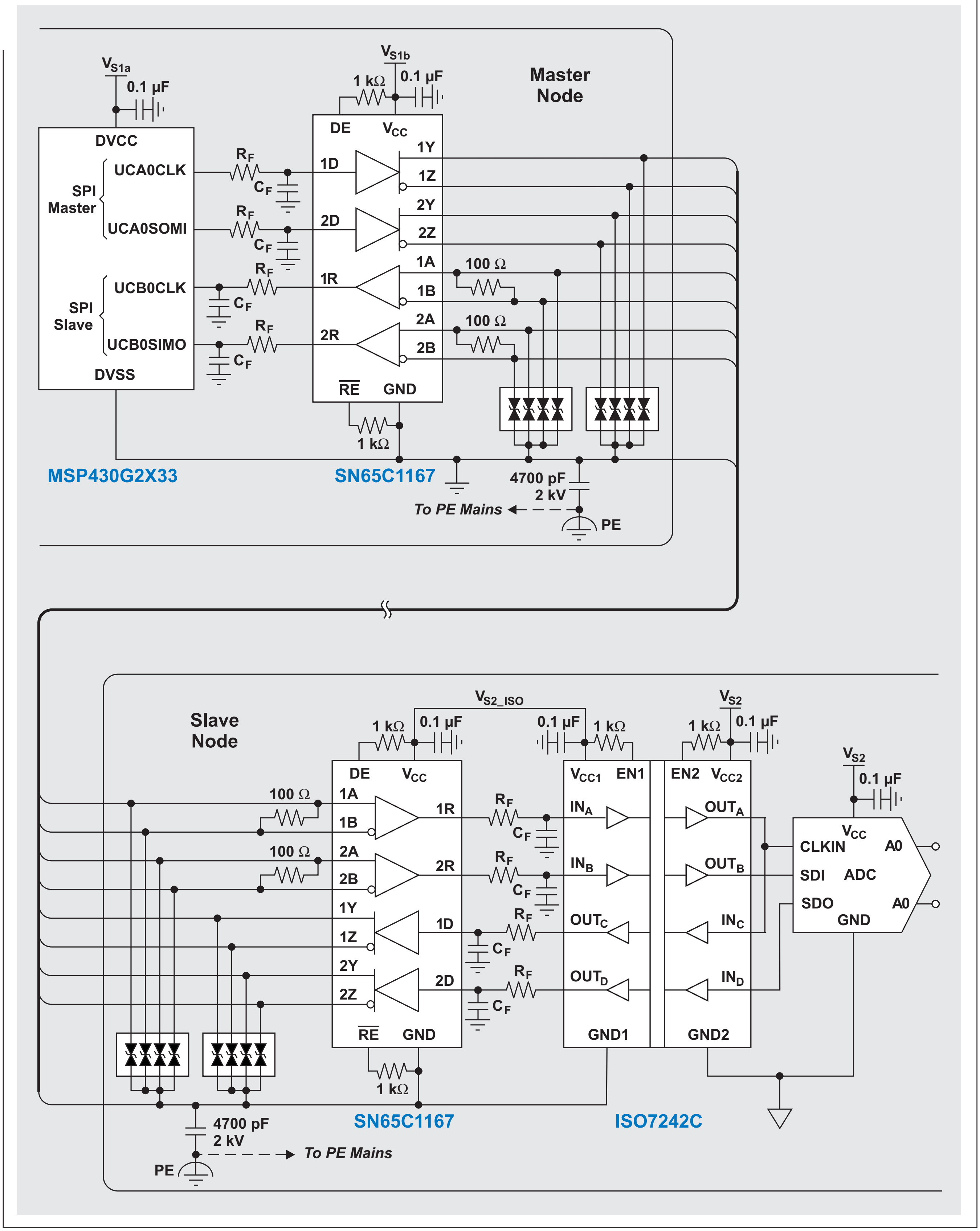


(a) Relationship of magnetic and electric fields

(b) Single conductor

(c) Closely coupled conductor pair

Figure 3. SPI extended via RS-422 data link



represent the maximum GPD. Much higher values are often encountered in industrial plants, sometimes reaching several hundreds and even thousands of volts. Because GPDs largely depend on factors outside the system designer's control, such as the electric installation and/or the number of electric motors and generators, the most secure way to prevent transceiver damage from large ground-potential variations is to galvanically isolate any remote network node from the bus. The circuit in Figure 3 demonstrates this by having only the remote transceiver connected to the bus, while the data-converter circuit is galvanically isolated.

Also, to provide the input and output signals of the remote transceiver with a stable ground reference, the transceiver's ground terminal as well as the digital isolator's ground terminal (GND1) are connected to the master ground potential via a separate ground conductor. This form of grounding is known as a single ground reference.

Avoiding antennas through line termination

The data link in Figure 3 is terminated with 100-Ω resistors, as suggested by the RS-422 standard, matching the characteristic impedance of the bus cable. A myth exists that bus cables of a few meters in length or data links operating at low data rates don't need termination. Don't believe it. Operating the bus without termination can turn the transmission line into a nasty receiver/transmitter antenna. The lack of termination resistors, which usually absorb the incident wave power sent by the driver, causes standing waves to occur; and the entire incident wave is reflected into the bus. The reflected waves mix with other incident waves, thus yielding standing waves for signal frequencies whose quarter wavelengths, or multiples thereof, equal the length of the data link.

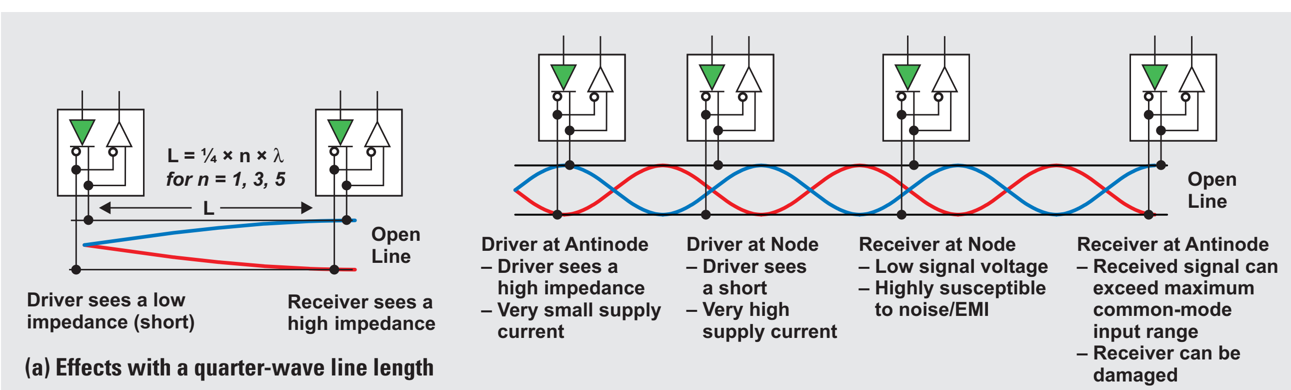
Depending on their location, the wave nodes (minima) and antinodes (maxima) can have varying effects on the bus transceivers (see Figure 5). A driver close to an antinode sees a high impedance and therefore transfers insufficient energy to the bus. A driver close to a node sees a very low impedance or a short. The resulting output current can exceed the driver's maximum drive capability and even trigger its current limit at around 250 mA. Receivers located at antinodes can be damaged by excessively large input signals that exceed the receiver's common-mode input range. Receivers close to nodes experience insufficient signal strength and are highly susceptible to noise and EMI. Any of the foregoing events will result in data errors from either the transmission or the reception of wrong data.

Protecting the network against damaging transients

Electrical overstress transients caused by electrostatic discharge (ESD), switching of inductive loads, or lightning strikes will corrupt data transmission and damage bus transceivers unless effective measures are taken to diminish their impact. Modern transient-voltage suppressors, such as the ones in Figure 3, are the preferred protection components for high-speed data transmission due to their low capacitance, which allows them to be designed into every node of a multinode network without requiring a reduction in data rate.

Depending on the power rating of the transient-voltage suppressor chosen, the maximum clamp voltages can range from 25 to 35 V, which is higher than a standard transceiver's maximum bus voltage of 14 V. In this case, the internal protection circuit of the transceiver must

Figure 5. Effects of an unterminated bus



(a) Effects with a quarter-wave line length

(b) Effects of connecting drivers and receivers at nodes and antinodes

absorb the remaining clamp energy to protect the device from damage.

For ESD and burst transients, the clamp energy is rather low due to the short pulse duration and does not pose a problem to the internal ESD cells. Clamp energy from surge transients, however, can present a serious challenge due to the much longer pulse duration. For transceivers specified with low ESD immunity, series resistors might be necessary to reduce the remaining current flowing into the transceiver. Common resistor values range from 5 to 10 Ω. Note that these resistors must be surge-rated to provide high pulse robustness.

Although the transient-voltage suppressor's diodes divert large transient currents to ground, it must be ensured that these currents are further diverted to true earth potential without disturbing the ground reference of the remaining circuitry. Often this is accomplished by implementing a high-voltage capacitor that has one plate connected to ground and the other plate connected to a protective-earth (PE) island. This island is then connected via a short, low-inductance earthing wire to the PE terminal of the local mains supply.

In addition to the suppressor's action on the bus side, further protection against signal degradation is required on the transceiver's single-ended sides. This is accomplished with R-C low-pass filters, which filter transient remnants in the reception path and stop high-frequency noise from entering the transmission path.

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