

TI Precision Designs: Verified Design

Ratiometric 3-Wire RTD Acquisition System, 0 °C – 100 °C, 0.005% FSR



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Circuit Description

This ratiometric temperature acquisition system accurately measures temperature over a range of 0 °C – 100 °C. The design uses a resistance temperature detector (RTD) in a 3-wire configuration to minimize the errors introduced by the lead resistances of a remotely located RTD. A 24-bit delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) excites the 3-wire RTD with 2 precision current sources and converts the differential voltage into a digital output. The digital output can then be translated into a final temperature result.

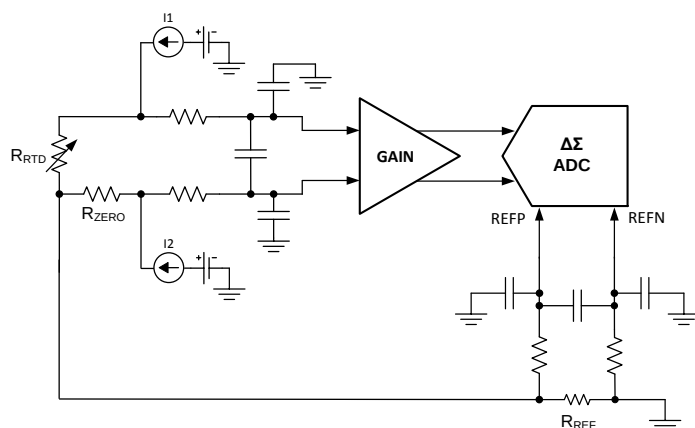
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1 Design Summary

The design requirements are as follows:

- Temperature Range: 0 °C – 100 °C
- Output: 0.005% FSR accurate temperature results
- System Supply Voltage: 4.3 V – 5.5 V
- Generated Supplies:
 - AVDD = 3.3 V
 - DVDD = 3.3 V
- ADC Reference Voltage: 1.65 V

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals and Measured Performance

	Goal	Measured
Unadjusted Precision Resistance Measurement Accuracy (%FSR)	0.15	0.15
Calibrated Precision Resistance Measurement Accuracy (%FSR)	0.005	0.0035
Unadjusted Temperature Error (including RTD) (%FSR)	0.025	0.023

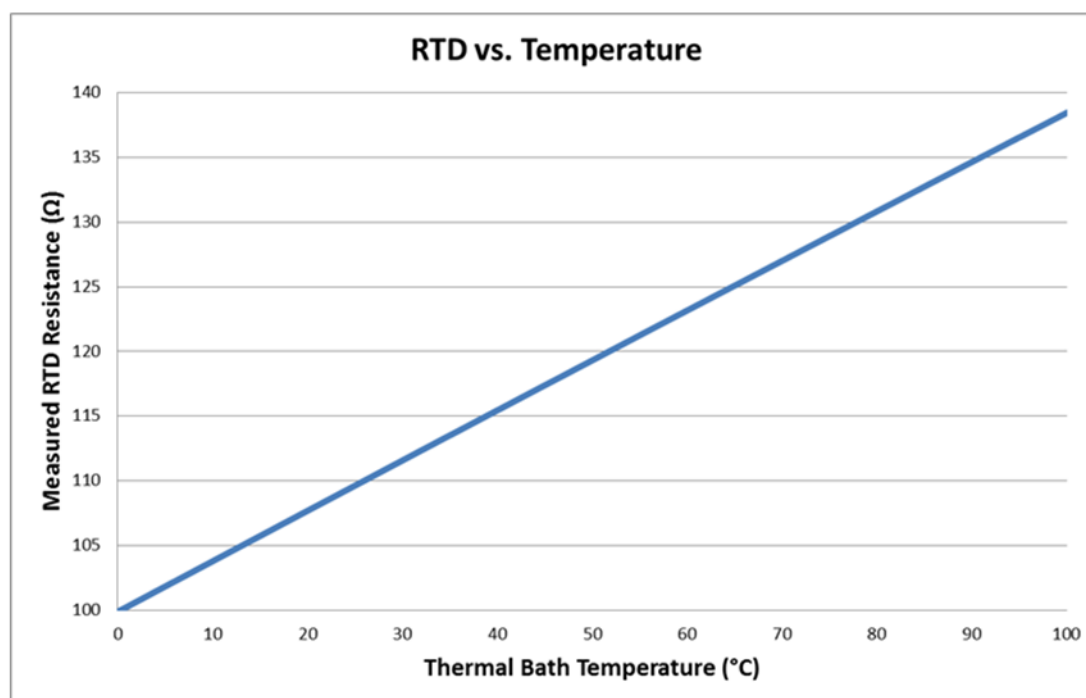


Figure 1. Measured Transfer Function

2 Theory of Operation

2.1 Resistance Temperature Detector (RTD) Overview

RTDs are sensing elements made of metals that have predictable resistance characteristics over temperature. The temperature of an RTD can therefore be calculated by measuring the resistance. RTD sensors offer wide temperature ranges, good linearity, and excellent long term stability and repeatability, making them suitable for many precision applications.

The relationship between resistance and temperature is defined by the Callendar-Van Dusen (CVD) equations which can be found in Appendix A.3

The main disadvantages of RTD sensors are their cost and requirement for an excitation source. The small change in output of an RTD also places demands on the accuracy of the acquisition circuit requiring a precision signal chain.

2.2 RTD Resistance Measurement

Most RTD applications use a current source as excitation for the RTD element. By driving a known current through the RTD, a voltage potential is developed that is proportional to the resistance of the RTD and the excitation current. This voltage potential is amplified and then fed to the inputs of an ADC, which converts the voltage into a digital output that can be used to calculate the RTD resistance.

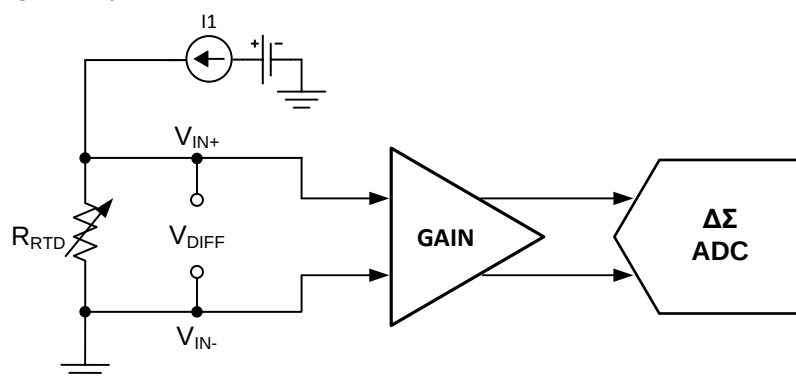


Figure 2. Simplified RTD Application

2.2.1 Current Source

The magnitude of the current source directly affects the magnitude of the RTD voltage. While maximizing the magnitude of the excitation current would seem desirable, higher excitation currents create higher power-dissipation leading to self-heating of the RTD. Errors due to self-heating cannot be easily corrected and should be avoided. Keeping the excitation current small will also minimize the heat produced in other signal path components, reducing drift and other additional measurement errors.

2.2.2 Amplification Stage

By choosing a small value for the excitation current, the RTD produces a small voltage over the span of the temperature measurement. This voltage would not use the full input range of the ADC configured for a mid-supply reference. A gain stage is therefore required to amplify the RTD voltage to a level that uses more of the full-scale ADC input range and maximizes resolution.

2.2.3 Ratiometric Measurements

An ADC requires a reference voltage to convert the input voltage into a digital output. In most applications, this reference is fixed and generated either internal or external to the ADC. This 3-wire RTD system uses what is known as a ratiometric configuration to provide an external reference which increases system accuracy.

In a ratiometric configuration, the excitation current that flows through the RTD returns to ground through a low-side reference resistor, R_{REF} , as shown in Figure 3. The voltage potential developed across R_{REF} is fed into the positive and negative reference pins (REFP and REFN) of the ADC and is used as the reference voltage for the analog-to-digital conversions. The R_{REF} resistor and excitation current will be sized to produce a 1.65 V external reference. R_{REF} should be selected as a low tolerance, low drift resistor for accurate results.

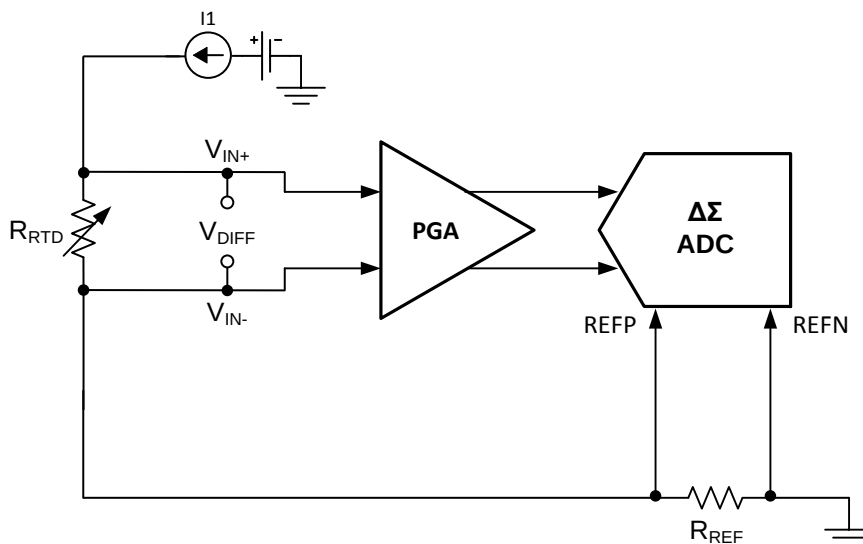


Figure 3. Ratiometric RTD Measurement

The voltage drop across the RTD and R_{REF} resistors is produced by the same excitation source. Therefore, any changes in the excitation source are reflected in both the RTD differential voltage and the reference voltage. Since the ADC output code is a relationship between the input voltage and the reference voltage, the effects of noise, drift, and accuracy of the current source cancel without affecting the final result. The ratiometric configuration also helps reduce external noise that appears common to both the inputs and the reference.

2.2.4 Hardware Compensated 3-Wire RTD Measurements

3-wire RTD configurations require two equal excitation sources to eliminate the resistance of the RTD leads from the final measurement. The input to the gain stage in a simplified hardware compensated 3-wire RTD measurement system and the equations that define its operation are shown in Figure 4 and Equations 1 – 4.

The hardware compensation resistor, R_{ZERO} , is placed in series with the negative ADC input. The voltage drop across R_{ZERO} subtracts from the voltage drop across the RTD, creating a bipolar voltage as opposed to the single-ended voltage of a traditional RTD measurement system. The bipolar voltage allows the system to make use of a larger gain stage, increasing the effective resolution. The value of R_{ZERO} is chosen to equal the resistance of the RTD at the mid-scale temperature value so that the input to the gain stage will swing equally in both the positive and negative directions.

Equation 4 shows that the final differential voltage is only based on the difference between the RTD and R_{ZERO} , assuming the current sources are perfectly matched and the resistances in all three RTD leads are equal.

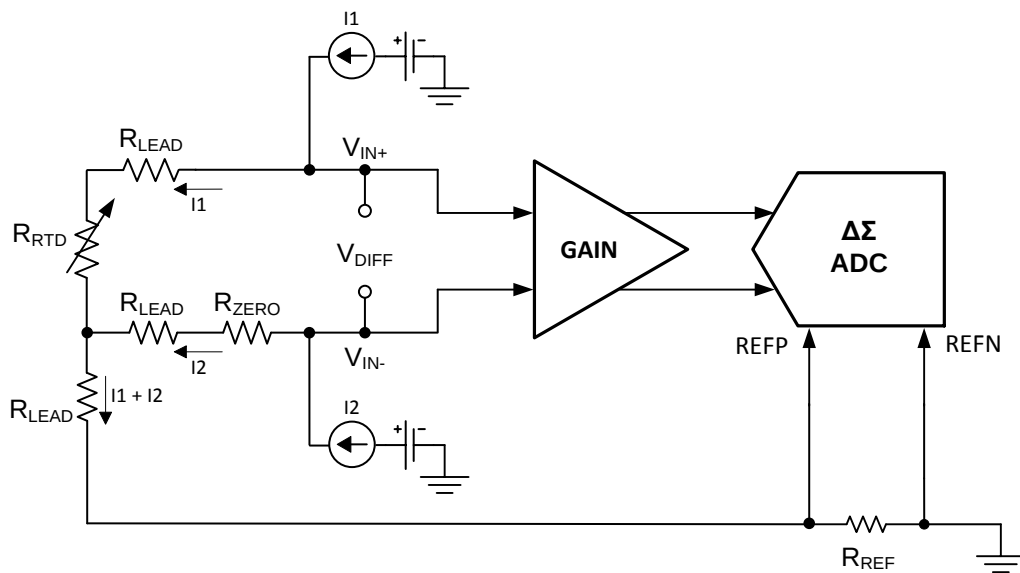


Figure 4. 3-Wire RTD Lead Resistances Canceled by Excitation Currents

$$I_1 = I_2 = I \quad (1)$$

$$\begin{aligned} V_{IN+} &= I \times (R_{LEAD} + R_{RTD}) + 2I \times (R_{LEAD} + R_{REF}) \\ V_{IN+} &= 3I \times R_{LEAD} + 2I \times R_{REF} + I \times R_{RTD} \end{aligned} \quad (2)$$

$$\begin{aligned} V_{IN-} &= I \times (R_{LEAD} + R_{ZERO}) + 2I \times (R_{LEAD} + R_{REF}) \\ V_{IN-} &= 3I \times R_{LEAD} + 2I \times R_{REF} \end{aligned} \quad (3)$$

$$V_{DIFF} = V_{IN+} - V_{IN-} = I \times (R_{RTD} - R_{ZERO}) \quad (4)$$

See Reference 2 for more information on other RTD configurations.

2.2.5 Input and Reference Low-Pass Noise Filters

Using differential and common-mode low-pass filters at the input and reference paths improves the cancellation of excitation and environment noise. However, it is important to note that the corner frequency of the two differential filters must be well matched as stated in Reference 1.

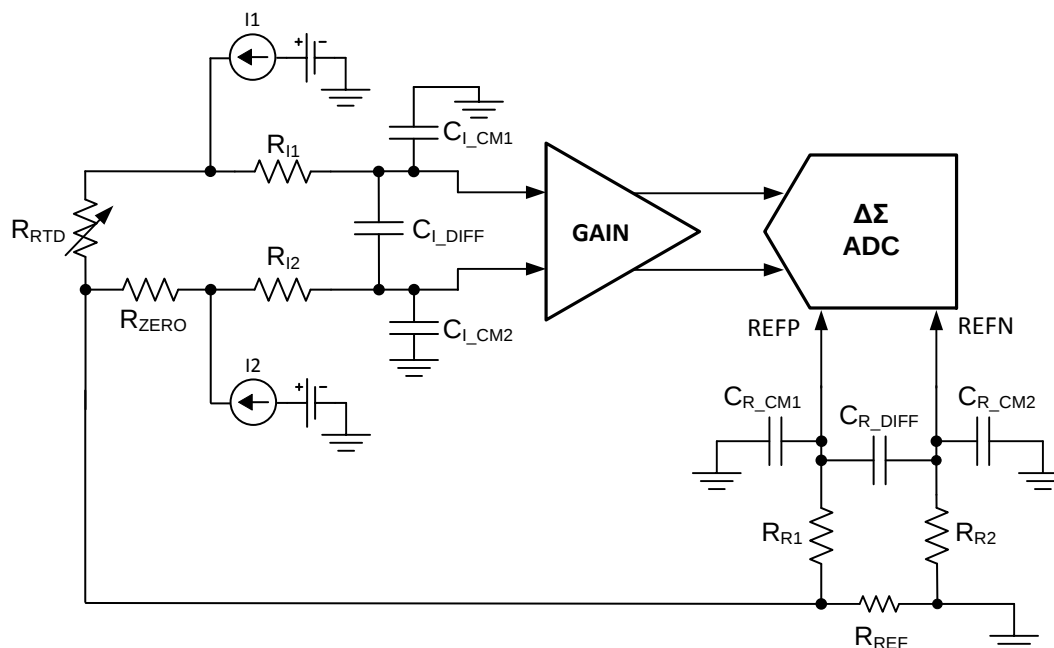


Figure 5. 3-Wire RTD Acquisition System with Input and Reference Filters

3 Component Selection

3.1 PT-100 RTD

The PT-100 RTD is a platinum-based RTD sensor. Platinum is a noble metal and offers excellent performance over a wide temperature range. Platinum also features the highest resistivity of commonly used RTD materials, requiring less material to create desirable resistance values. The PT-100 RTD has an impedance of 100 Ω at 0 $^{\circ}\text{C}$ and roughly 0.385 Ω of resistance change per 1 $^{\circ}\text{C}$ change in temperature, resulting in 119.6 Ω at 50 $^{\circ}\text{C}$ and 138.4 Ω at 100 $^{\circ}\text{C}$. Higher-valued resistance sensors, such as PT-1000 or PT-5000, can be used for increased sensitivity and resolution.

Verified performance in Section 6 was collected with a Class-A PT-100 RTD. Class-A RTDs were chosen for this application to provide good pre-calibration accuracy and long-term stability. A Class-A RTD will have less than 0.5 $^{\circ}\text{C}$ of error at 100 $^{\circ}\text{C}$ without calibration and the long-term stability makes accurate infrequent calibration possible. Table 2 displays the tolerance, initial accuracy and resulting error at 100 $^{\circ}\text{C}$ for the five main classes of RTDs.

Table 2. RTD Class Tolerance Information

Tolerance Class (DIN-IEC 60751)	Tolerance Values ($^{\circ}\text{C}$)	Resistance at 0 $^{\circ}\text{C}$ (Ω)	Error at 100 $^{\circ}\text{C}$ ($^{\circ}\text{C}$)
*AAA	+/- (0.03 + 0.0005*t)	100 +/- 0.012	+/- 0.08
AA	+/- (0.01 + 0.0017*t)	100 +/- 0.04	+/- 0.27
A	+/- (0.15 + 0.002*t)	100 +/- 0.06	+/- 0.35
B	+/- (0.3 + 0.005*t)	100 +/- 0.12	+/- 0.8
C	+/- (0.6 + 0.01*t)	100 +/- 0.24	+/- 1.6

*AAA is not included in the DIN-IEC 60751 specification but is an industry accepted tolerance for performance demanding applications.

3.2 ADC – ADS1247

The ADS1247 is a 24-bit, delta-sigma ($\Delta\Sigma$) ADC from Texas Instruments that offers a complete front-end solution for RTD applications. It comes from a product family of highly integrated precision data converters, featuring a low-noise, programmable gain amplifier (PGA), a precision $\Delta\Sigma$ modulator, a digital filter, an internal oscillator, and two digitally controlled precision current sources (IDACs). It is a popular industry choice for precision temperature measurement applications.

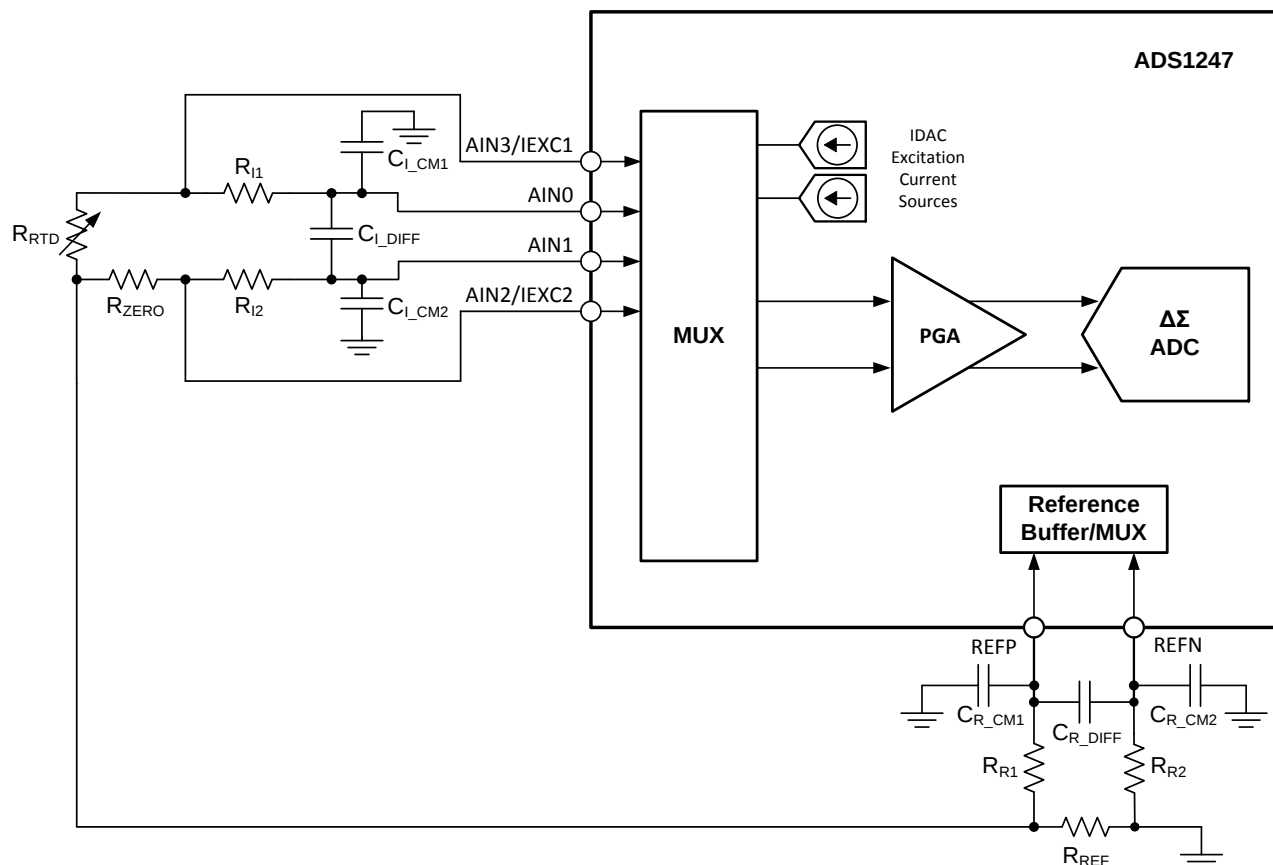


Figure 6. Ratiometric 3-Wire RTD Acquisition System Featuring the ADS1247

3.2.1 Current Source (IDAC) Configuration

The ADS1247 features two IDAC current sources capable of outputting currents from 50 μA to 1.5 mA. To minimize self-heating of the RTD, R_{REF} , and R_{ZERO} resistors, the excitation currents will be set to 100 μA .

The internal reference voltage must be on while using the IDACs, even if an external reference is used for ADC conversions. Table 3 displays the required register settings to set the IDACs to 100 μA and configure them for the proper output channels.

Table 3. Register Settings for Current Sources

Register (Address)	Register Bits	Bits Name	Bit Values	Comment
MUX1 (02h)	MUX1[6:5]	VREFCON[1:0]	01	Internal Reference ON
IDAC0 (0Ah)	IDAC0[2:0]	IMAG[2:0]	010	IDACs = 100 μA
IDAC1 (0Bh)	IDAC1[7:4]	I1DIR[3:0]	0011	IDAC1 $\rightarrow$ AIN3

IDAC1 (0Bh)	IDAC1[3:0]	I2DIR[3:0]	0010	IDAC2 → AIN2
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3.2.2 IDAC Multiplex Chopping

As Equation 1 through Equation 4 show, the two current sources must be perfectly matched to successfully cancel the lead resistances of the RTD wires. While initial matching of the current sources is important, any remaining mismatch in the two sources can be minimized by using a multiplexor to swap, or “chop,” the two current sources between the two inputs. Taking a measurement in both configurations and averaging the two readings will greatly reduce the effects of mismatched current sources. This design uses the digitally-controlled multiplexer in the ADS1247 to realize this technique. The multiplexer also affords the user some additional flexibility when routing the input voltage signals and excitation current sources on their printed circuit board (PCB) layout.

3.2.3 Programmable Gain Amplifier (PGA) Configuration

In this application, the ADC uses a 3.3 V supply for both the analog (AVDD) and digital (DVDD) power supplies. The excitation currents and R_{REF} have been selected to produce a mid-supply 1.65 V reference, allowing for a differential input signal range of ± 1.65 V into the $\Delta\Sigma$ modulator.

The maximum allowable PGA gain setting is based on the reference voltage, the RTD resistance change, and the excitation current as shown in Equations 5 – 7.

$$\begin{aligned} R_{DIFF_MAX} &= R_{ZERO} - R_{RTD_MIN} = 120\ \Omega - 100\ \Omega \\ R_{DIFF_MAX} &= 20\ \Omega \end{aligned} \quad (5)$$

$$\begin{aligned} V_{IN_PGA(max)} &= I_{IDAC} \times R_{DIFF_MAX} = 100\ \mu A \times 20\ \Omega \\ V_{IN_PGA(max)} &= 2\ mV \end{aligned} \quad (6)$$

$$\begin{aligned} PGA_{MAX} &= \frac{V_{REF}}{V_{IN_PGA(max)}} = \frac{1.65\ V}{2\ mV} \\ PGA_{MAX} &= 825\ V/V \end{aligned} \quad (7)$$

Based on Equation 7, the PGA gain is set to the maximum value available in the ADS1247, 128 V/V, as shown in Table 4. This will yield optimal resolution and noise performance.

Table 4. Register Settings for PGA

Register (Address)	Register Bits	Bits Name	Bit Values	Comment
SYS0 (03h)	SYS0[6:4]	PGA[2:0]	111	PGA = 128 V/V

3.3 Passive Components

3.3.1 R_{REF}

The voltage drop across the reference resistor, R_{REF} , serves as an external reference input to the ADC. This external reference is used by the ADC to make the analog-to-digital conversion and determines the input common-mode of the PGA.

The value of R_{REF} is selected based on the IDAC setting and the desired V_{REF} voltage of 1.65 V as shown in Equations 8 - 9.

$$R_{REF} = \frac{V_{REF}}{2 \times I_{IDAC}} \quad (8)$$

$$R_{REF} = \frac{1.65 \text{ V}}{2 \times 100 \text{ } \mu\text{A}} = 8.25 \text{ k}\Omega \quad (9)$$

An 8.2 k Ω R_{REF} resistor was chosen based on availability of high tolerance resistors resulting in a reference voltage of 1.64 V as shown in Equation 10. The tolerance and temperature drift of R_{REF} directly affect the measurement gain error, so a 0.02% precision resistor with $\pm 5 \text{ ppm}/^\circ\text{C}$ drift was chosen.

$$V_{REF} = 8.2 \text{ k}\Omega \times 200 \text{ } \mu\text{A} = 1.64 \text{ V} \quad (10)$$

3.3.2 R_{ZERO}

The impedance range of the PT-100 RTD is 100 Ω – 138.5 Ω for temperatures from 0 $^\circ\text{C}$ - 100 $^\circ\text{C}$. At mid-scale, the RTD will equal 119.25 Ω . Using standard values, R_{ZERO} was chosen to be 120 Ω such that the differential input would swing almost equally in the positive and negative directions. The tolerance and temperature drift of R_{ZERO} directly affect the measurement accuracy, so a 0.02% precision resistor with $\pm 5 \text{ ppm}/^\circ\text{C}$ drift was chosen.

3.3.3 *Input and Reference Low-Pass Noise Filters*

The differential filters chosen for this application were designed to have a -3 dB corner frequency of about 250 Hz at mid-scale temperature ($R_{RTD} = 120 \text{ } \Omega$). For proper operation, the differential cutoff frequencies of the reference and input low-pass filters must be well matched. This can be difficult because as the resistance of the RTD changes over the span of the measurement, the filter cutoff frequency changes as well. To mitigate this effect, the two resistors used in the input filter (R_{I1} and R_{I2}) were chosen to be more than an order of magnitude larger than the RTD. Keeping the resistors to less than 20 k Ω will reduce dc errors due to input bias current. The two resistors were selected such that standard capacitor values could be used.

$$R_{I1} = R_{I2} = 6.8 \text{ k}\Omega \quad (11)$$

The input filter differential capacitor (C_{I_DIFF}) can be calculated as shown in Equation 12.

$$f_{-3dB_DIFF} = \frac{1}{2 \times \pi \times C_{I_DIFF} \times (R_{I1} + R_{RTD} + R_{ZERO} + R_{I2})} \quad (12)$$

$$C_{I_DIFF} \approx 47 \text{ nF}$$

To ensure that mismatch of the common-mode filtering capacitors is not translated to a differential voltage, the common-mode capacitors (C_{I_CM1} and C_{I_CM2}) were chosen to be 10 times smaller than the differential capacitor, making them 4.7 nF each. This results in a common-mode cutoff frequency that is roughly twenty times larger than the differential filter, making the matching of the common-mode cutoff frequencies less critical.

$$C_{I_CM1} = C_{I_CM2} = 4.7 \text{ nF} \quad (13)$$

$$f_{-3dB_CM+} = \frac{1}{2 \times \pi \times C_{I_CM1} \times (R_{I1} + R_{RTD} + R_{REF})} \quad (14)$$

$$f_{-3dB_CM+} = 2.24 \text{ kHz}$$

$$f_{-3dB_CM-} = \frac{1}{2 \times \pi \times C_{IN_CM2} \times (R_{I2} + R_{ZERO} + R_{REF})} \quad (15)$$

$$f_{-3dB_CM-} = 2.24 \text{ kHz}$$

The differential reference filter is designed to have a -3 dB corner frequency of 250 Hz to match the differential input filter. Once again, keeping the resistors to less than 20 kΩ will reduce dc errors. The two reference filter resistors were selected to be 17.4 kΩ to allow for standard capacitor values.

$$R_{R1} = R_{R2} = 17.4 \text{ k}\Omega \quad (16)$$

The differential capacitor for the reference filter can be calculated as shown in Equation 17.

$$f_{-3dB_DIFF} = \frac{1}{2 \times \pi \times C_{R_DIFF} \times (R_{R1} + R_{REF} + R_{R2})} \quad (17)$$

$$C_{R_DIFF} \approx 15 \text{ nF}$$

To ensure that mismatch of the common-mode filtering capacitors is not translated to a differential voltage, the reference common-mode capacitors (C_{R_CM1} and C_{R_CM2}) were chosen to be 10 times smaller than the reference differential capacitor, making them 1.5 nF each. Again, the resulting cutoff frequency for the common-mode filters is roughly twenty times larger than the differential filter, making the matching of the cutoff frequencies less critical.

$$C_{R_CM1} = C_{R_CM2} = 1.5 \text{ nF} \quad (18)$$

$$f_{-3dB_CM+} = \frac{1}{2 \times \pi \times C_{R_CM1} \times (R_{R1} + R_{REF})} \quad (19)$$

$$f_{-3dB} = 4.14 \text{ kHz}$$

$$f_{-3dB_CM-} = \frac{1}{2 \times \pi \times C_{R_CM2} \times R_{R2}} \quad (20)$$

$$f_{-3dB} = 6.1 \text{ kHz}$$

3.4 Low-Dropout (LDO) Linear Regulator

The RTD acquisition board in this design interfaces with an external PC GUI through a USB interface board to post-process the ADC digital output and display the temperature result. Power for the acquisition board comes from the USB power supply rail. To avoid the inaccuracies and noise from the USB power supply, VDUT may be passed through a high-PSRR low-dropout regulator (LDO) to create the AVDD and DVDD supplies.

The TPS7A4901 comes from a series of high-voltage, ultra-low noise LDOs that are ideal for precision applications. A resistor divider at the LDO output sets the output voltage (V_{LDO_OUT}) proportional to the LDO's internal reference voltage (V_{LDO_REF}). For this device, $V_{LDO_REF} = 1.194 \text{ V}$. In order to set V_{LDO_OUT} to the desired 3.3 V, the resistor divider components are selected as:

$$V_{LDO_OUT} = V_{LDO_REF} \times \left(1 + \frac{R1}{R2}\right) \quad (21)$$

$$R1 = 140 \text{ k}\Omega \quad (22)$$

$$R2 = 78.7 \text{ k}\Omega \quad (23)$$

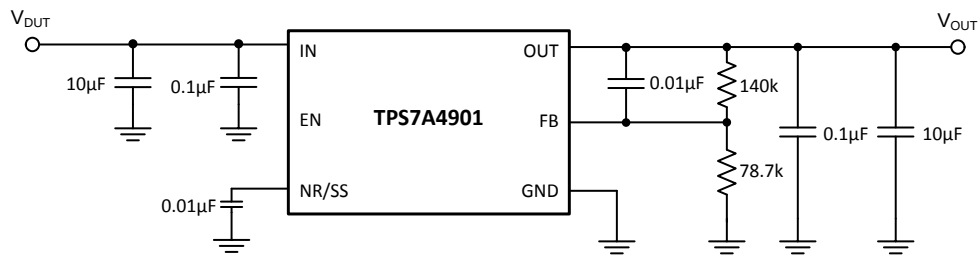


Figure 7. LDO Configuration for +3.3 V Output

4 Simulation

Figure 8 shows the TINA-TI™ circuit used to simulate the behavior of the RTD, input filtering, and PGA in this system. The RTD has been modeled with a PT-100 macromodel that converts an input voltage representative of the RTD temperature into the correct output resistance using the CVD equations. The simplified ADS1247 PGA does not accurately represent the internal circuitry to the ADC; however, it does represent the ideal behavior of the internal PGA.

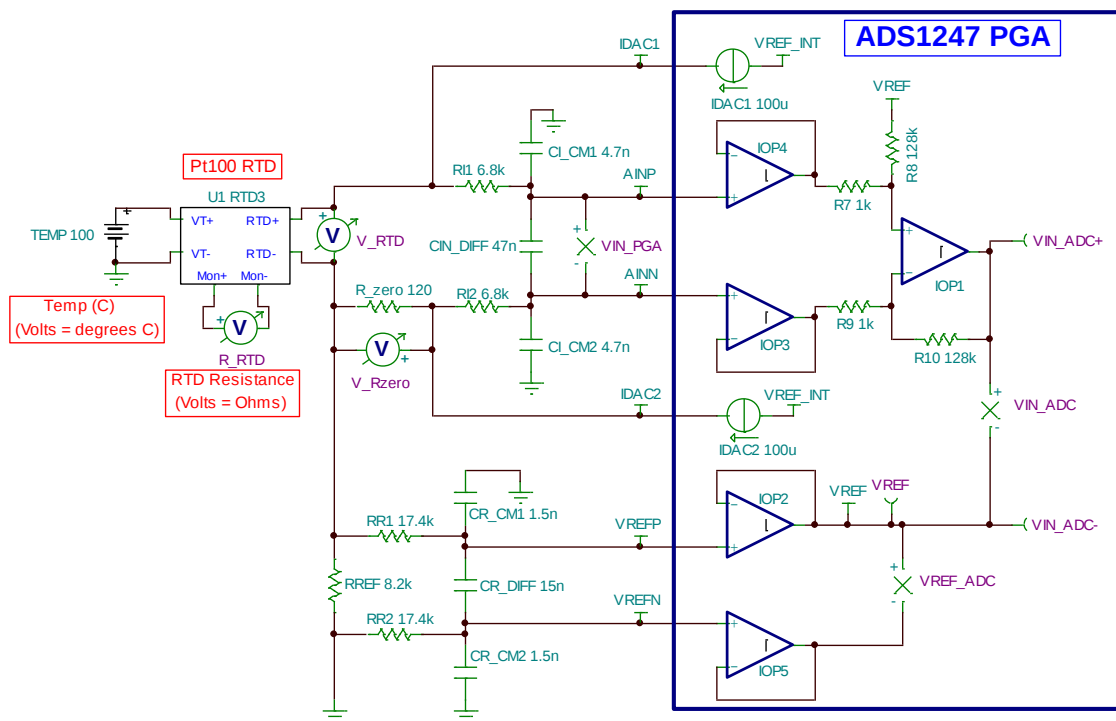


Figure 8. TINA-TI™ Simulation Circuit for the RTD and ADS1247 Inputs

4.1 RTD Transfer Function

Figure 9 displays the RTD resistance and voltage, the R_{ZERO} voltage, and the resulting differential voltage applied to the inputs of the PGA as the RTD temperature is swept from 0 °C – 100 °C. The results are displayed on the image for the minimum, mid-scale, and maximum temperatures. The 120 Ω value of R_{ZERO} is not exactly mid-scale of the RTD span (100 Ω – 138.5 Ω), so the bipolar ADC output features more negative codes than positive codes.

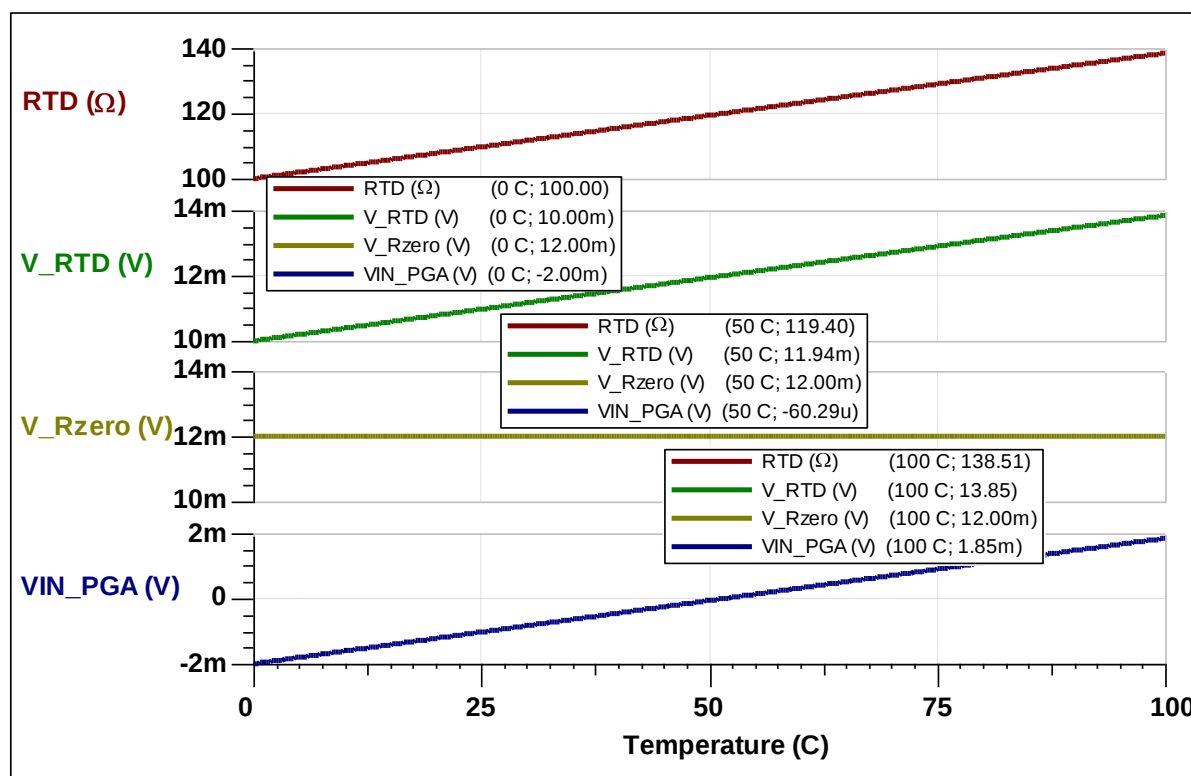


Figure 9. RTD, R_{ZERO} , and PGA Input from 0 °C – 100 °C

Figure 10 displays the input and the theoretical output of the PGA into the ADC when configured for a gain of 128 V/V. With an input of -2 mV to 1.85 mV, the PGA output is the expected -256 mV to 237 mV. The ADC reference voltage, V_{REF} , is also displayed in the Figure and is the expected 1.64 V.

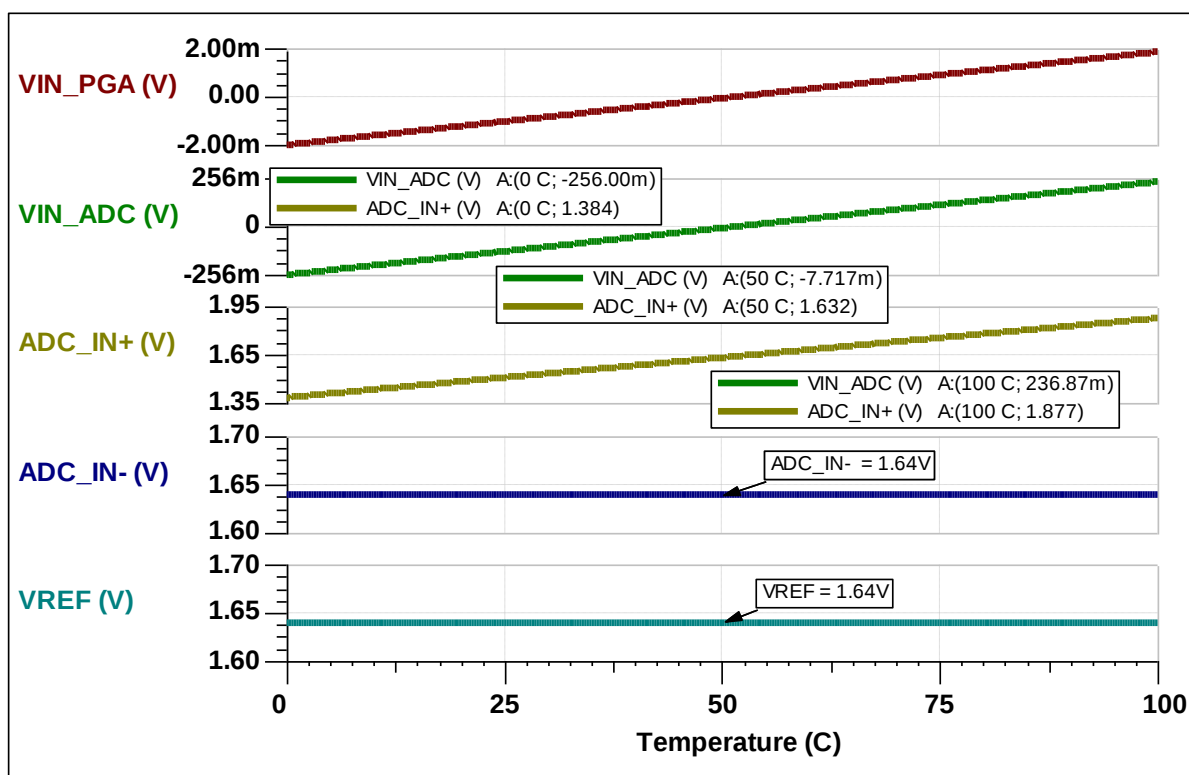


Figure 10. The Input and Output of the PGA and VREF from 0 °C – 100 °C

4.2 Low-pass Noise Filter Response

The frequency response of the input and reference filters was tested using an ac current generator in place of the IDAC1 source and is shown in Figure 11. The -3 dB cutoff frequency of the filters is near 230 Hz for both filters and is well matched with less than 3 Hz difference between them. The dc magnitude of the results is based on the current-to-voltage transfer function ($I \cdot R$) as the excitation currents pass through the passive resistors in the signal chain. The results with IDAC2 active are very similar and can be seen in Appendix O.

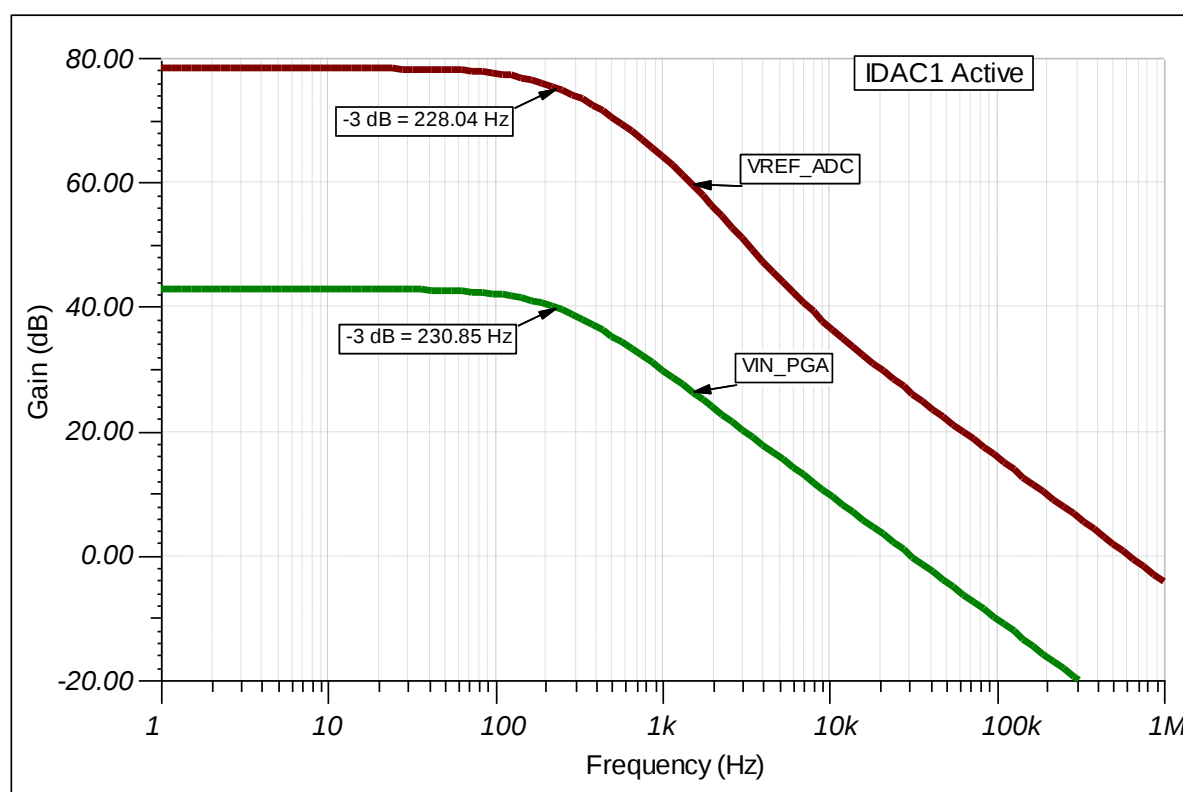


Figure 11. Simulated Filter Frequency Response

4.3 Noise Performance

The circuit and results for the simulated noise performance of the passive components in the design are shown in Figure 12 and Figure 13 respectively. The noise of the IDAC sources was not included because it should cancel with the ratiometric measurement. The extrinsic noise reduction of filtering the inputs is clearly shown in the difference between the magnitudes of noise before and after the filtering.

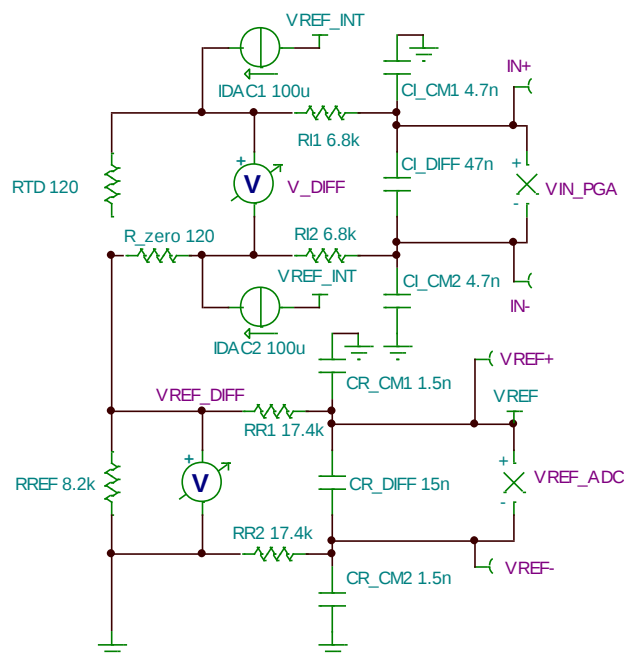


Figure 12. Noise Performance Simulation Schematic

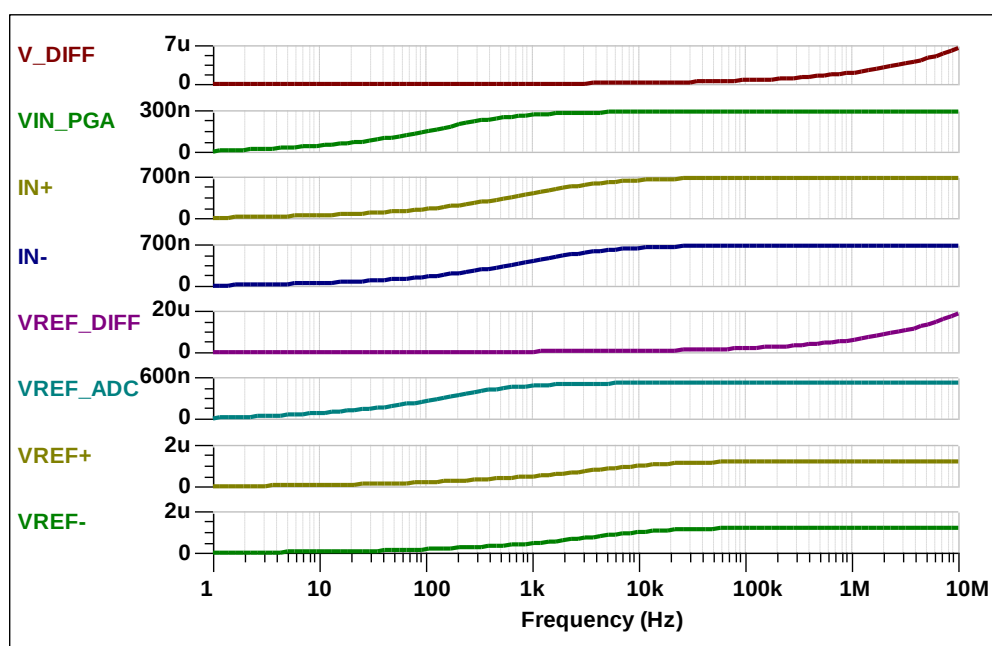


Figure 13. Simulated Noise Performance

5 PCB Design

Providing proper decoupling, grounding, and minimizing cross-over between the analog and digital circuitry return currents is required to achieve optimal performance in all mixed-signal PCB designs. In addition to standard practices, minimizing or balancing PCB trace resistance is a primary concern because the design is based on accurately measuring the difference between the RTD and R_{ZERO} . Implementing a 4-wire Kelvin connection at the RTD, R_{ZERO} , and R_{REF} resistors help to minimize PCB resistance in series with the sense elements.

As discussed in Section 2.2.4, the lead resistances of the 3-wire RTD are effectively cancelled when they are equal and the magnitude of the excitation current sources are also equal. The same theory applies to PCB trace resistance in series with the 3 RTD leads. Therefore, the PCB trace resistance in series with R_{ZERO} and the RTD must be balanced, otherwise additional differential signals will be formed. The resistance of the R_{REF} trace is common to both inputs and is cancelled by taking the differential measurement, making it less critical.

Balancing the RTD and R_{REF} trace resistance is accomplished by creating traces of equal length between the terminal block and the R_{ZERO} and RTD connection points. Figure 14 displays these critical PCB layout areas. The full PCB layout is shown in Figure 15.

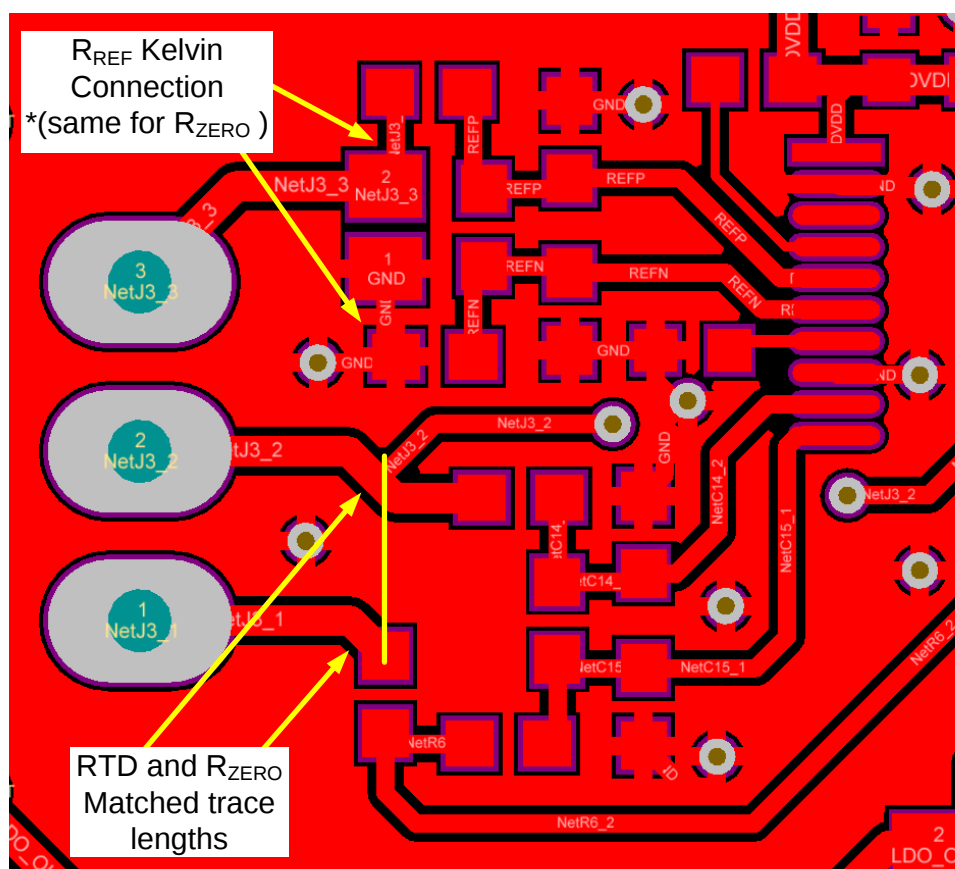


Figure 14. PCB Layout Highlighting Important PCB Layout Concerns

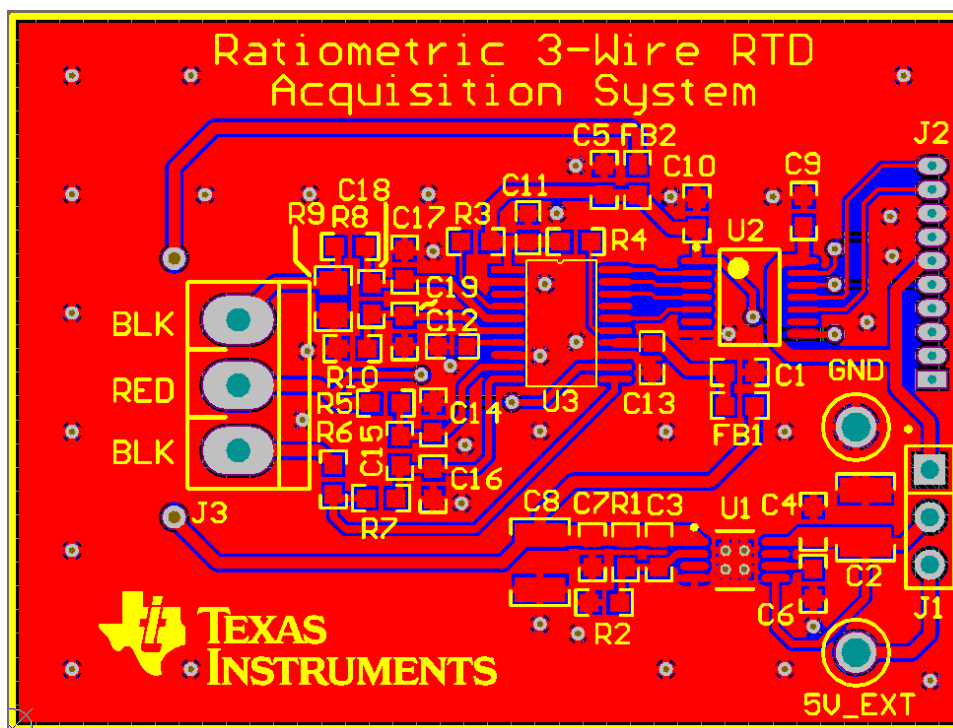


Figure 15. Full PCB Layout

6 Verification & Measured Performance

6.1 Measured Transfer Function with Precision Resistor Input

To test the accuracy of only the acquisition circuit, a series of calibrated high-precision discrete resistors were used as the input to the system. Figure 16 displays the unadjusted accuracy of the system over a resistance input span from 100 Ω to 140 Ω . The offset error can be attributed largely to the tolerance of the R_{ZERO} resistor and the offset of the ADC, while the gain error can be attributed to the accuracy of the R_{REF} resistor and gain error of the PGA and ADC.

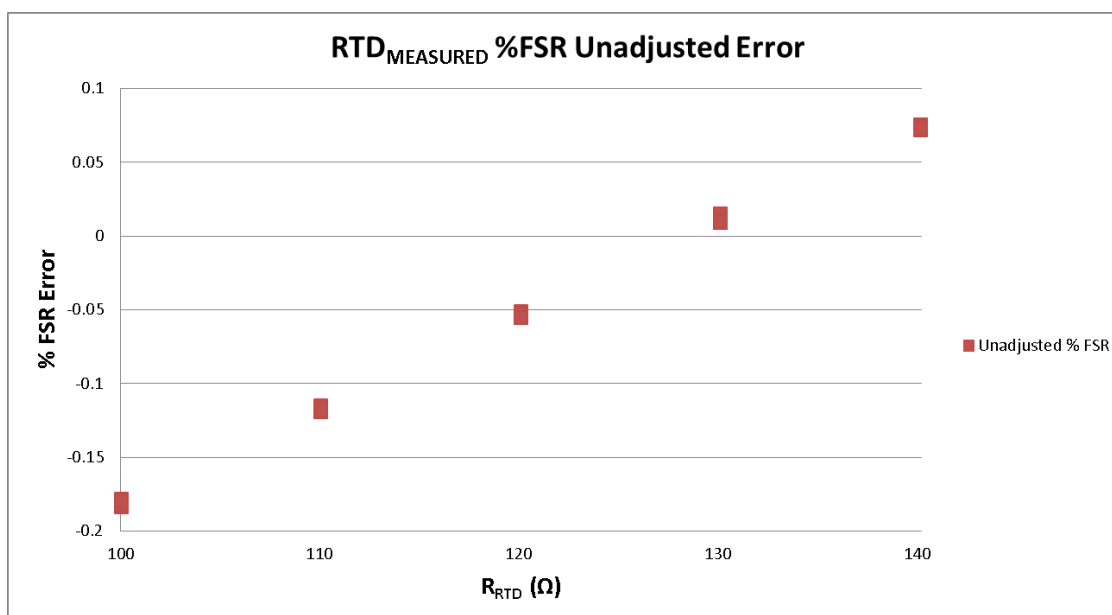


Figure 16. Performance Results with Precision Resistors before Calibration

Applying a simple first-order gain and offset calibration yields the calibrated results shown in Figure 17.

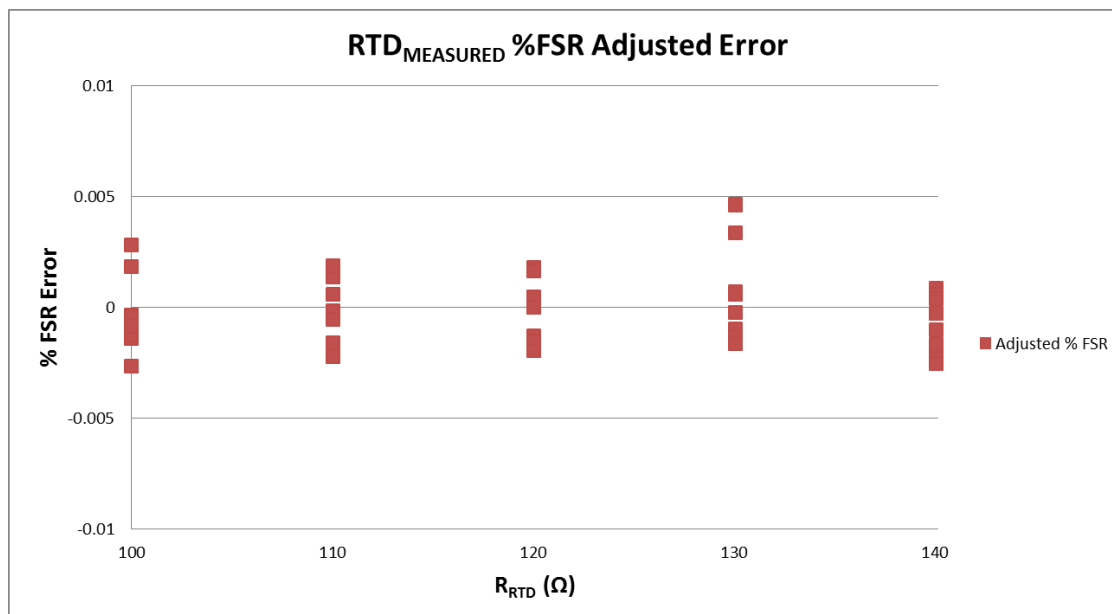


Figure 17. Performance Results with Precision Resistors after Calibration

6.2 Noise Histogram

The peak-to-peak noise of the acquisition system can be approximated from an output code histogram. The RTD was replaced with a 120 Ω, 0.01% precision resistor in order to remove noise from the sense element and then 100 individual samples were recorded to generate the histogram plot shown in Figure 18. The peak-to-peak code deviation in the histogram is 273 codes. Equation 24 calculates the Least-Significant Bit (LSB) size of the ADC, which is then used to translate the 273 code spread to 0.42 μV_{PP} of noise in Equation 25.

$$1 \text{ LSB} = \frac{\pm V_{\text{REF}} / \text{PGA}}{2^{24} - 1} \quad (24)$$

$$1 \text{ LSB} = \frac{\pm 1.65 \text{ V} / 128}{2^{24} - 1} = 1.54 \text{ nV}$$

$$\text{Noise } (\mu\text{V}_{\text{PP}}) = 273 \times 1.54 \text{ nV} = 0.42 \mu\text{V}_{\text{PP}} \quad (25)$$

Due to the ratiometric configuration of this circuit, the averaging of the chopped IDAC measurements, and non-contiguous data collection, it is reasonable to assume that the measured peak-to-peak noise for this system will not perfectly correlate to the performance in the datasheet because the product was not characterized in this manner.

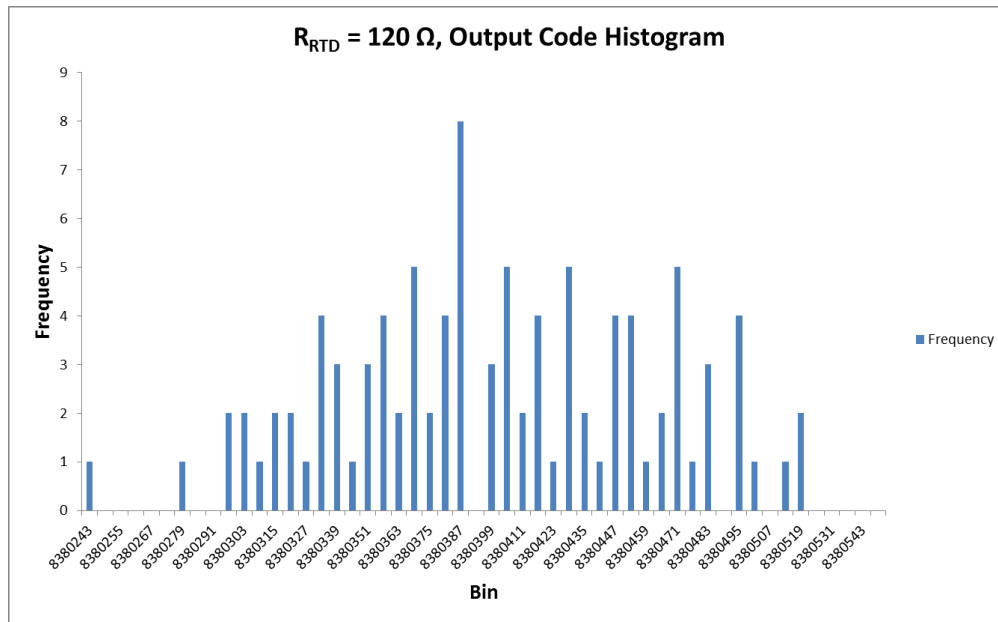


Figure 18. 100-point Histogram with $R_{RTD} = 120 \Omega$, 0.01%

Equations 26 and 27 calculate the number of codes per degree Celsius in this application:

$$\text{TotalFS Codes} = \frac{PGA_{FS_SWING}}{1 \text{ LSB}} = \frac{3.85 \text{ mV}}{1.54 \text{ nV}} = 2.5 \times 10^6 \text{ codes} \quad (26)$$

$$^{\circ}\text{C} / \text{Code} = \frac{100^{\circ}\text{C}}{2.5 \times 10^6 \text{ codes}} = 40 \mu^{\circ}\text{C} / \text{code} \quad (27)$$

Based on the result of the histogram and Equation 27, the 6- σ noise spread in degrees Celsius can be calculated as shown in Equation 28:

$$\text{Noise } (^{\circ}\text{C}_{PP}) = 40 \mu^{\circ}\text{C} \times 273 \text{ codes} = 0.0109^{\circ}\text{C}_{PP} \quad (28)$$

The noise can be reduced by applying additional averaging or filtering in software.

6.3 Transfer Function with RTD in Thermal Bath

To test the system in an example application, an Omega PR-11-2-100-M15-150-E RTD was connected to the acquisition system and placed into a 0.01 °C accurate calibrated thermal bath. As a control measurement, a 0.001 °C calibrated 4-wire probe was also placed into the thermal bath and recorded simultaneously. The bath temperature was then swept from 0 °C – 100 °C. The resulting measured RTD resistance is shown in Figure 19.

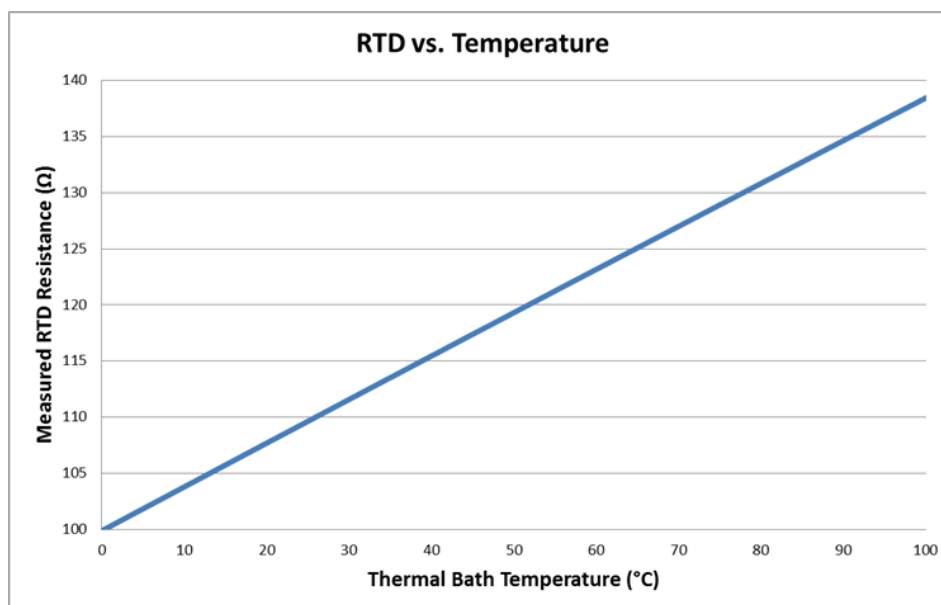


Figure 19. RTD Resistance Change vs. Temperature in Thermal Bath

The resulting error shown in Figure 20 falls within the accuracy of a Class A RTD. To achieve the same accuracy shown with the precision resistor measurements, the RTD element itself must be calibrated to correct for its inherent errors.

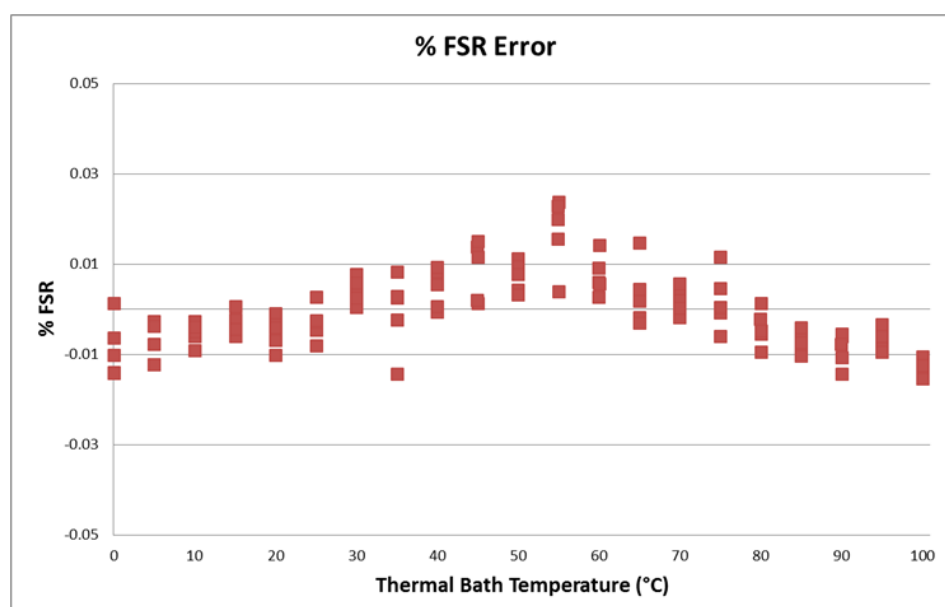


Figure 20. Unadjusted Temperature Error with RTD in Thermal Bath

7 Modifications

There are a few other fully integrated products that feature the same required building blocks as the ADS1247 that feature different performance, channel count, and cost. Several of these devices are listed in Table 5.

Table 5. Alternate Fully-Integrated ADC Solutions

ADC	Resolution	Differential Inputs	PGA Range	IDACs Magnitude	Noise	Power Consumption	Cost (1ku)
ADS1147	16	2	1 – 128 V/V	50 μ A – 1.5 mA	0.14 μ Vrms	1.4 mW	\$3.45
ADS1247	24	2	•	•	•	•	\$4.45
ADS1148	16	4	•	•	•	•	\$3.95
ADS1248	24	4	•	•	•	•	\$4.95
ADS1220	24	2	•	10 μ A – 1.5 mA	0.09 μ Vrms	0.4 mW	\$3.95
LMP90100	24	4	•	100 μ A – 1 mA	0.25 μ Vrms	1.2 mW	\$3.33

Table 6 features other suitable ADC solutions that feature integrated PGAs.

Table 6. Alternate ADC + PGA Solutions

ADC	Resolution	Differential Inputs	PGA Range	Noise	Power Consumption	Cost (1ku)
ADS1146	16	1	1 – 128 V/V	0.14 μ Vrms	1.4 mW	\$2.70
ADS1246	24	1	•	•	•	\$3.45
ADS1120	16	2	•	0.09 μ Vrms	0.4 mW	\$3.78
LMP90099	24	4	•	0.25 μ Vrms	1.2 mW	\$3.17

Discrete current sources could be comprised of an integrated device such as the REF200 or a circuit such as the designs featured in [TIPD101](#) or [TIPD107](#).

8 About the Author

Ryan Andrews is an applications engineer with the Precision Analog Delta-Sigma ADC team at Texas Instruments, where he supports industrial and medical products and applications. Ryan received his BS in Biomedical Engineering and his BA in Spanish from the University of Rhode Island.

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

9 Acknowledgements & References

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2. *Robert Burnham and Nagaraj Ananthapadamanabhan, "Example Temperature Measurement Applications Using the ADS1247 and ADS1248" SBAA180, January 2011.*
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4. *Omega®, "The Omega® Temperature Measurement HandbookTM and Encyclopedia, Vol MMXIVTM, 7th Edition.*

Appendix A.

A.1 Electrical Schematic

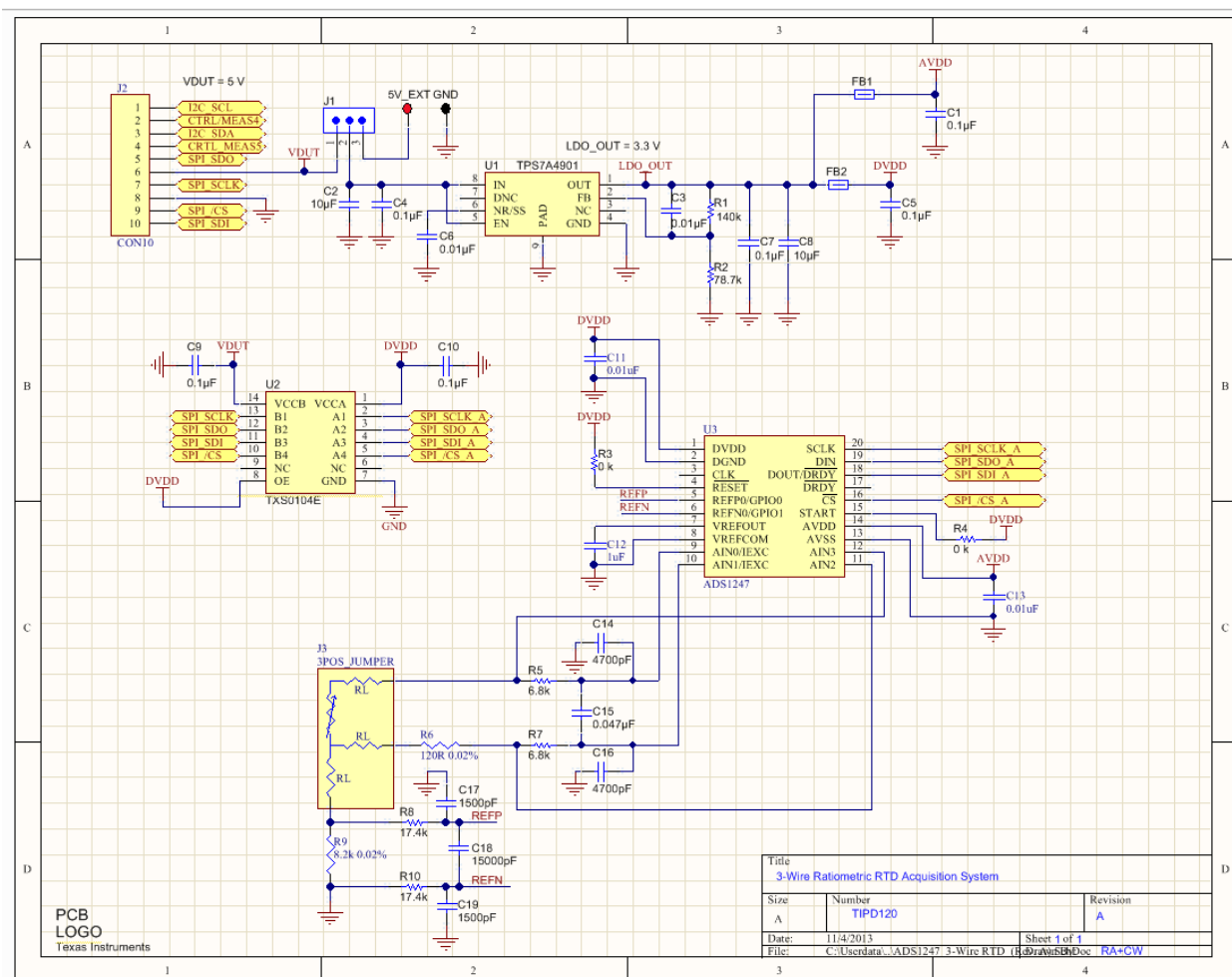


Figure 21. Electrical Schematic

A.2 Bill of Materials

Quantity	Value	Designator	Description	Manufacturer	Manufacturer Part Number	Digi-Key Part Number
6	0.1uF	C1, C4, C5, C7, C9, C10	CAP CER 0.1UF 50V 10% X7R 0603	MuRata	GRM188R71H104KA93D	490-1519-1-ND
2	10 uF	C2, C8	CAP CER 10UF 25V 20% X7R 1210	TDK	C3225X7R1E106M250AC	445-1434-1-ND
4	0.01 uF	C3, C6, C11, C13	CAP CER 10000PF 25V 5% NP0 0603	TDK	C1608C0G1E103J080AA	445-2664-1-ND
1	1 uF	C12	CAP CER 1UF 25V 10% X7R 0603	Taiyo Yuden	TMK107B7105KA-T	587-2984-1-ND
2	4700 pF	C14, C16	CAP CER 4700PF 25V 5% NP0 0603	TDK	C1608C0G1E472J080AA	445-2712-1-ND
1	0.047 uF	C15	CAP CER 0.047UF 25V 5% NP0 0805	Kemet	C0805C473J3GACTU	399-8092-1-ND
2	1500 pF	C17, C19	CAP CER 1500PF 50V 5% NP0 0603	TDK	C1608C0G1H152J080AA	445-1295-1-ND
1	15000 pF	C18	CAP CER 0.015UF 25V 5% NP0 0603	Kemet	C0603C153J3GACTU	399-10044-1-ND
1	140 k	R1	RES 140K OHM 1/10W 1% 0603 SMD	Vishey Dale	CRCW0603140KFKEA	541-140KHCT-ND
1	78.7 k	R2	RES 78.7K OHM 1/10W 1% 0603 SMD	Vishey Dale	CRCW060378K7FKEA	541-78.7KHCT-ND
2	0 k	R3, R4	RES 0.0 OHM 1/10W JUMP 0603 SMD	Panasonic Electronic Components	ERJ-3GEY0R00V	P0.0GCT-ND
2	6.8 k	R5, R7	RES 6.80K OHM 1/8W 1% SMD 0603	Vishey Beyschlag	MCT06030C6801FP500	MCT0603-6.80K-CFCT-ND
1	120	R6	RES 120 OHM 1/10W .02% 0603	Susumu	RG1608V-121-P-T1	RG1608V120PCT-ND
2	17.4 k	R8, R10	RES 17.4K OHM 1/10W 1% 0603	Stackpole Electronics	RMCF0603FT17K4	RMCF0603FT17K4CT-ND
1	8.2 k	R9	RES 8.2K OHM 1/8W .02% 0805	Susumu	RG2012V-822-P-T1	RG2012V8.2KPCT-ND
1	Red	TP1	Test Point, TH, Compact, Red	Keystone	5005	5005K-ND
1	Black	TP2	Test Point, TH, Compact, Black	Keystone	5006	5006K-ND
1		U1	IC REG LDO ADJ 0.15A 8MSO	Texas Instruments Inc	TPS7A4901DGNR	296-27751-1-ND
1		U2	IC 4BIT NONINV TRANSLTR 14TSSOP	Texas Instruments Inc	TXS0104EPWR	296-20697-1-ND
1		U3	IC ADC 24BIT DEL/SIG LN 20TSSOP	Texas Instruments Inc	ADS1247IPW	296-24293-5-ND
2		FB1, FB2	FERRITE CHIP 600 OHM 200MA 0603	MuRata	BLM18HG601SN1D	490-1033-6-ND
1		J1	CONN HEADER 3POS .100" SGL GOLD	Samtec, Inc.	TSW-103-07-G-S	SAM1029-03-ND
0.2		J2	CONN SOCKET 50PIN .050 R/A SINGL	Mill-Max Manufacturing Corp.	851-43-050-20-001000	ED90278-ND
1		J3	TERMINAL BLOCK 3.5MM 3POS PCB	On Shore Technology Inc	ED555/3DS	ED1515-ND
Note: J2 is a 10-pin connector socket. The 50-pin connector sockets will have to be cut down, 1 is enough to supply 5 boards.						

Figure 22. Bill of Materials

A.3 Additional PT-100 RTD Information

For positive temperatures the CVD equations is a 2nd-order polynomial Equation 26.

$$RTD(T) = R_0 \times [1 + A(T) + B(T)^2] \quad (29)$$

For negative temperatures from -200 °C to 0 °C, the CVD equation expands to a 4th-order polynomial shown in Equation 27.

$$RTD(T) = R_0 \times [1 + A(T) + B(T)^2 + C(T)^3 \times (T - 100)] \quad (30)$$

The coefficients in the Calendar Van-Dusen equations are defined by the IEC-60751 standard. R_0 is the resistance of the RTD at 0 °C. For a PT-100 RTD with an alpha (α) of 0.00385, the coefficients are:

$$\begin{aligned} R_0 &= 100 \, \Omega \\ A &= 3.9083 \times 10^{-3} \, ^\circ\text{C}^{-1} \\ B &= -5.775 \times 10^{-7} \, ^\circ\text{C}^{-1} \\ C &= -4.183 \times 10^{-12} \, ^\circ\text{C}^{-1} \end{aligned} \quad (31)$$

The change in resistance of a PT-100 RTD from 0 °C – 100 °C is displayed in Figure 23.

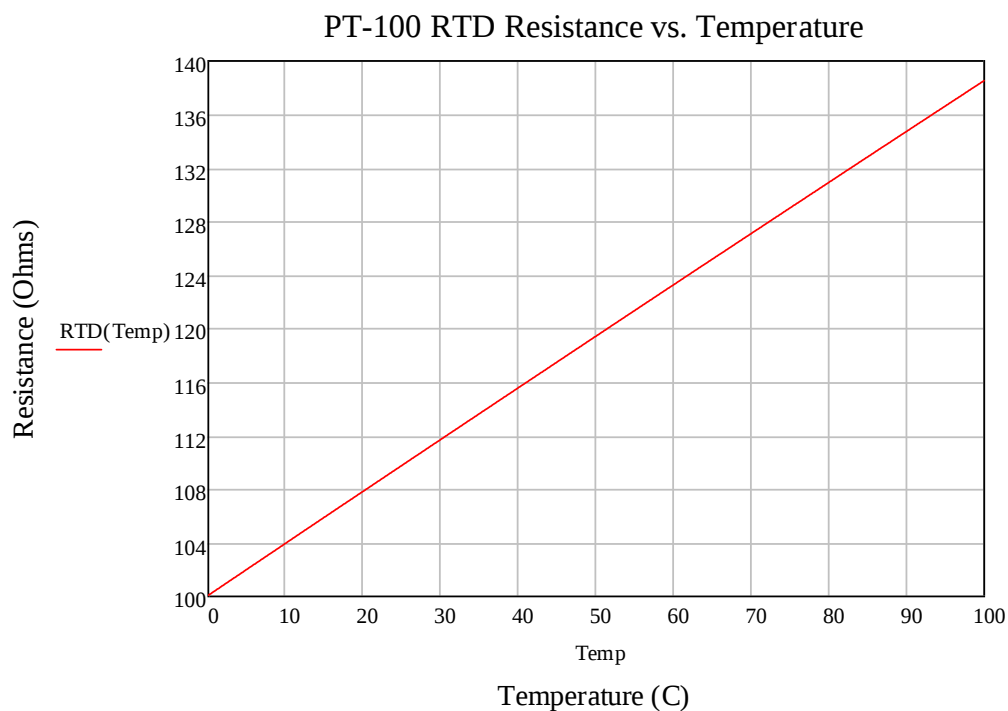


Figure 23. PT-100 RTD Resistance from 0 °C – 100 °C

While the change in RTD resistance is fairly linear over small temperature ranges, Figure 24 displays the resulting non-linearity if an end-point fit is made to the curve shown in Figure 23. The results show roughly 0.375% non-linearity and illustrate the need for digital calibration.

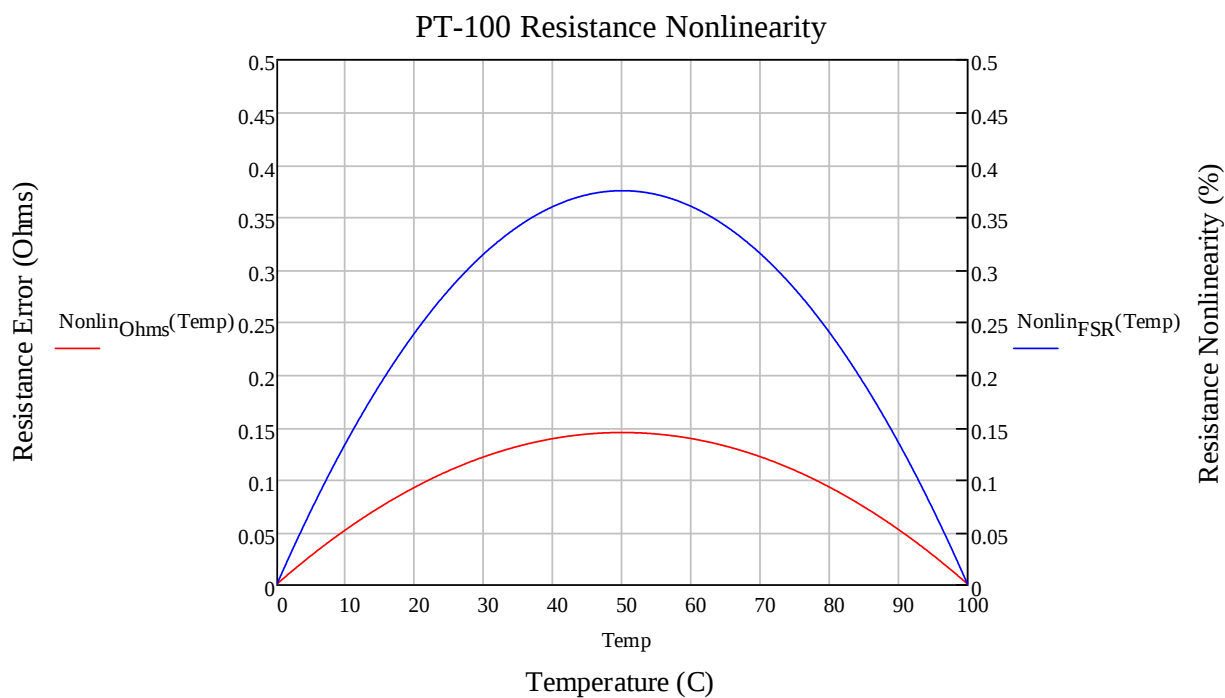


Figure 24. PT-100 RTD Non-Linearity from 0 °C – 100 °C

A.4 Additional Simulated Data

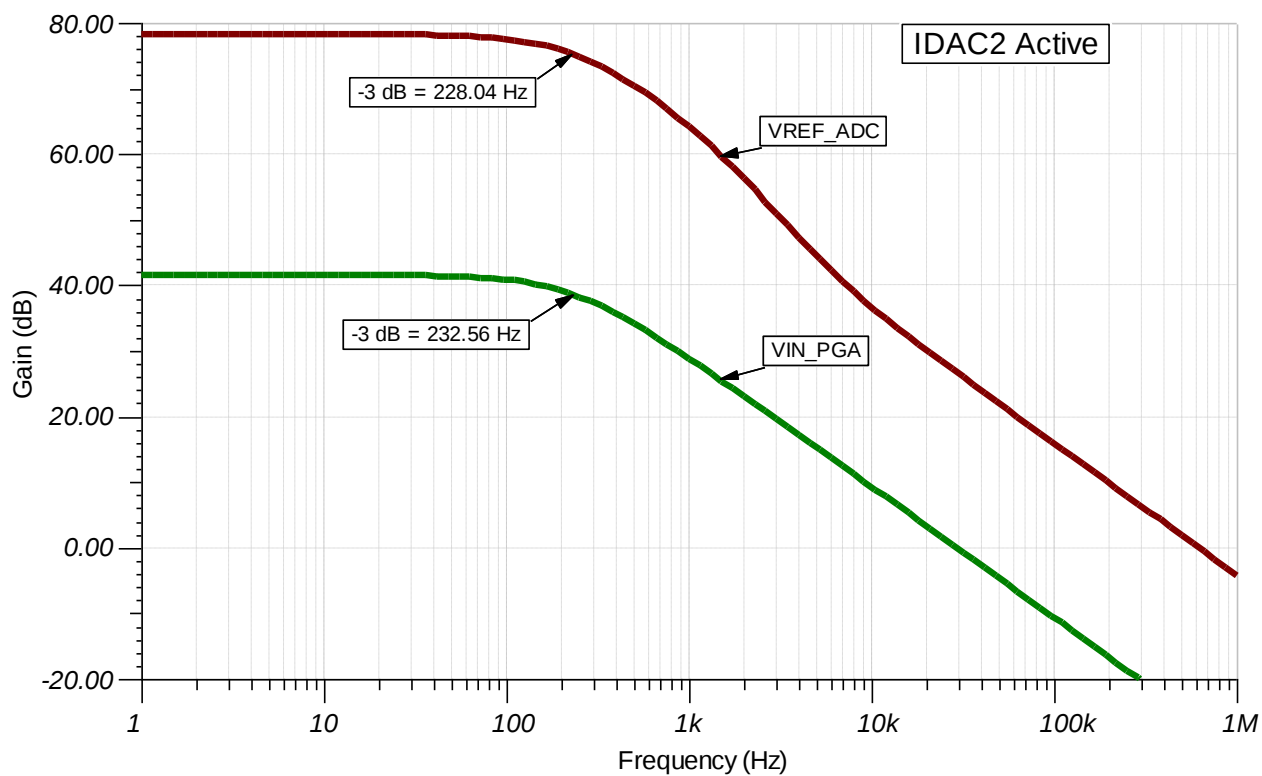


Figure 25. Input Filter Frequency Response with IDAC2 Active

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