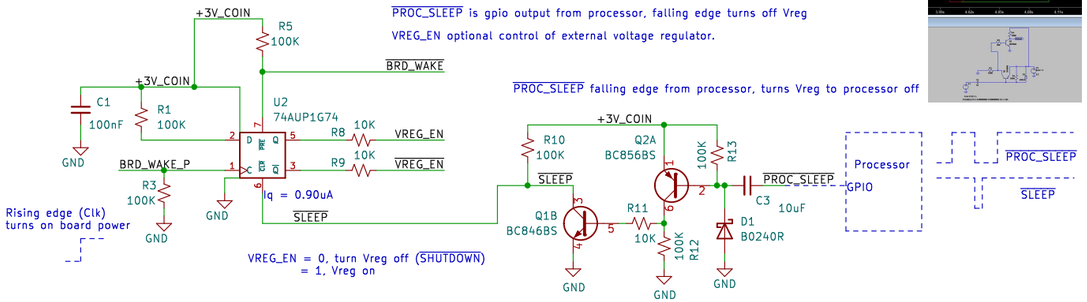
RTC with board power control for Sleep / Wake

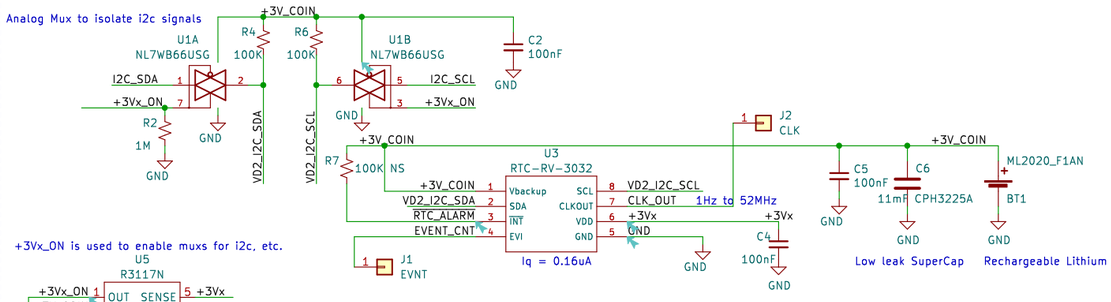


BRD_WAKE (Preset#) = 0, turns on board power

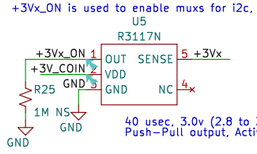
PROC_SLEEP is gpio output from processor, falling edge turns off Vreg

VREG_EN optional control of external voltage regulator.

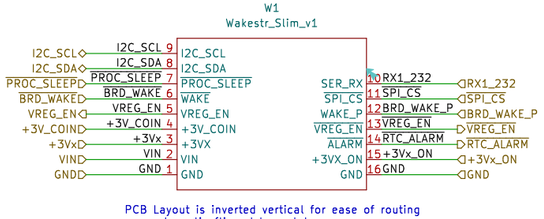
PROC_SLEEP falling edge from processor, turns Vreg to processor off



+3Vx_ON is used to enable muxs for i2c, etc.



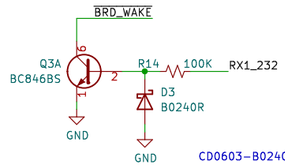
40 usec, 3.0v (2.8 to 3.2), Iq=0.3uA
Push-Pull output, Active Lo



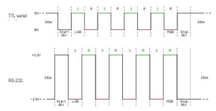
PCB Layout is inverted vertical for ease of routing
– schematic flipped to match.

Can't use TLV840 as there are no push-pull output available in <100usec delay
Use R3111N282C-TR-FE or
R3117K313C-TR (0.3uA)

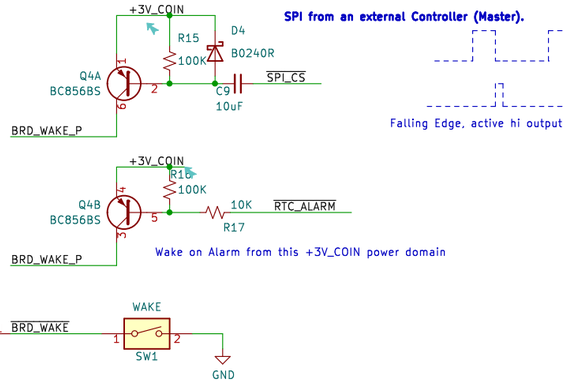
Wake on RTC Alarm, SPI_CS, 1x rs232 Rx Serial



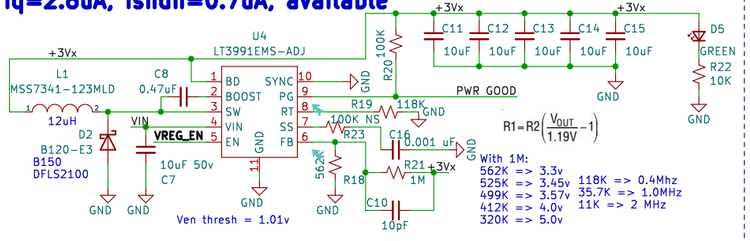
RS232 RX Console wakeup –12v to +12v, typical –5v to +5v



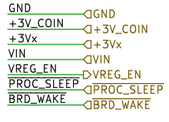
Wake on SPI_CS or TTL Serial RX from another +3V3 power domain



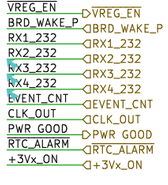
Switching Regulator +3v3 @ 1.2amp, Iq=2.8uA, Ishdn=0.7uA, available



Minimum Viable Interface



Optional signals



Board level Sleep:
- Processor/+3v3 Vreg is turned off by processor active low gpio (PROC_SLEEP)
- Wake on RTC interrupt. Processor programs wakeup time before sleep
- Wake on r232 serial console rx
- Wake on SPI chip select or TTL serial rx(active low)
- Wake on button push
- Low shutdown current 3.3v 1.2 amp voltage regulator 4.5v to 50v input, Ishdn=0.7uA
- Ishdn = 3.06uA = 0.9uA (74aup1g74) + 0.16uA (RV-3032) + 0.3uA (R3117) + + 1uA (nl7WB66) + 0.7uA (LT3991 Vreg)

Board Sleep Wake Notes:
- Open Collector/Drain Wake circuits have almost no leakage (<100nA)
- esd protect pins?
- Would be great to switch Vin on/off by RTC_Alarm, etc.