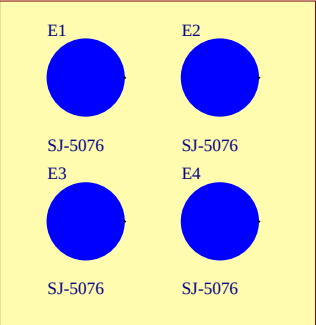
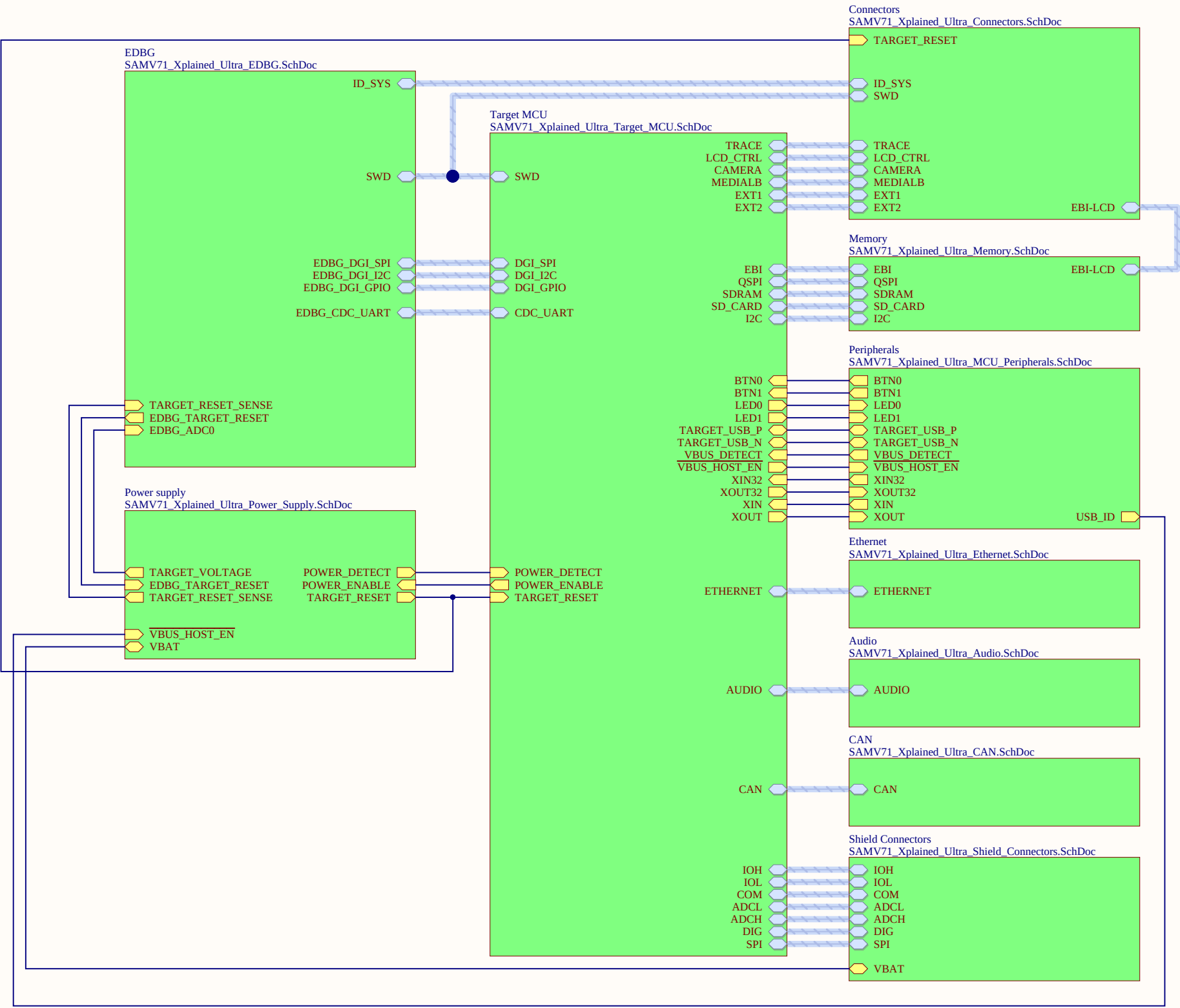


SAM V71 Xplained Ultra



LABEL1

Product number/revision
Serial number

Label PCBA (ES)

PCB1: A08-2216 SAM V71 Xplained Ultra PCB Documentation

PCBADOC1: A12-0950

TESTDOC1: A12-0951

FW1: A11-0196

TEST1: A11-0280

Vin has to be 12V when MediaLB extensions are used.

When Vin = 5V the regulator uses a 100% duty-cycle mode (passthrough).

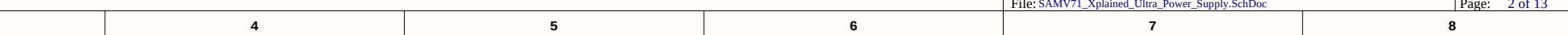
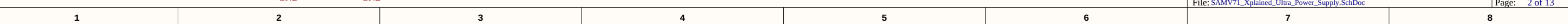
VCC_EXT_P5V0:
This power input can be used to power the whole board and it has a higher priority as the USB power inputs. Connect a power supply if a target MCU with USB host is present and VCC_EXT_P5V0_P17V0 is not used. 4.3V to 5.5V is possible but for USB host operation and in case on-board devices use this voltage it should be 5V $\pm$ 2%.

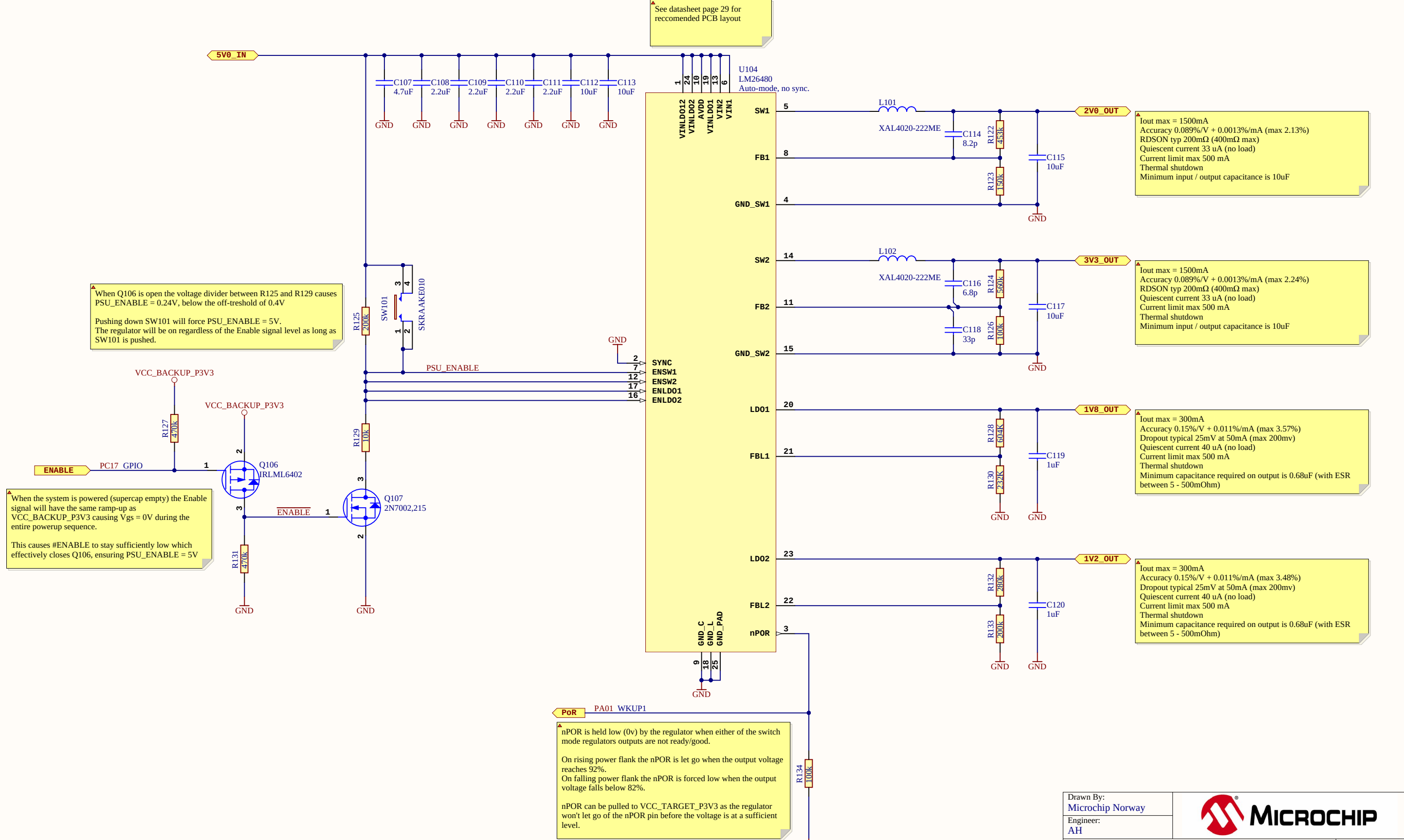
VCC_TARGET_USB_P5V0:
Target MCU USB power input. It is used to power the whole board when no other 5V power supply is present.

VCC_P3V3: Regulated 3.3V from VCC_P5V0
VCC_P2V0: Regulated 2.0V from VCC_P5V0
VCC_P1V8: Regulated 1.8V from VCC_P5V0
VCC_P1V2: Regulated 1.2V from VCC_P5V0

[illegible]

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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See datasheet page 29 for recommended PCB layout

When Q106 is open the voltage divider between R125 and R129 causes PSU_ENABLE = 0.24V, below the off-threshold of 0.4V
Pushing down SW101 will force PSU_ENABLE = 5V.
The regulator will be on regardless of the Enable signal level as long as SW101 is pushed.

When the system is powered (supercap empty) the Enable signal will have the same ramp-up as VCC_BACKUP_P3V3 causing Vgs = 0V during the entire powerup sequence.
This causes #ENABLE to stay sufficiently low which effectively closes Q106, ensuring PSU_ENABLE = 5V

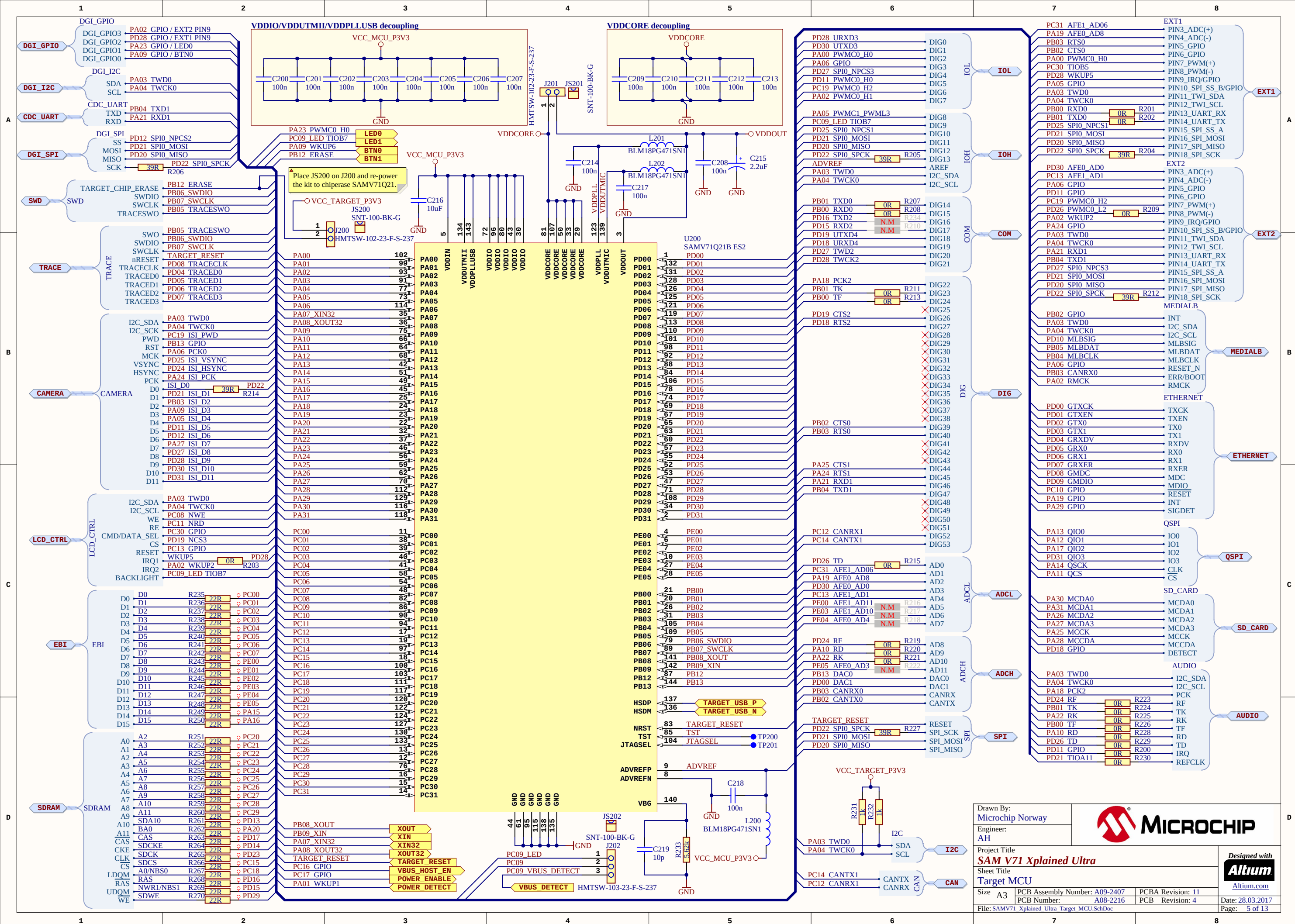
Iout max = 1500mA
Accuracy 0.089%/V + 0.0013%/mA (max 2.13%)
RDSOn typ 200mΩ (400mΩ max)
Quiescent current 33 uA (no load)
Current limit max 500 mA
Thermal shutdown
Minimum input / output capacitance is 10uF

Iout max = 1500mA
Accuracy 0.089%/V + 0.0013%/mA (max 2.24%)
RDSOn typ 200mΩ (400mΩ max)
Quiescent current 33 uA (no load)
Current limit max 500 mA
Thermal shutdown
Minimum input / output capacitance is 10uF

Iout max = 300mA
Accuracy 0.15%/V + 0.011%/mA (max 3.57%)
Dropout typical 25mV at 50mA (max 200mv)
Quiescent current 40 uA (no load)
Current limit max 500 mA
Thermal shutdown
Minimum capacitance required on output is 0.68uF (with ESR between 5 - 500mOhm)

Iout max = 300mA
Accuracy 0.15%/V + 0.011%/mA (max 3.48%)
Dropout typical 25mV at 50mA (max 200mv)
Quiescent current 40 uA (no load)
Current limit max 500 mA
Thermal shutdown
Minimum capacitance required on output is 0.68uF (with ESR between 5 - 500mOhm)

nPOR is held low (0v) by the regulator when either of the switch mode regulators outputs are not ready/good.
On rising power flank the nPOR is let go when the output voltage reaches 92%.
On falling power flank the nPOR is forced low when the output voltage falls below 82%.
nPOR can be pulled to VCC_TARGET_P3V3 as the regulator won't let go of the nPOR pin before the voltage is at a sufficient level.



Verification showed: 4.7pF
Accuracy: 5.2 ppm
Startup time: 400 ms to reach full swing
with a 9.5pF probe connected to the
crystal.
Safety factor: Above 5.5

The schematic diagram illustrates the electrical connection between the XOUT pin of the Xilinx device and the XIN pin of the Altera device. The signal path is as follows:

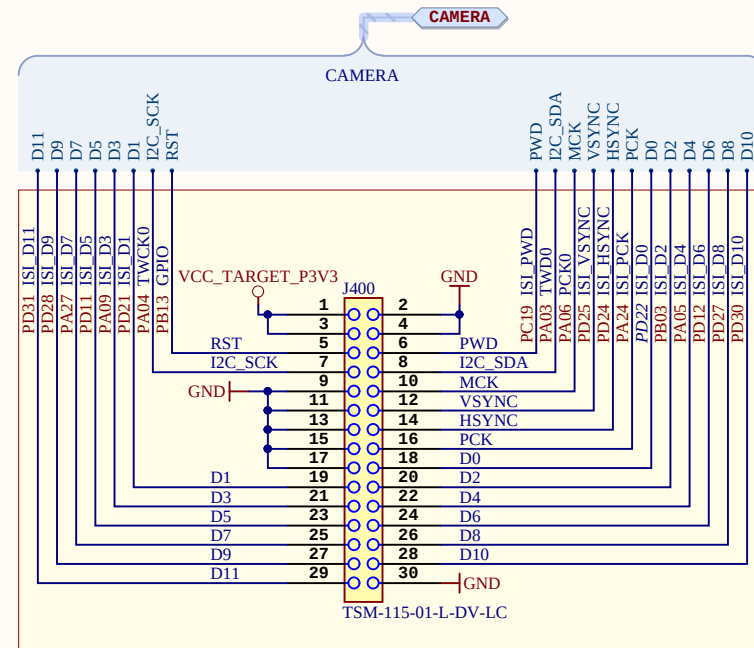
- XOUT** (pin 10) is connected to the **PB08_XOUT** pin of the Xilinx device.
- The signal then passes through a buffer, **J301** (pin 10), which is connected to the **PB09_XIN** pin of the Xilinx device.
- The signal continues through a 12.00MHz crystal, **XC301** (pin 10), which is connected to the **PB09_XIN** pin of the Altera device.
- The signal then passes through a 12pF capacitor, **C303** (pin 10), which is connected to the **XIN** pin of the Altera device.
- Two 12pF capacitors, **C302** and **C303**, are connected to ground from the nodes before and after the crystal, respectively, to provide proper termination and filtering.

Verification showed: 12.0pF
Accuracy 5 ppm
Startup: full swing after 850 μ s (first clock after 451 μ s)
Safety factor: Above 5.5

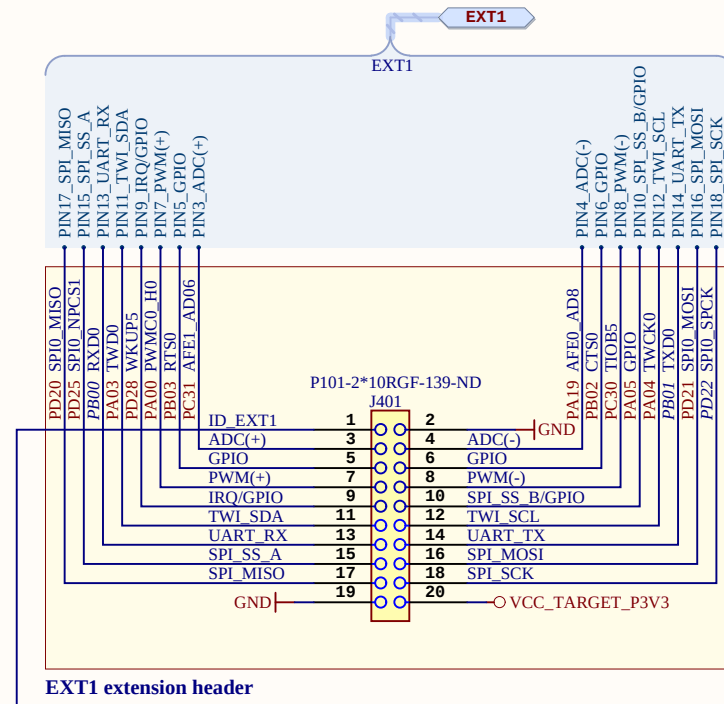
[illegible]

▲ PC16 is connected to the USB_ID signal and can be used to check if an OTG cable or a host mode cable is connected. These cables will pull the USB_ID signal low and enable the power switch to supply voltage to the connected USB device. Pulling PC16 low will also enable the power switch.

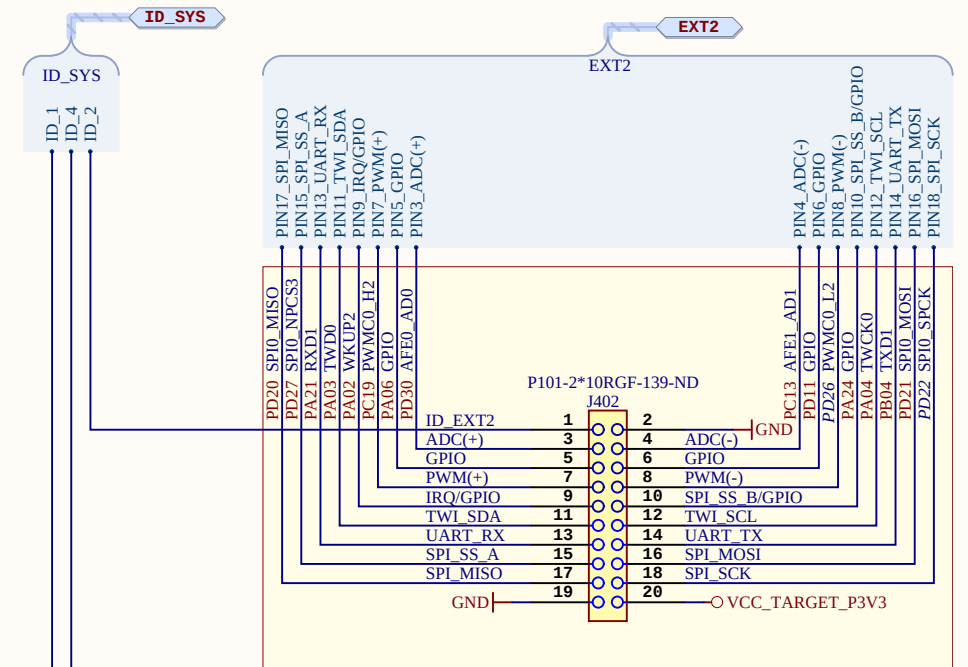
Drawn By: Microchip Norway		 MICROCHIP	
Engineer: AH			
Project Title <i>SAM V71 Xplained Ultra</i>			Designed with  Altium.com
Sheet Title Target MCU Peripherals			
Size A3	PCB Assembly Number: A09-2407 PCB Number: A08-2216	PCBA Revision: 11 PCB Revision: 4	
File: SAMV71_Xplained_Ultra_MCU_Peripherals.SchDoc			Date: 28.03.2017 Page: 6 of 13



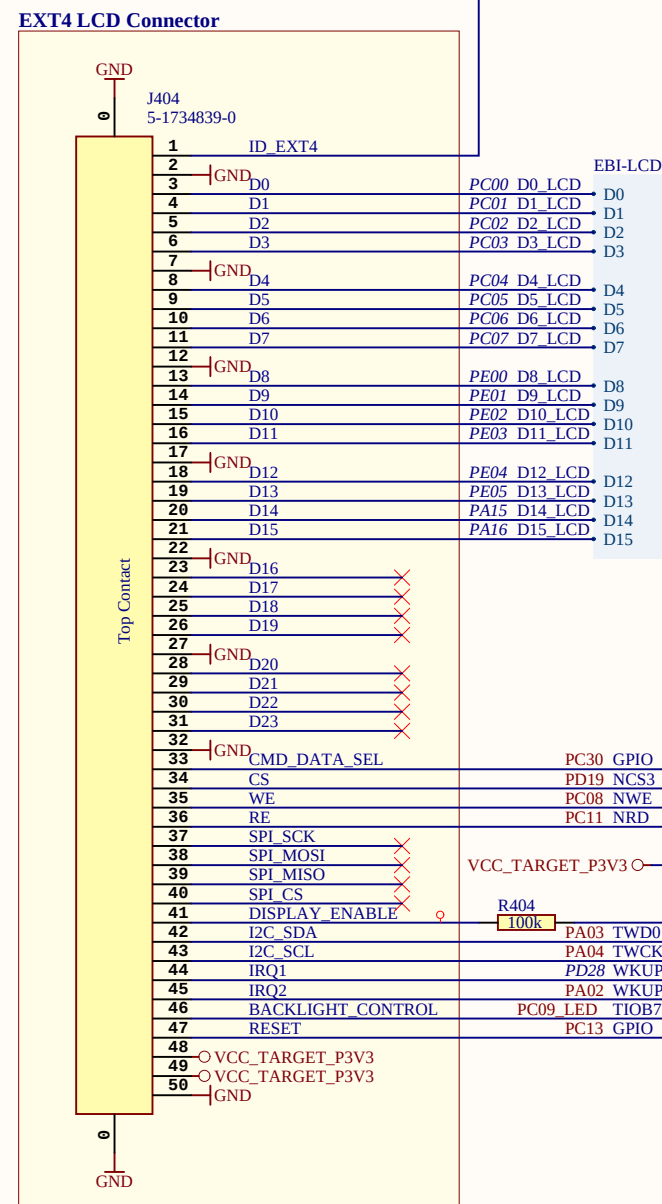
Camera Interface Connector



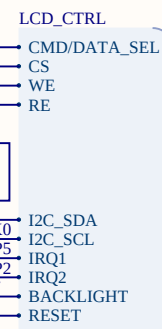
EXT1 extension header



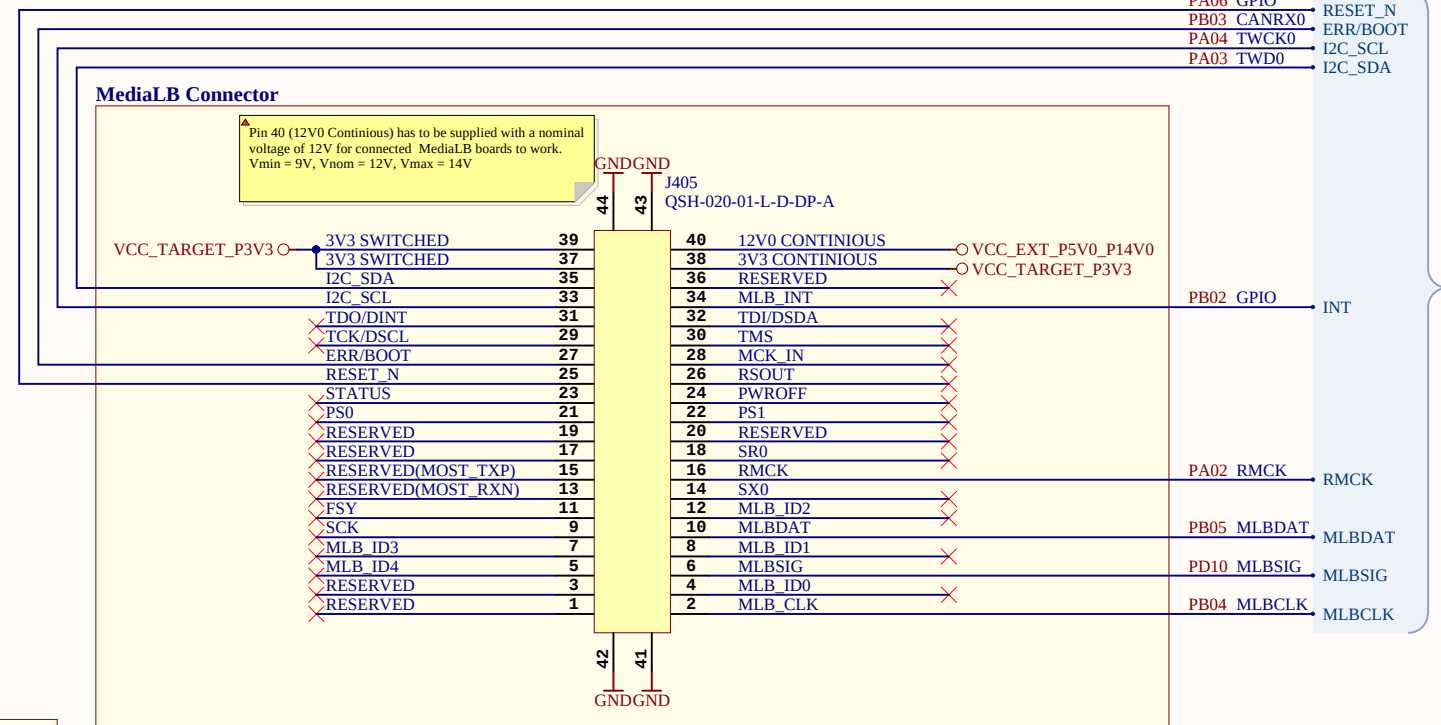
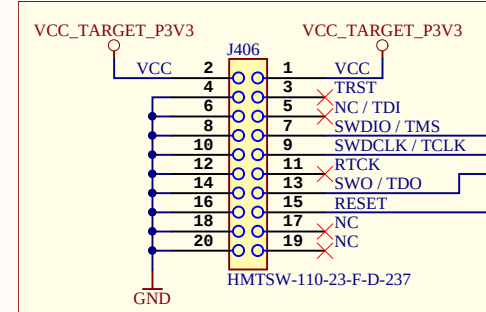
EXT2 extension header



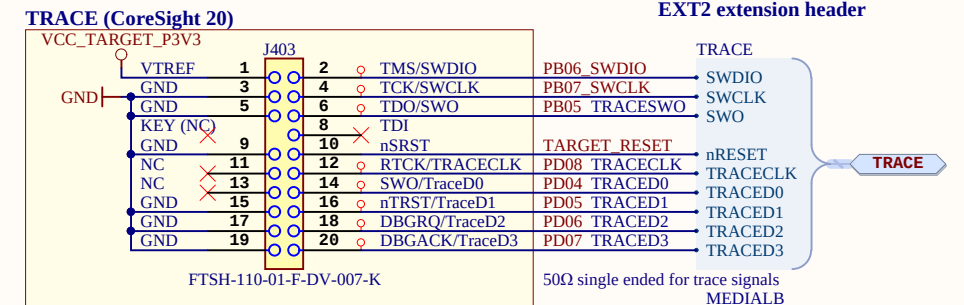
EBI - LCD



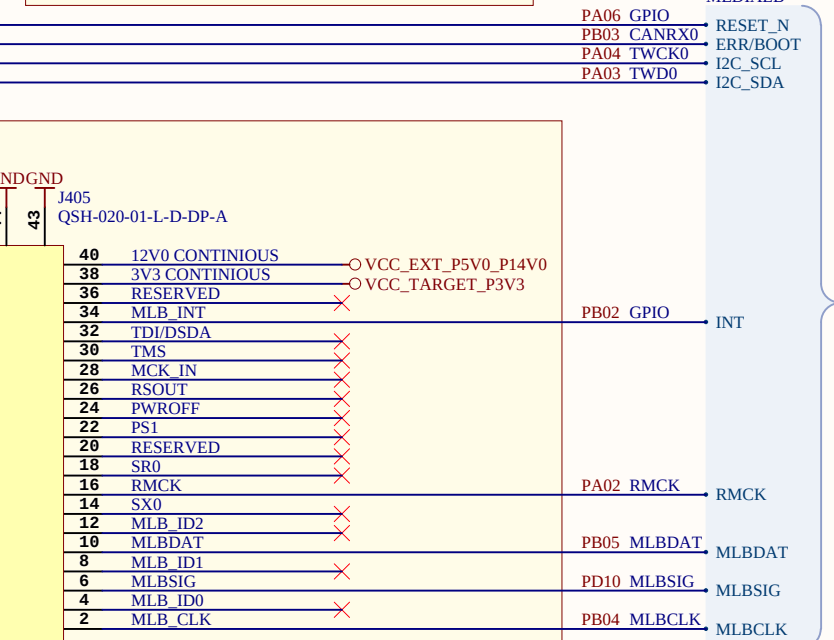
ARM JTAG



MediaLB Connector

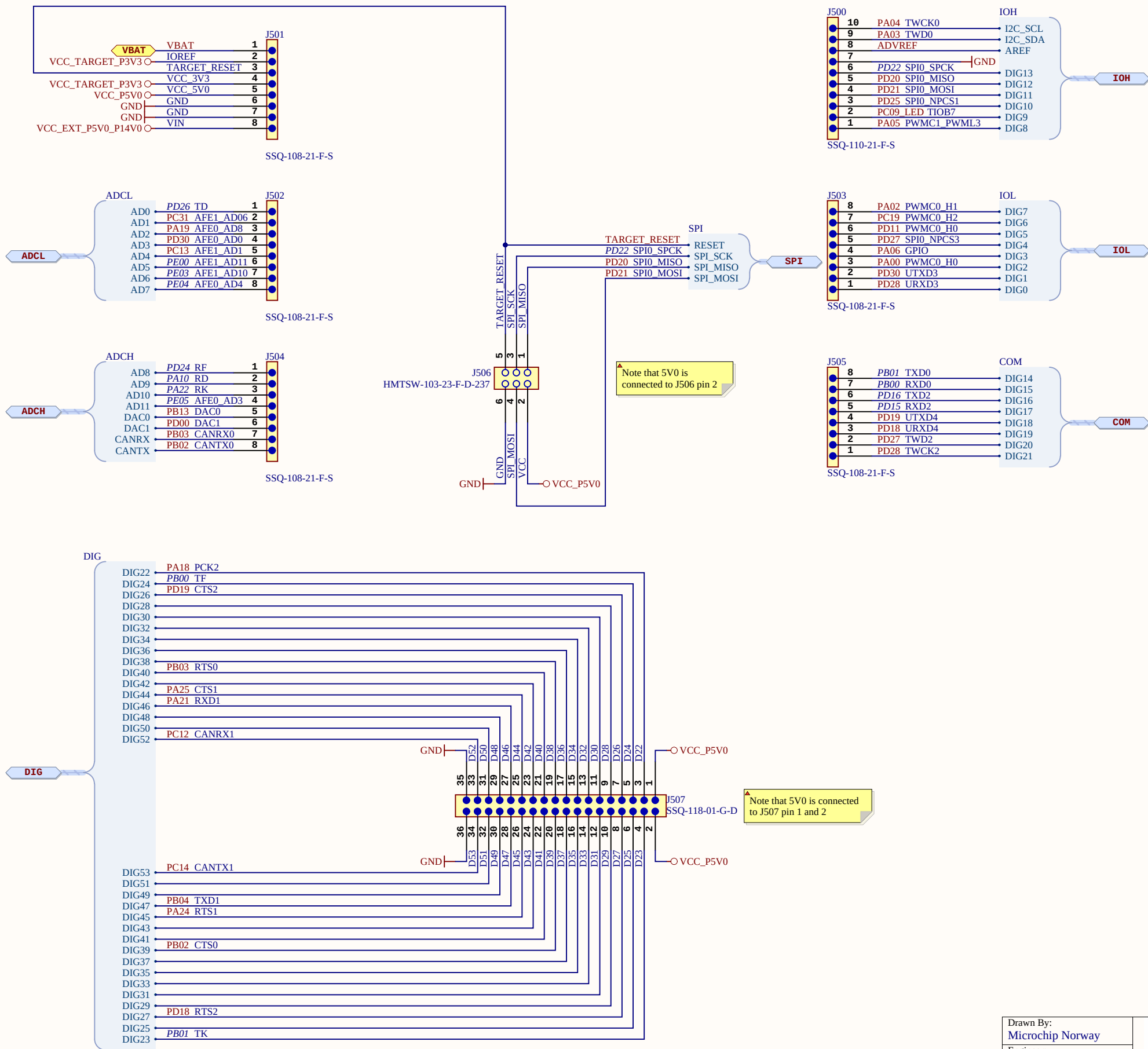


TRACE (CoreSight 20)



TRACE

MEDIALB



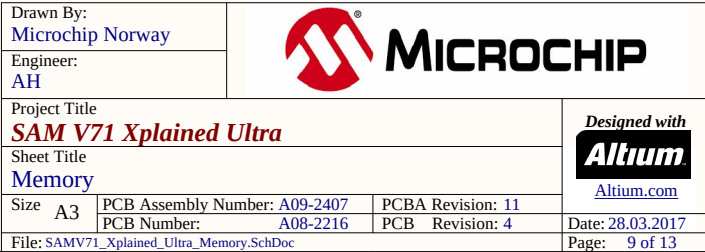
Drawn By:
Microchip Norway
Engineer:
AH

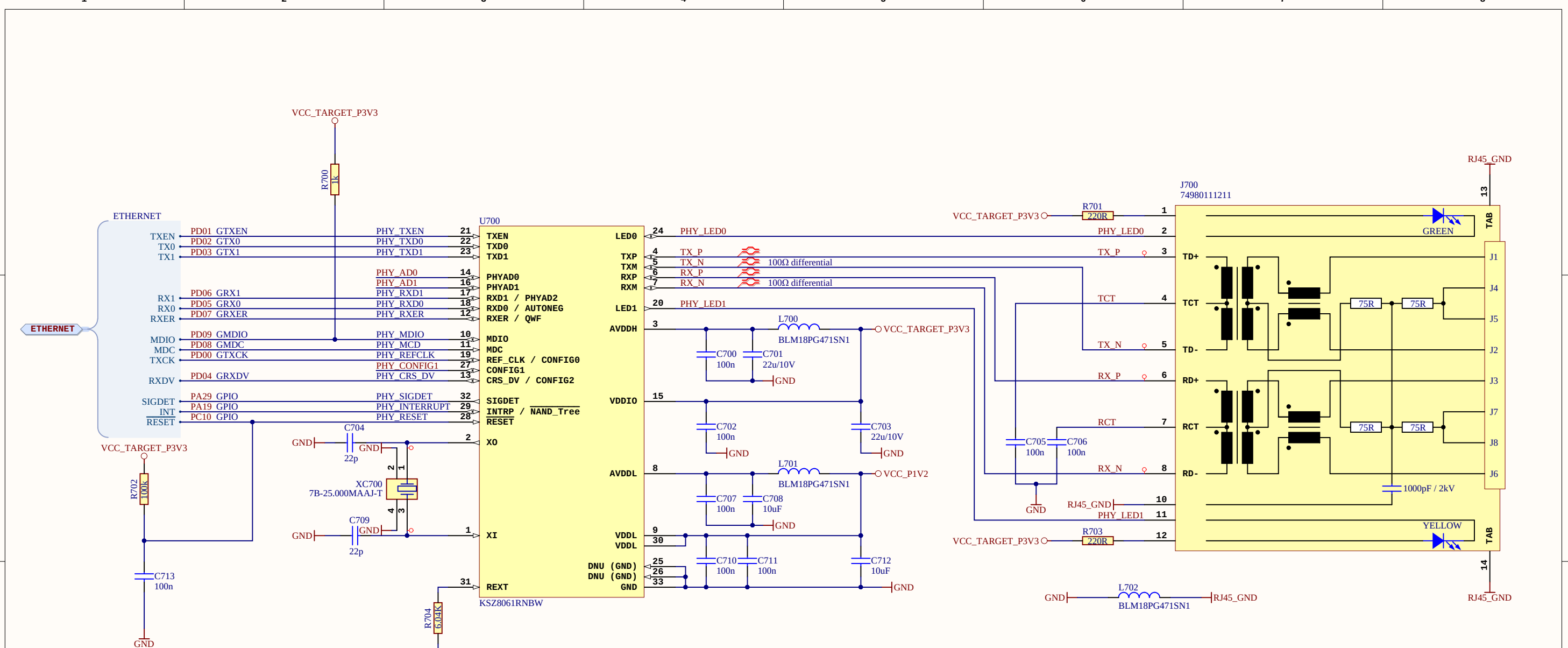


Project Title
SAM V71 Xplained Ultra
Sheet Title
Shield Connectors

Designed with
Altium
Altium.com

Size A3	PCB Assembly Number: A09-2407	PCBA Revision: 11
	PCB Number: A08-2216	PCB Revision: 4
File: SAMV71_Xplained_Ultra_Shield_Connectors.SchDoc		Page: 8 of 13





When the KSZ8061RNBW is released from reset the configuration values on the pins are latched into the PHY's registers.

▲ PHYAD[2:0] is used to set the PHY's address:
001 (default on board)
010
....
110
111

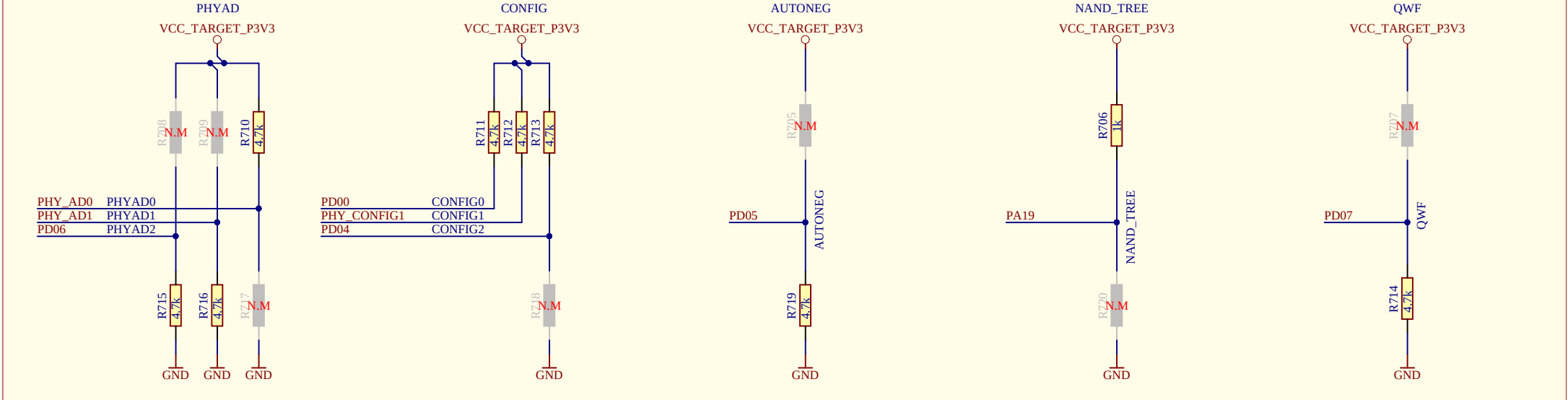
▲ CONFIG[2:0] is used to select operation mode.
001 = RMII normal, MDI/MDI-X disabled
101 = RMII back to back
111 = RMII normal MDI/MDI-X enabled
Not configurable on board as back to back

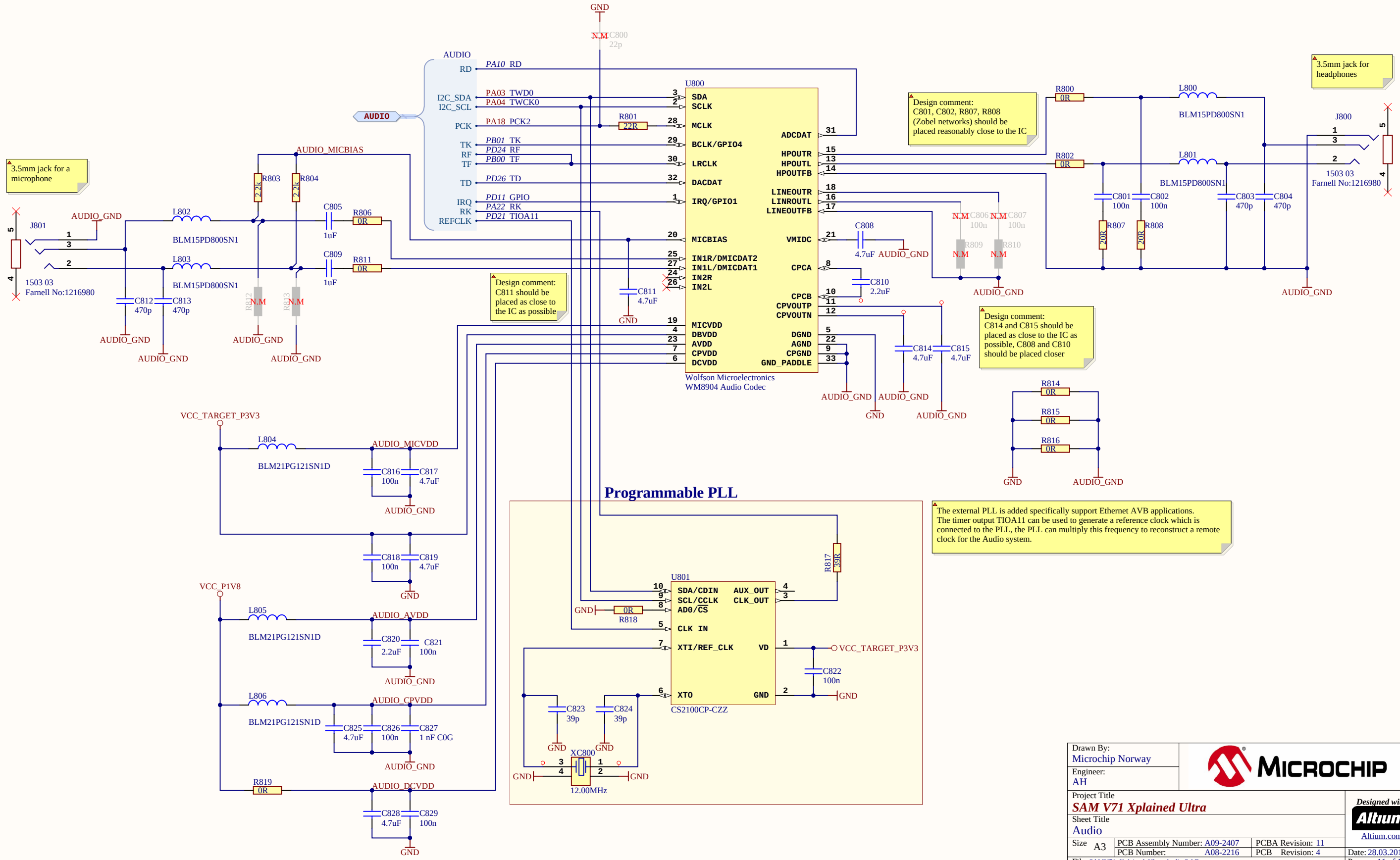
▲ AUTONEG is used to select if auto negotiation of link speed should be enabled.
1 = disable Auto-Negotiation
0 = enable Auto-Negotiation (default on board)

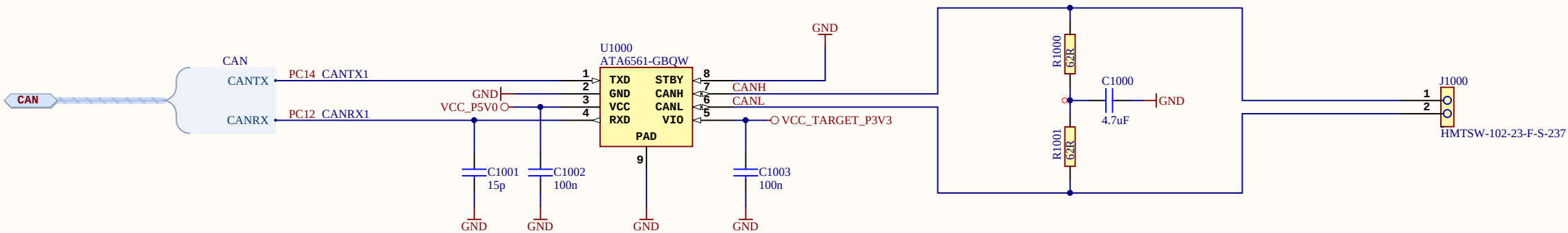
▲ NAND_TREE enables a test mode for all pins connected to the SAMV71Q21.
1 = Disable NAND_TREE (default on board)
0 = Enable NAND_TREE

▲ QWF is used to enable/disable Quiet-WIRE Filtering
1 = Disale Quiet-WIRE Filtering
0 = Enable Quiet-WIRE Filtering (default on board)

PHY Configuration







Drawn By:
Microchip Norway
Engineer:
AH

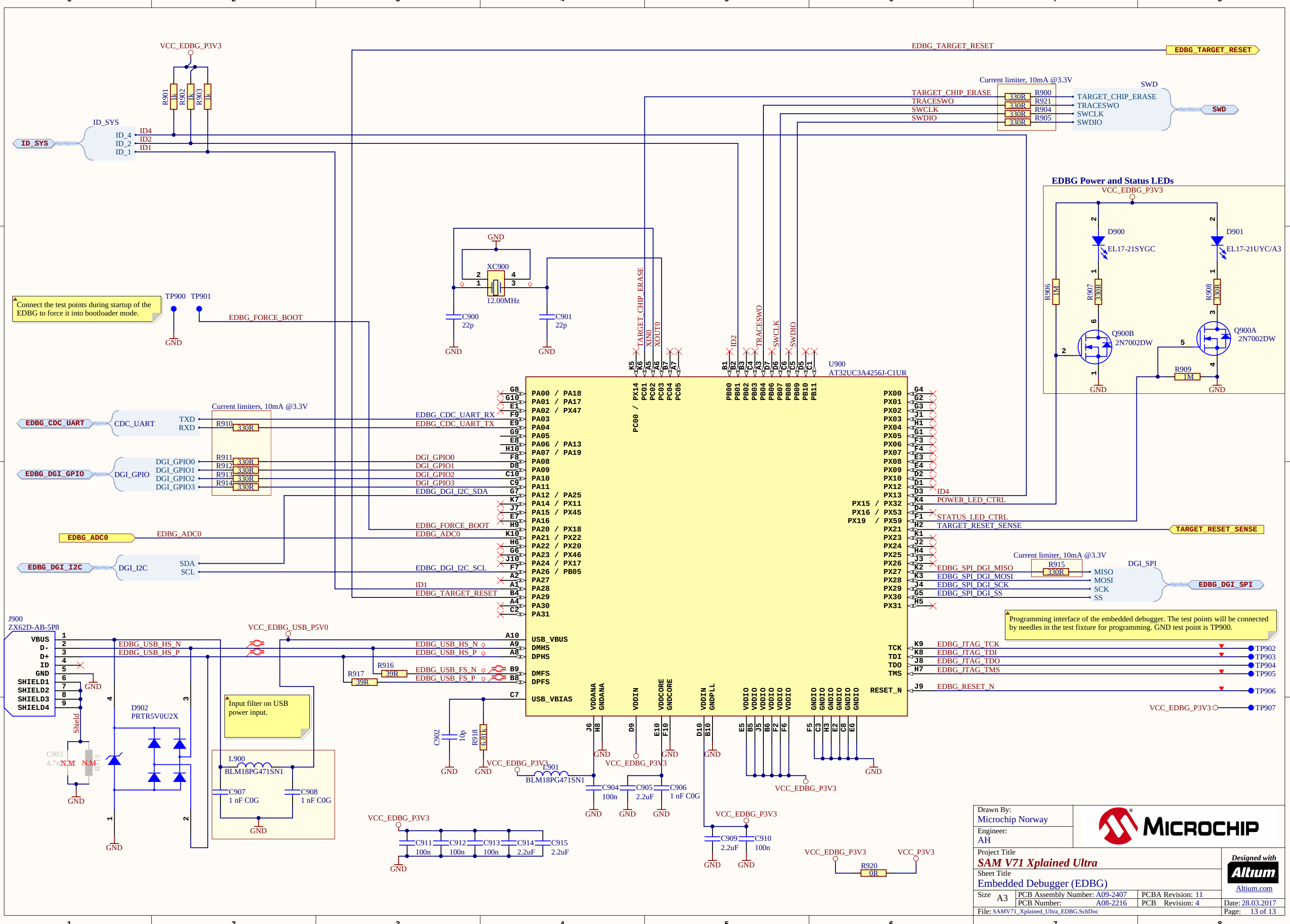


Project Title
SAM V71 Xplained Ultra
Sheet Title
CAN

Designed with
Altium
Altium.com

Size A3	PCB Assembly Number: A09-2407	PCBA Revision: 11	Date: 28.03.2017
	PCB Number: A08-2216	PCB Revision: 4	Page: 12 of 13

File: SAMV71_Xplained_Ultra_CAN.SchDoc



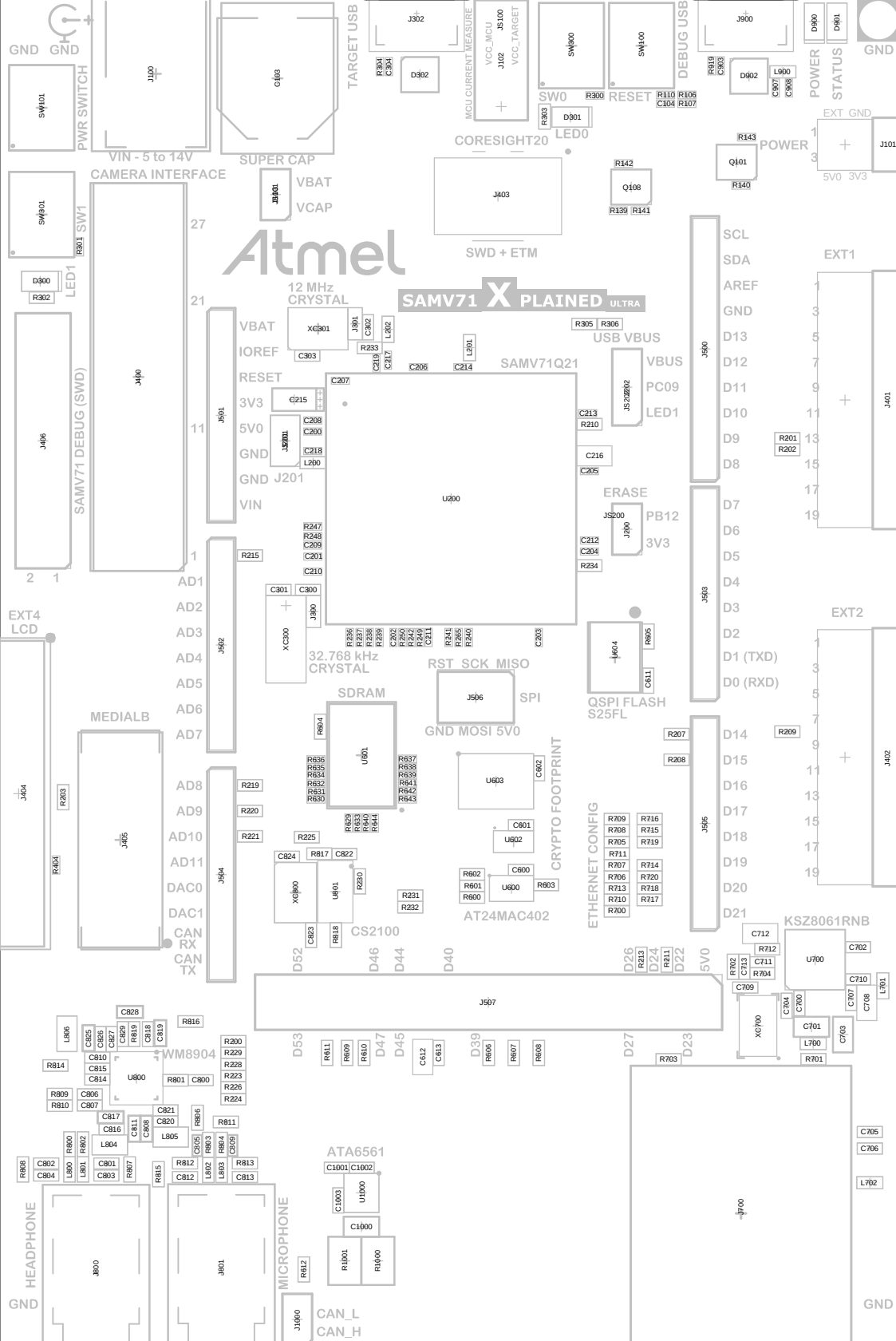
Drawn By:
Microchip Norway
Engineer:
AH



Project Title
SAM V71 Xplained Ultra
Sheet Title
Embedded Debugger (EDBG)

Designed with
Altium
Altium.com

Size A3	PCB Assembly Number: A09-2407	PCBA Revision: 11
PCB Number: A08-2216	PCB Revision: 4	Date: 28.03.2017
File: SAMV71_Xplained_Ultra_EDBG.SchDoc		Page: 13 of 13



Atmel

SAMV71 X PLAINED ULTRA

SAMV71Q21

32.768 kHz CRYSTAL

SDRAM

GND MOSI 5V0

RST SCK MISO

SPI

CRYPTO FOOTPRINT

ERASE

QSPI FLASH S25FL

ETHERNET CONFIG

AT24MAC402

CS2100

MEDIA L B

CAMERA INTERFACE

SUPER CAP

TARGET USB

CORESIGHT20

DEBUG USB

EXT4 LCD

EXT1

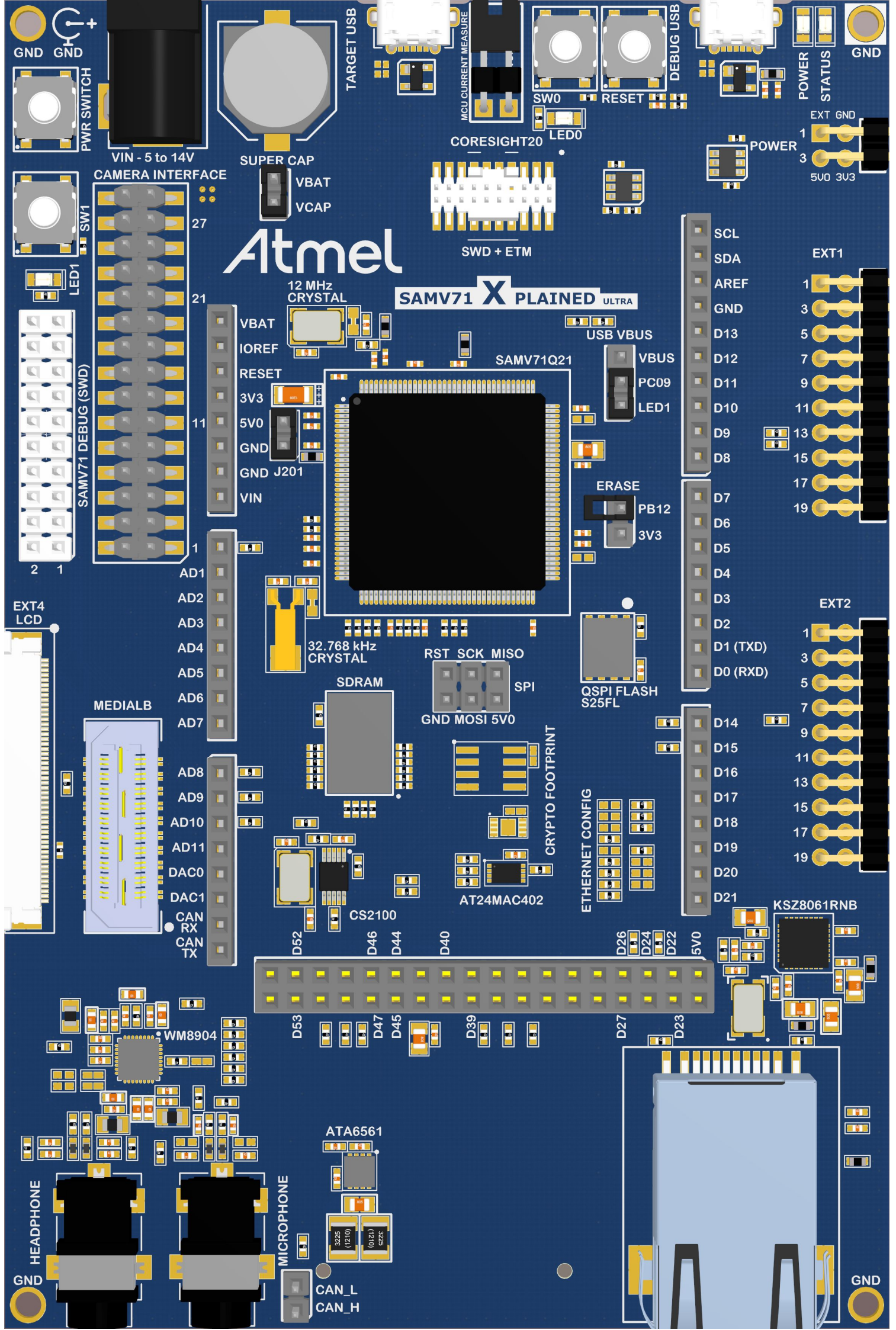
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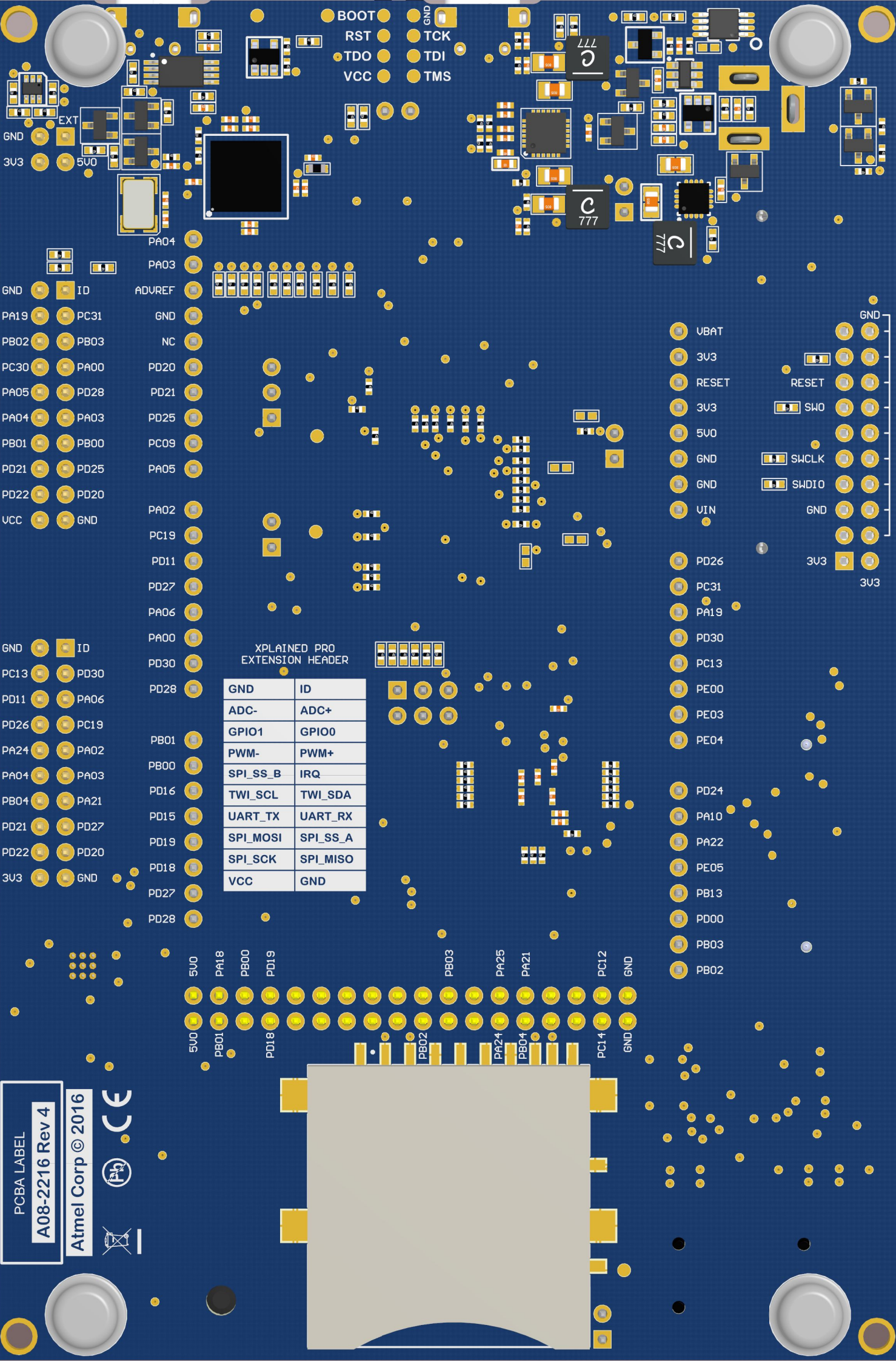
HEADPHONE

MICROPHONE

GND

GND





PCBA LABEL
A08-2216 Rev 4
Atmel Corp © 2016



BOOT
RST
TDO
VCC
TCK
TDI
TMS

PA04
PA03
GND
ID
PA19
PB02
PC30
PA05
PA04
PB01
PD21
PD22
VCC
GND

GND
PC13
PD11
PD26
PA24
PA04
PB04
PD21
PD22
3V3
GND
PD30
PA06
PC19
PA02
PA03
PA21
PD27
PD20
GND
PD28

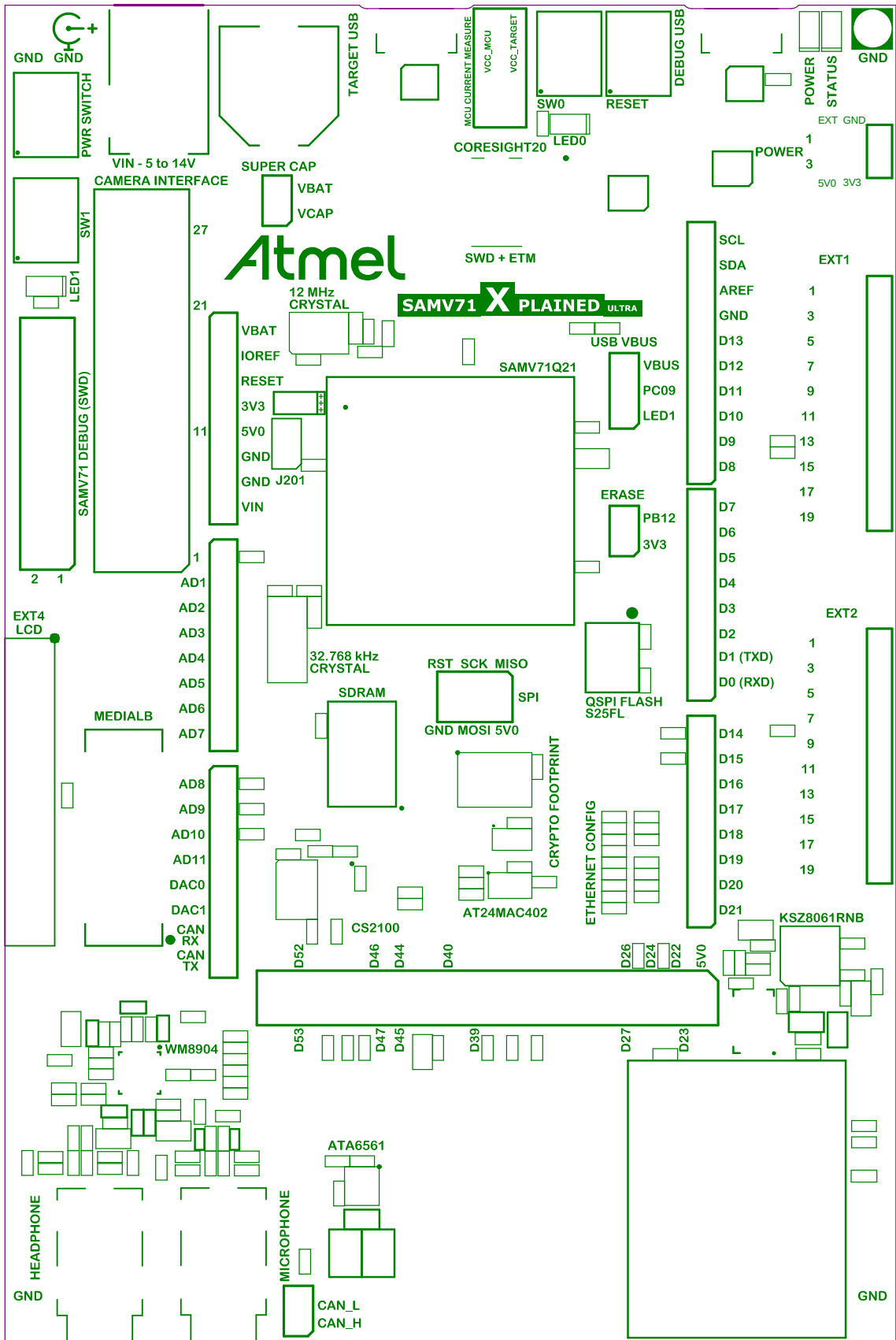
ADUREF
GND
NC
PD20
PD21
PD25
PC09
PA05
PA02
PC19
PD11
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PA06
PA00
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PD28
PB01
PB00
PD16
PD15
PD19
PD18
PD27
PD28

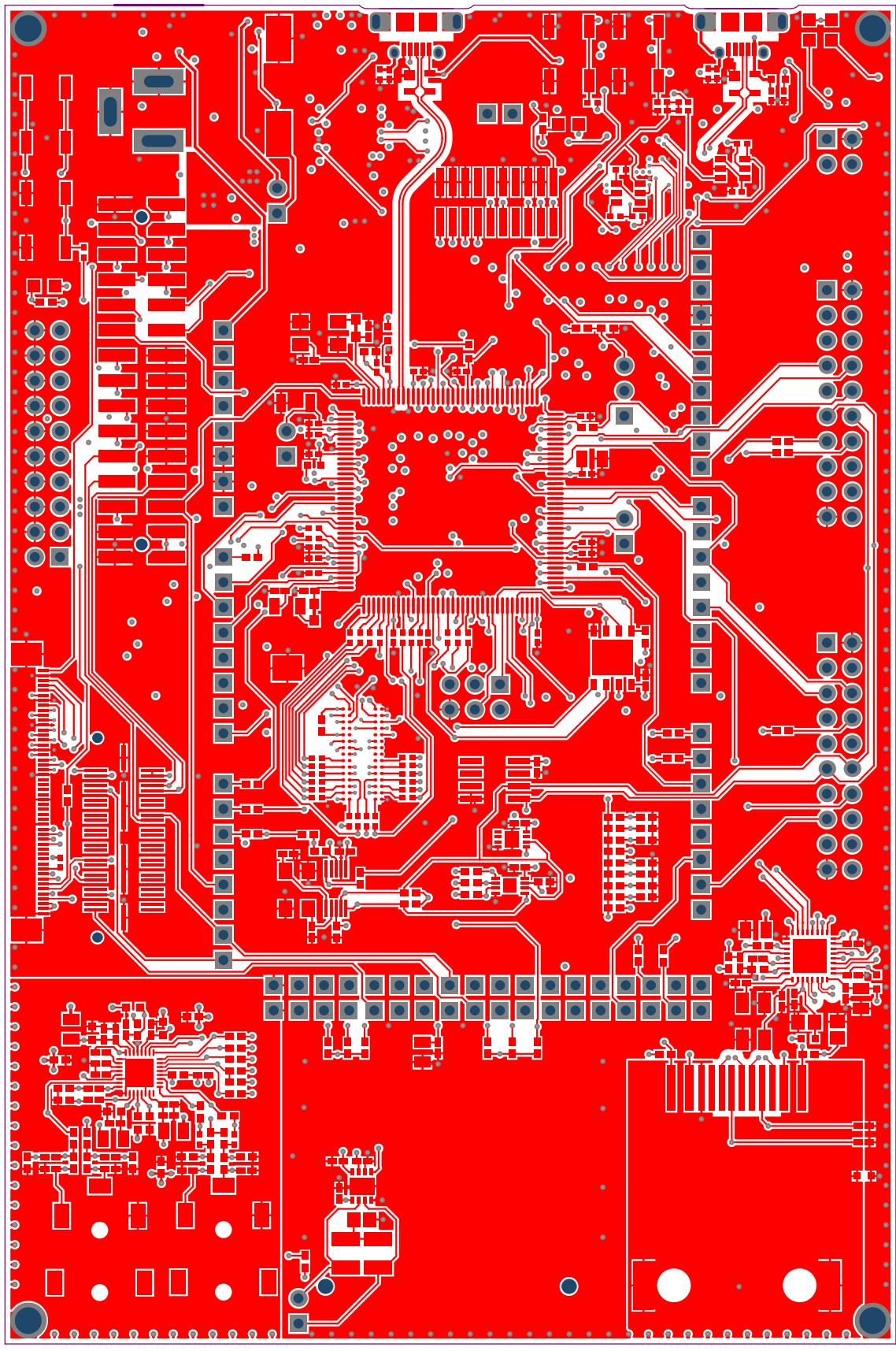
XPLAINED PRO EXTENSION HEADER	
GND	ID
ADC-	ADC+
GPIO1	GPIO0
PWM-	PWM+
SPI_SS_B	IRQ
TWI_SCL	TWI_SDA
UART_TX	UART_RX
SPI_MOSI	SPI_SS_A
SPI_SCK	SPI_MISO
VCC	GND

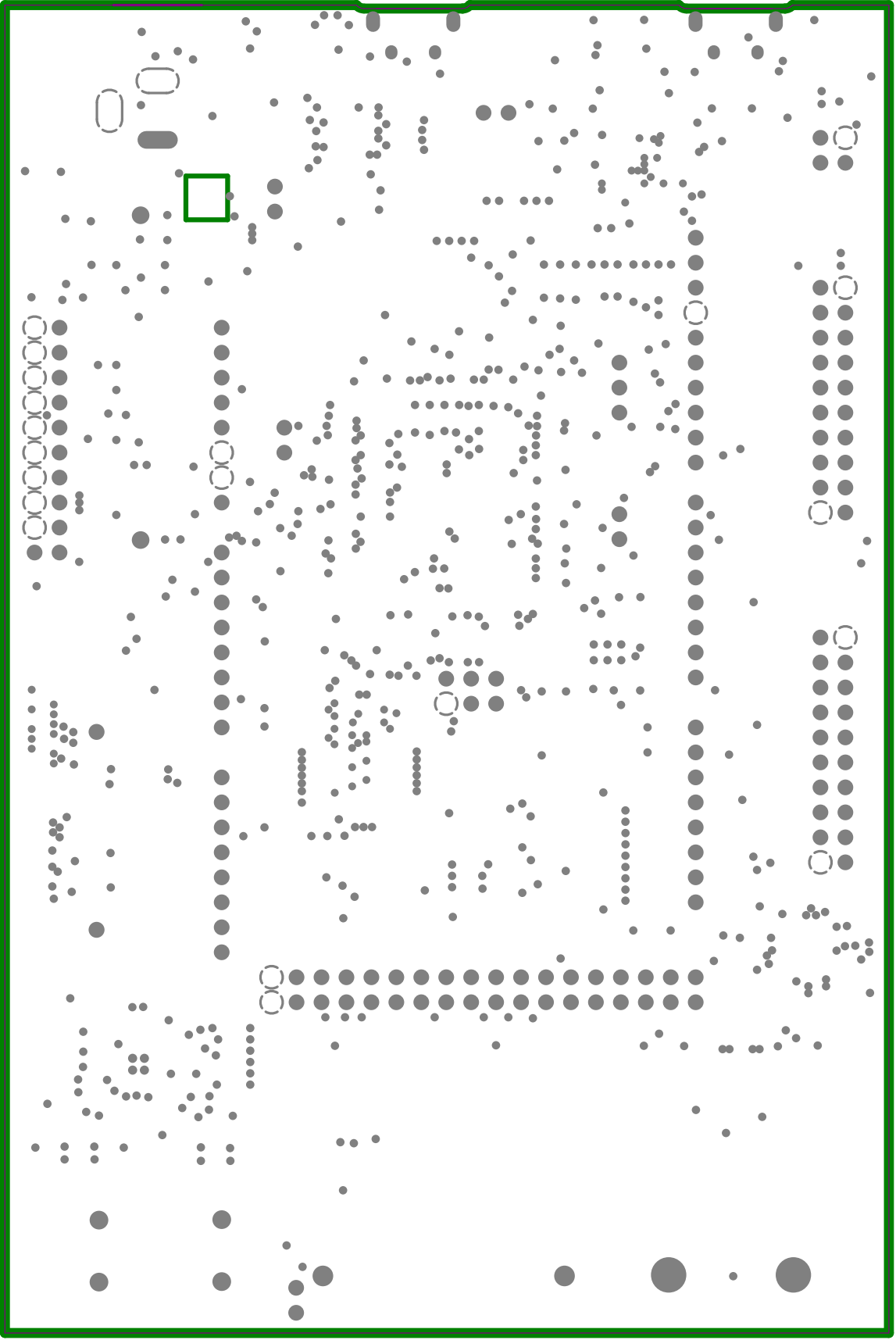
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5V0 PB01 PD18 PB02 PA24 PB04 PC14 GND

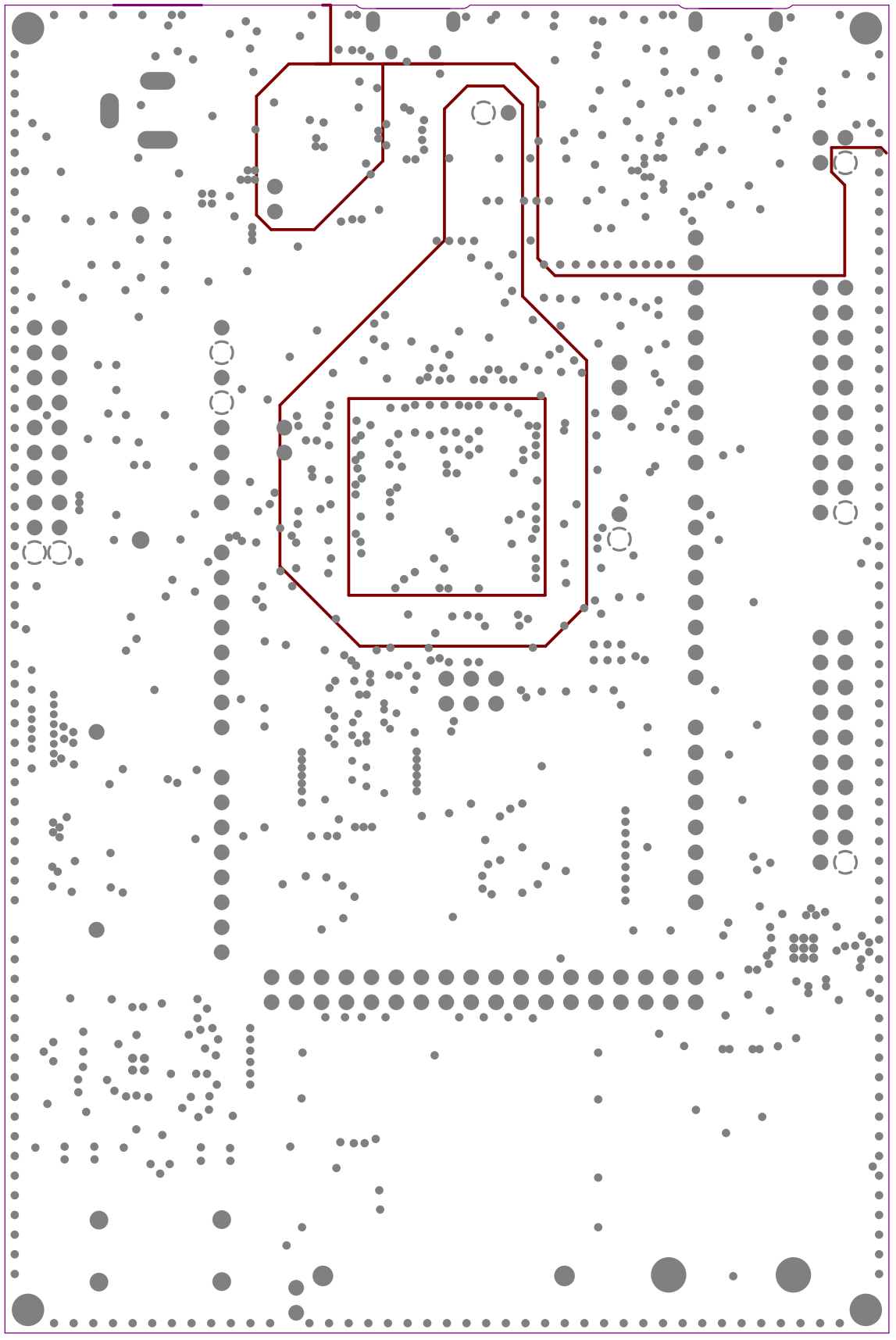
UBAT
3V3
RESET
3V3
5V0
GND
GND
VIN
PD26
PC31
PA19
PD30
PC13
PE00
PE03
PE04
PD24
PA10
PA22
PE05
PB13
PD00
PB03
PB02

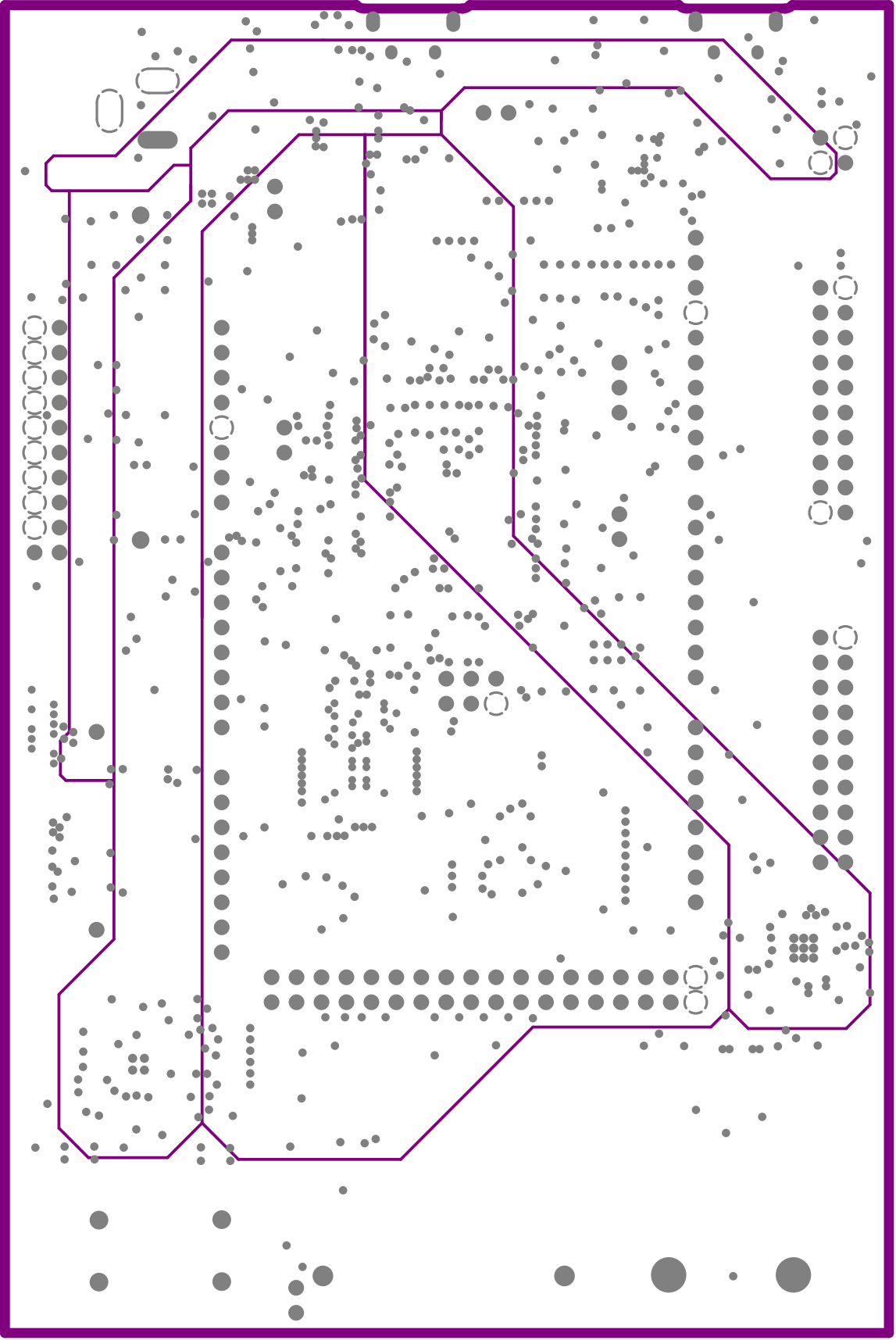
GND
RESET
SWO
SWCLK
SWDIO
GND
3V3
3V3

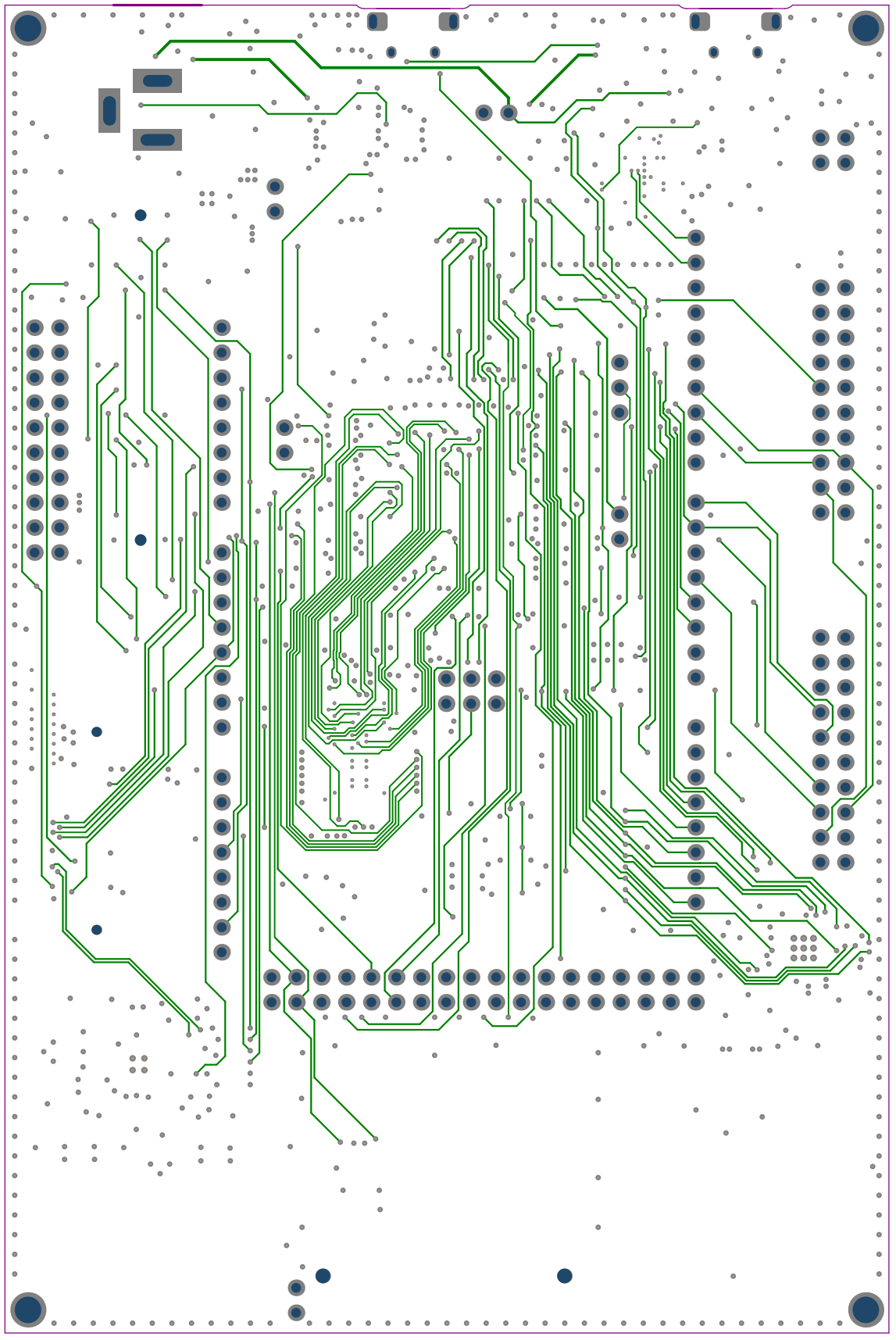


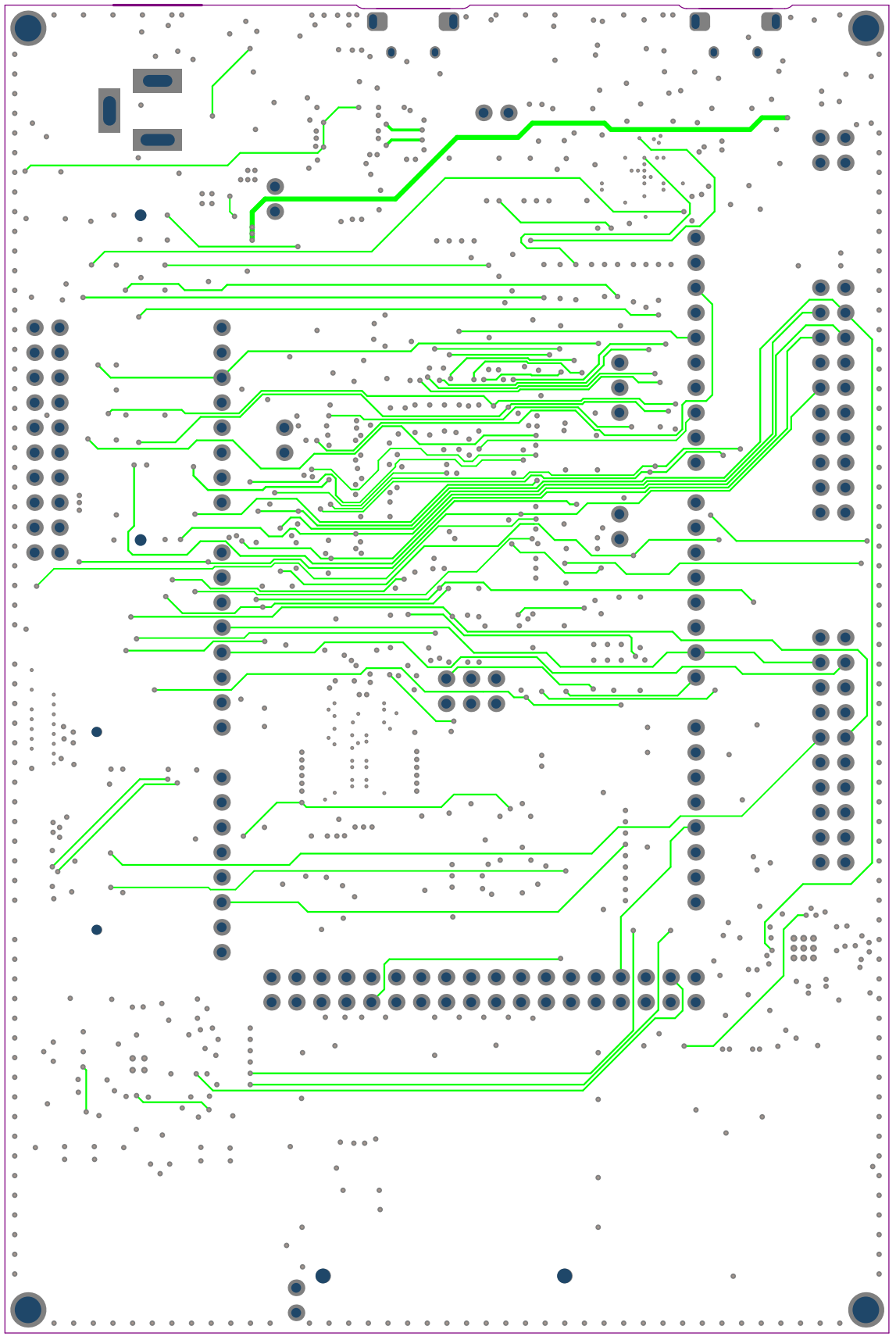


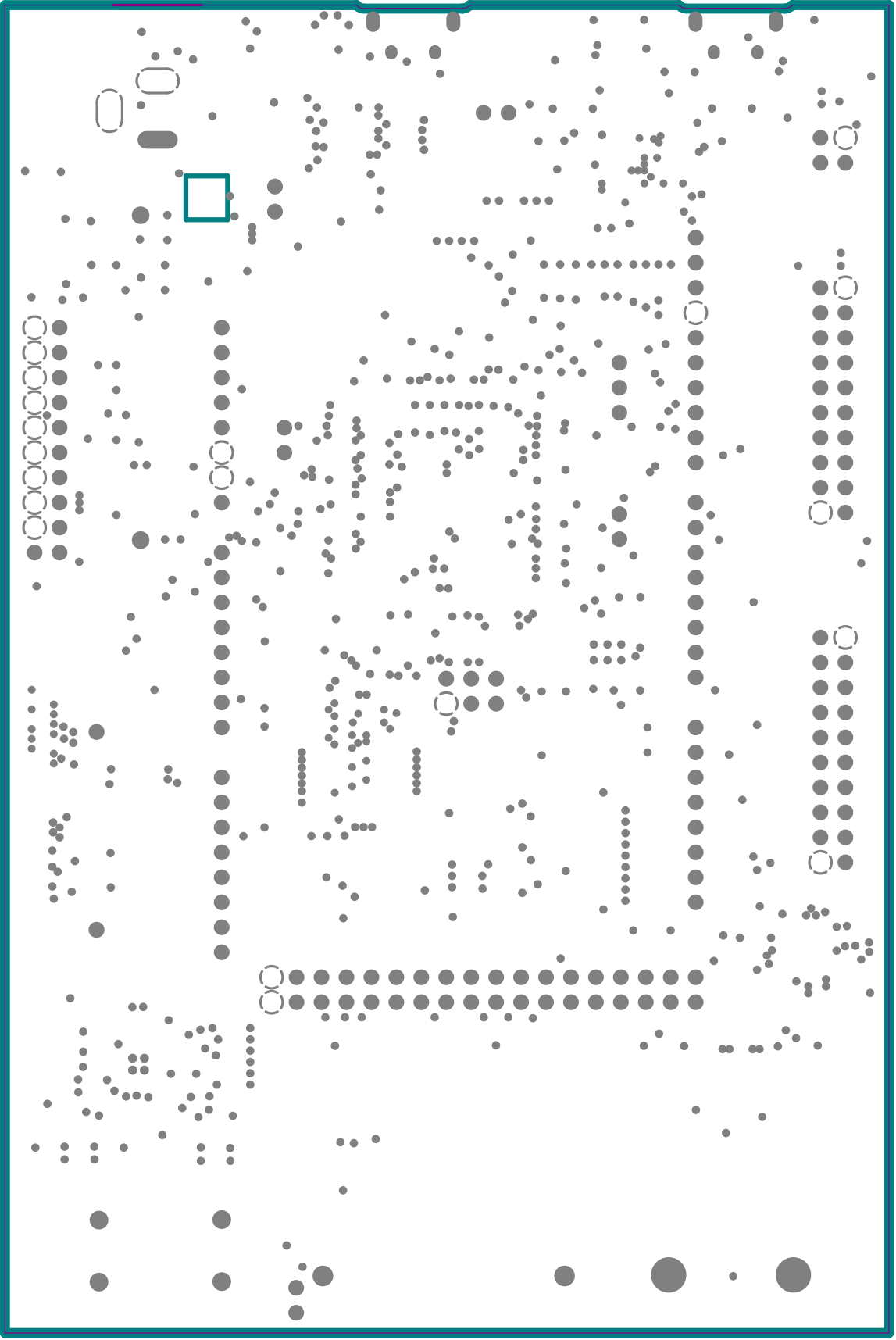


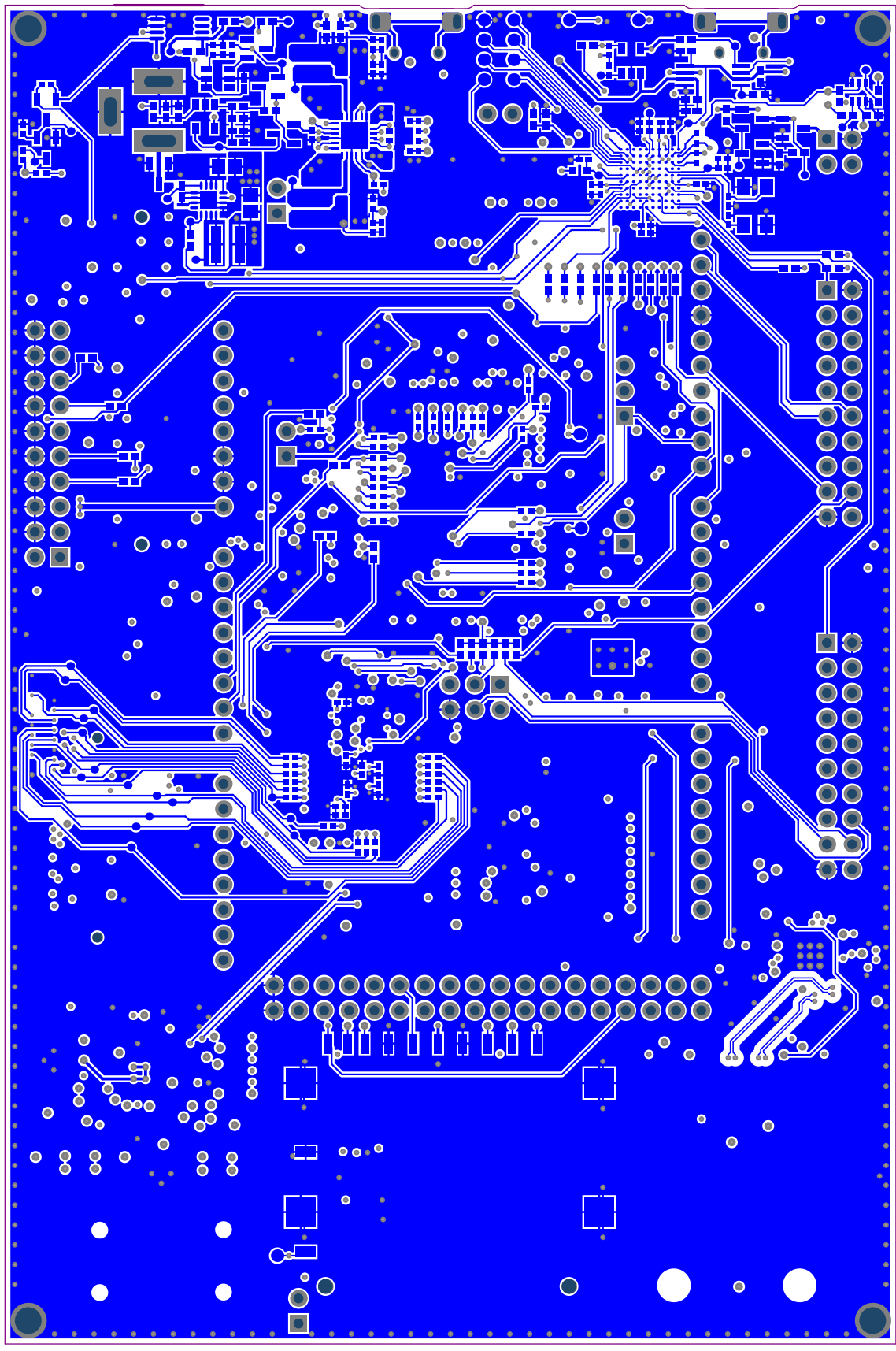


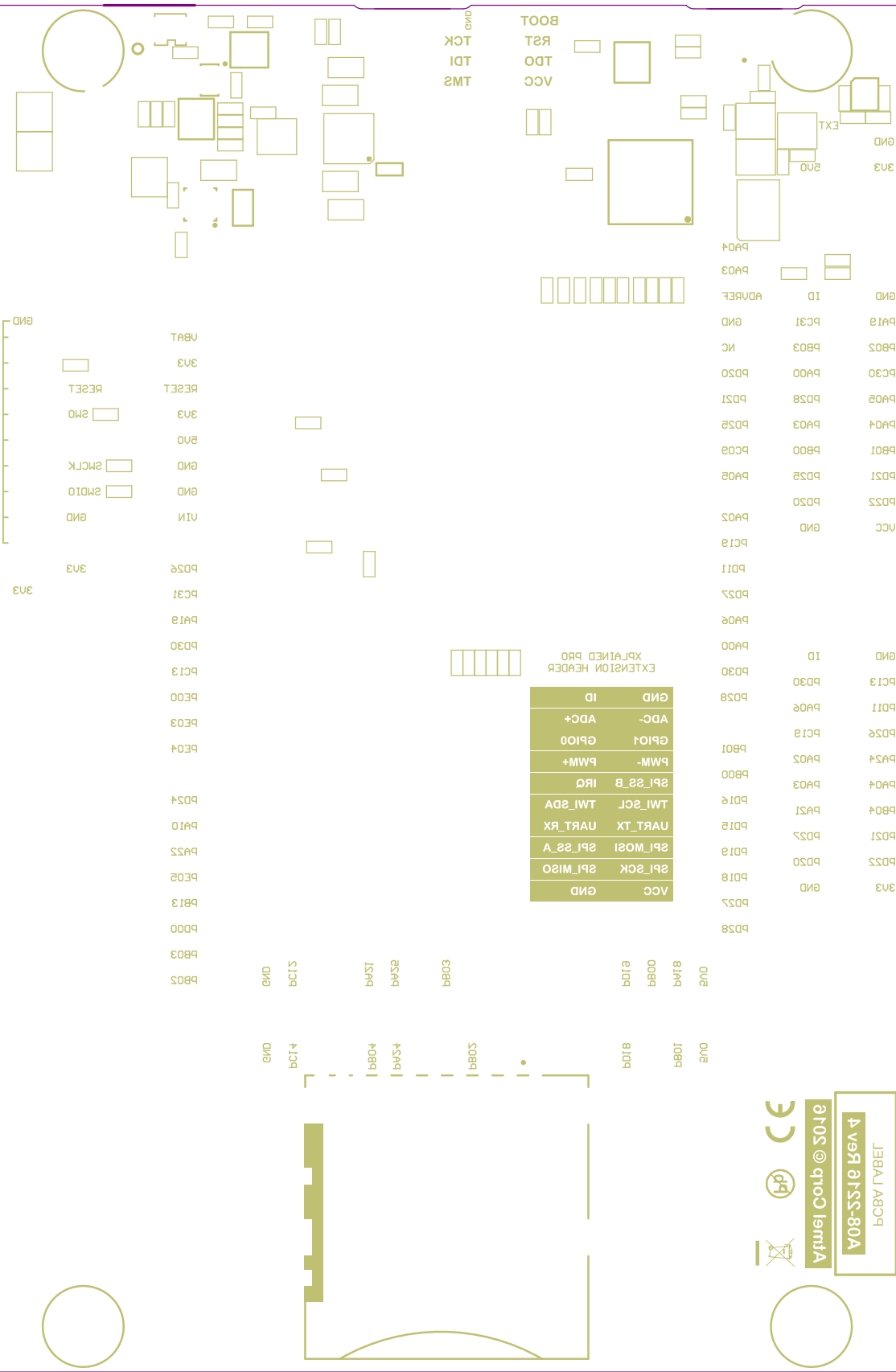




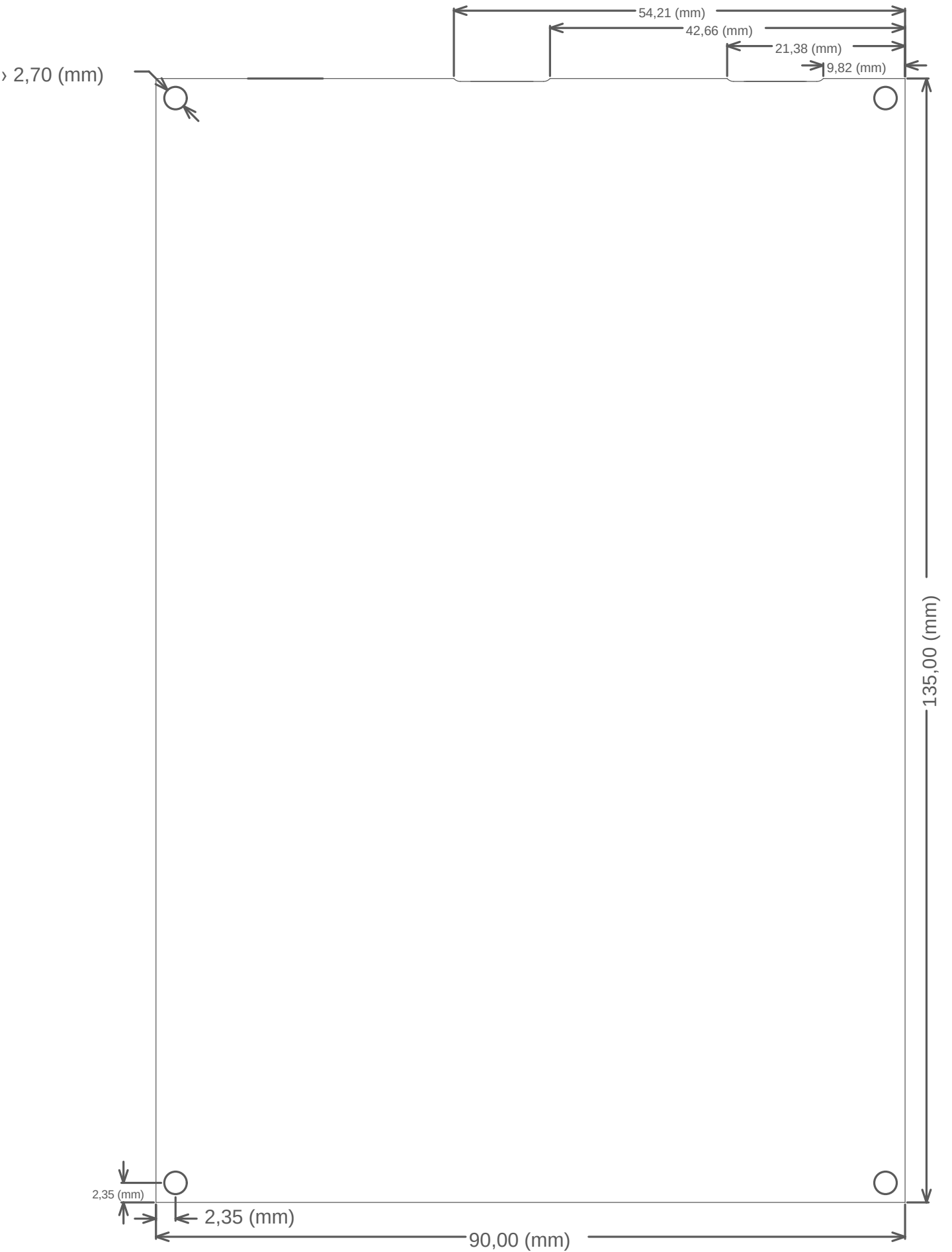




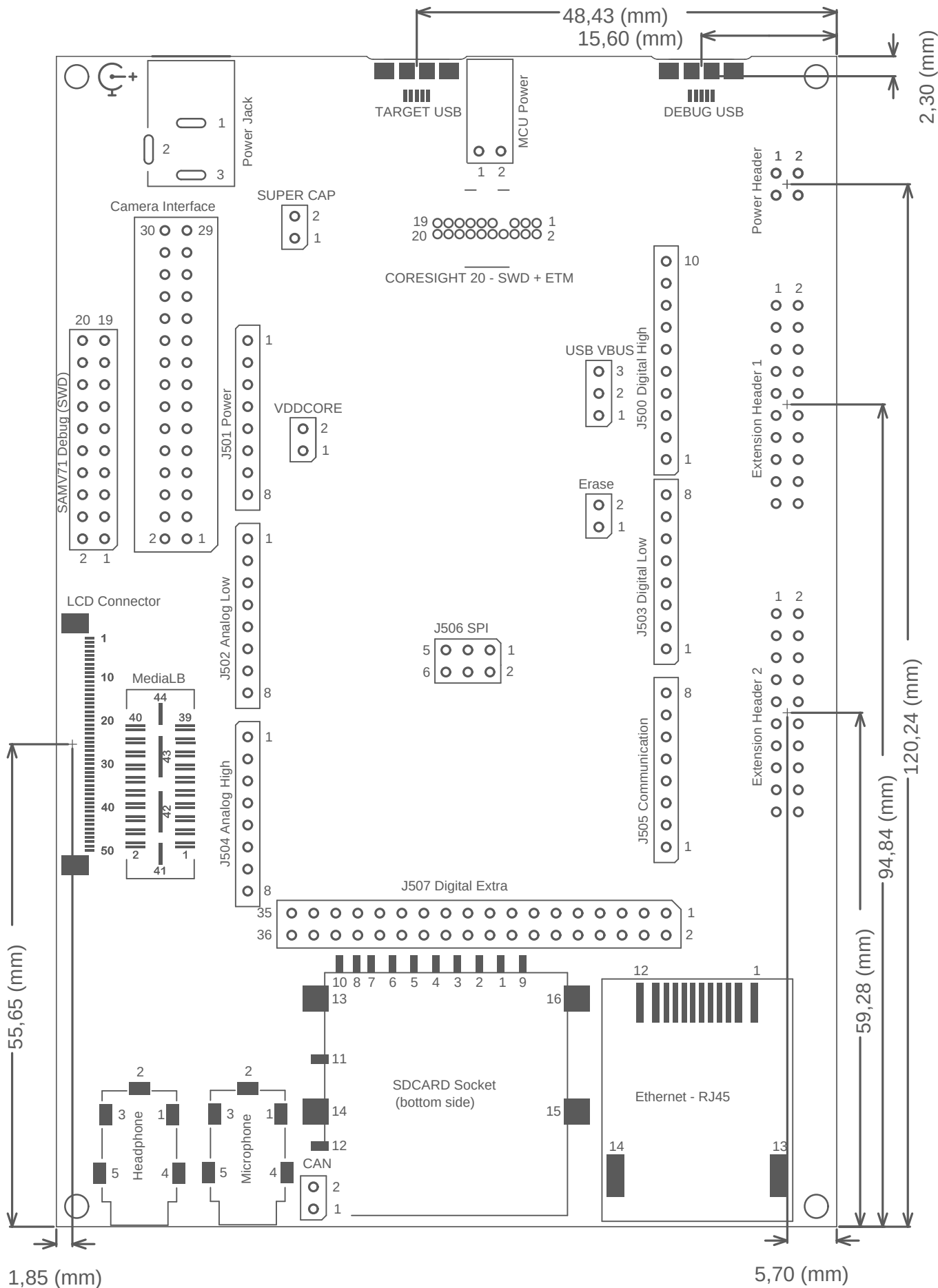




Xplained Ultra Mechanical Dimensions



Xplained Ultra MCU Connector Placement



Bill of Materials Fitted For Variant [Default_assembly] of Project [SAMV71_Xplained_Ultra.PrjPCB] (No PCB Document Select

SAMV71_Xplained_Ultra.PrjPCB

SAMV71_Xplained_Ultra.PrjPCB

Default assembly



Approved	Notes