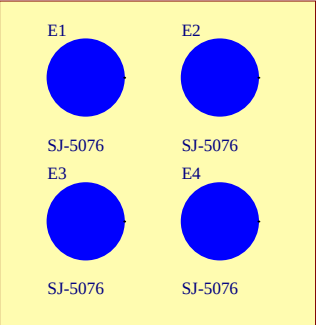
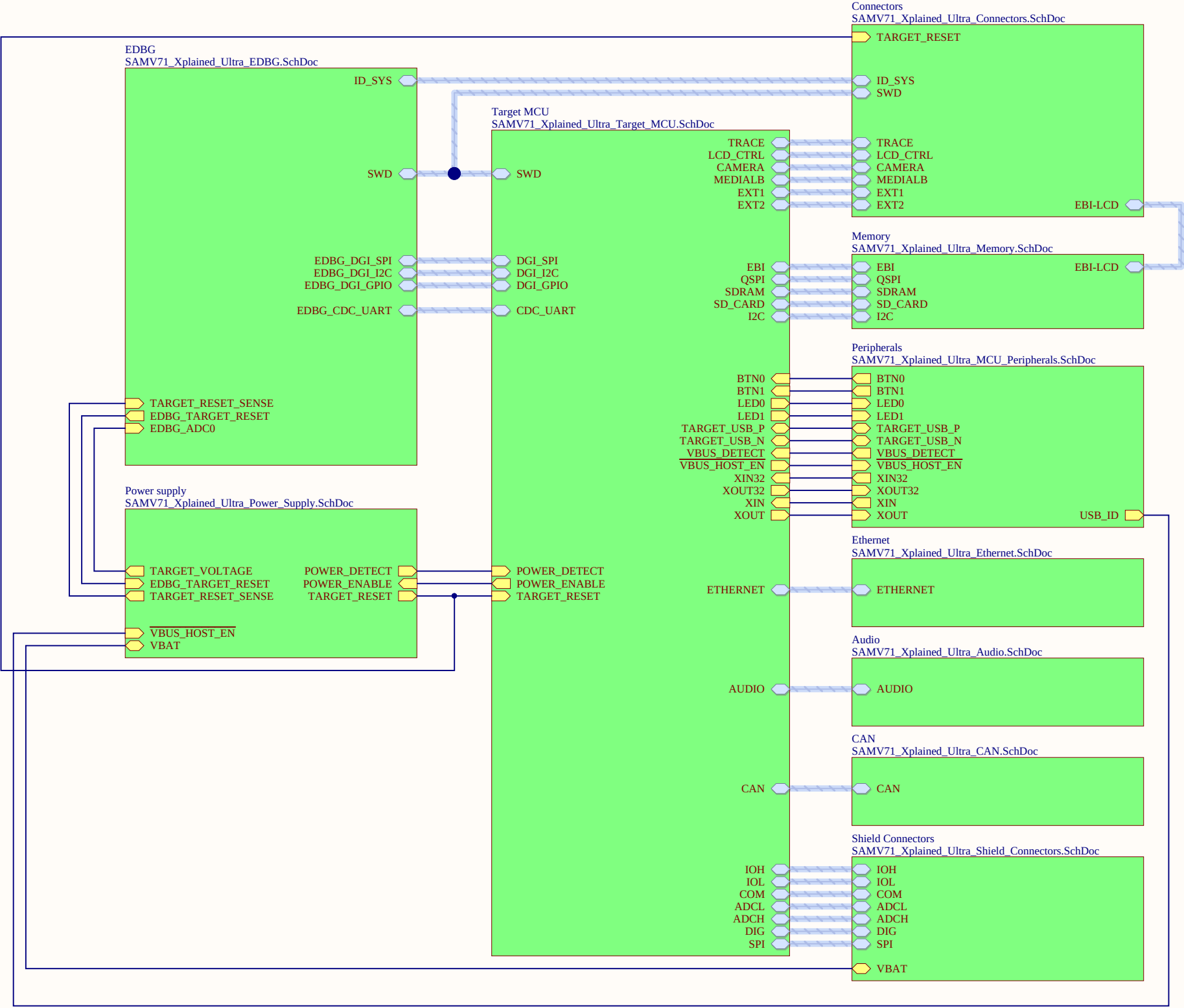


SAM V71 Xplained Ultra



LABEL1

Product number/revision
Serial number

Label PCBA

PCB1: A08-2216 SAM V71 Xplained Ultra PCB Documentation

PCBADOC1: A12-0950

TESTDOC1: A12-0951

FW1: A11-0196

TEST1: A11-0280

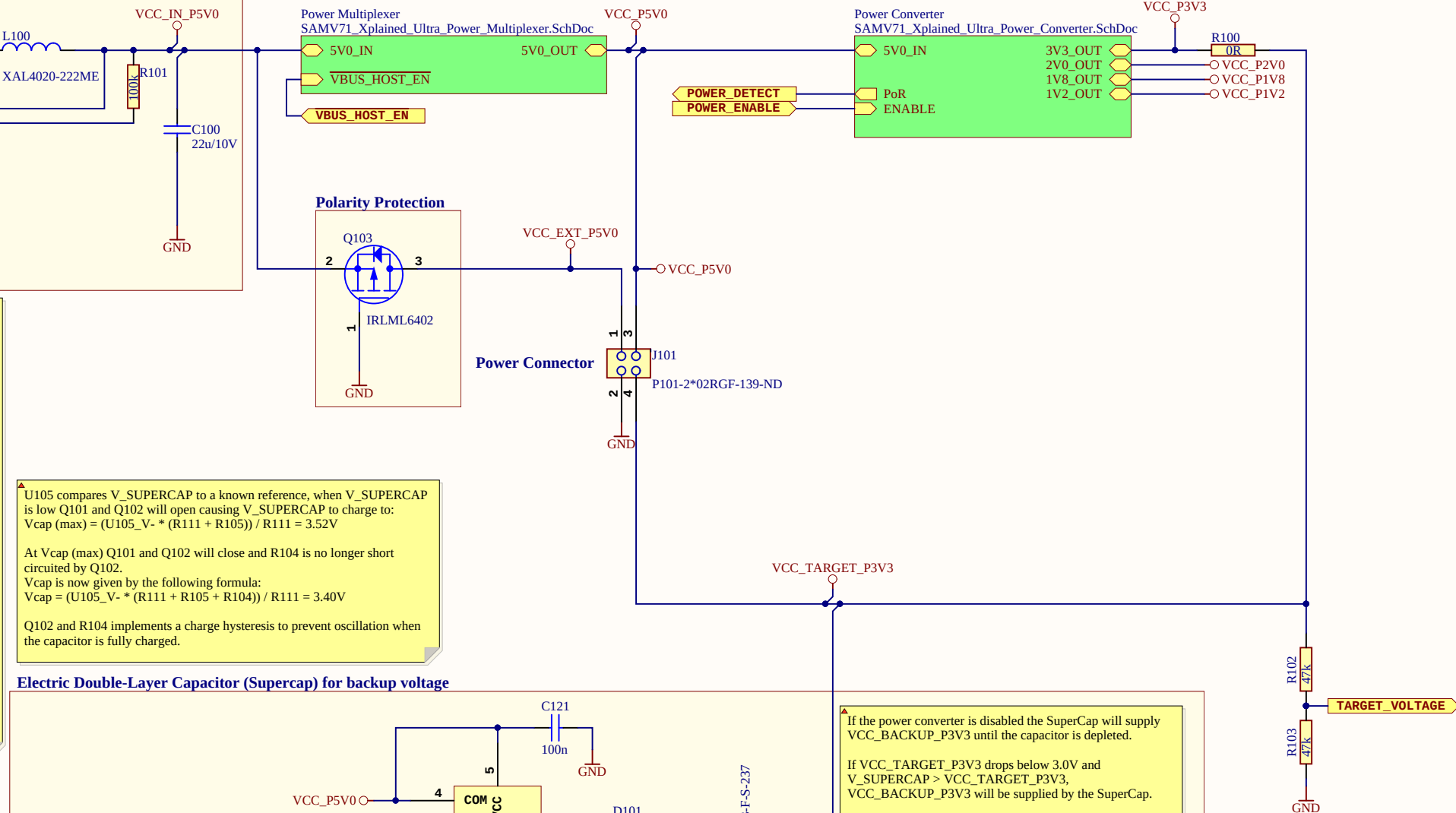
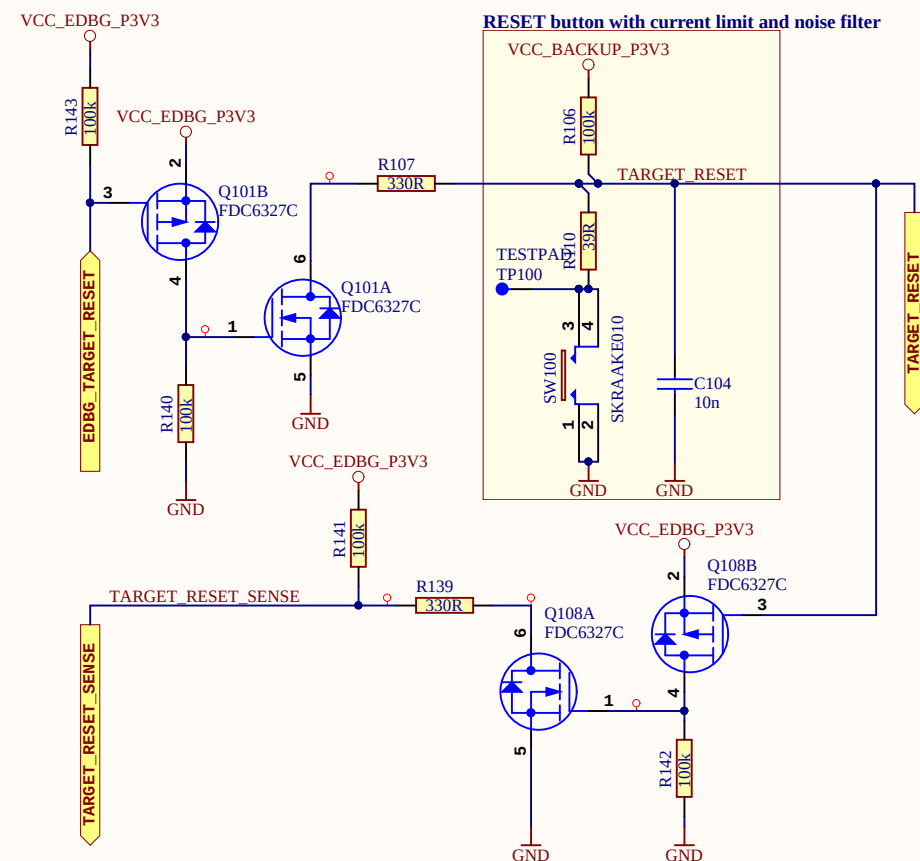
Vin has to be 12V when MediaLB extensions are used.

When Vin = 5V the regulator uses a 100% duty-cycle mode (passthrough).

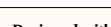
VCC_EXT_P5V0:
This power input can be used to power the whole board and it has a higher priority as the USB power inputs. Connect a power supply if a target MCU with USB host is present and VCC_EXT_P5V0_P17V0 is not used. 4.3V to 5.5V is possible but for USB host operation and in case on-board devices use this voltage it should be 5V +2%.

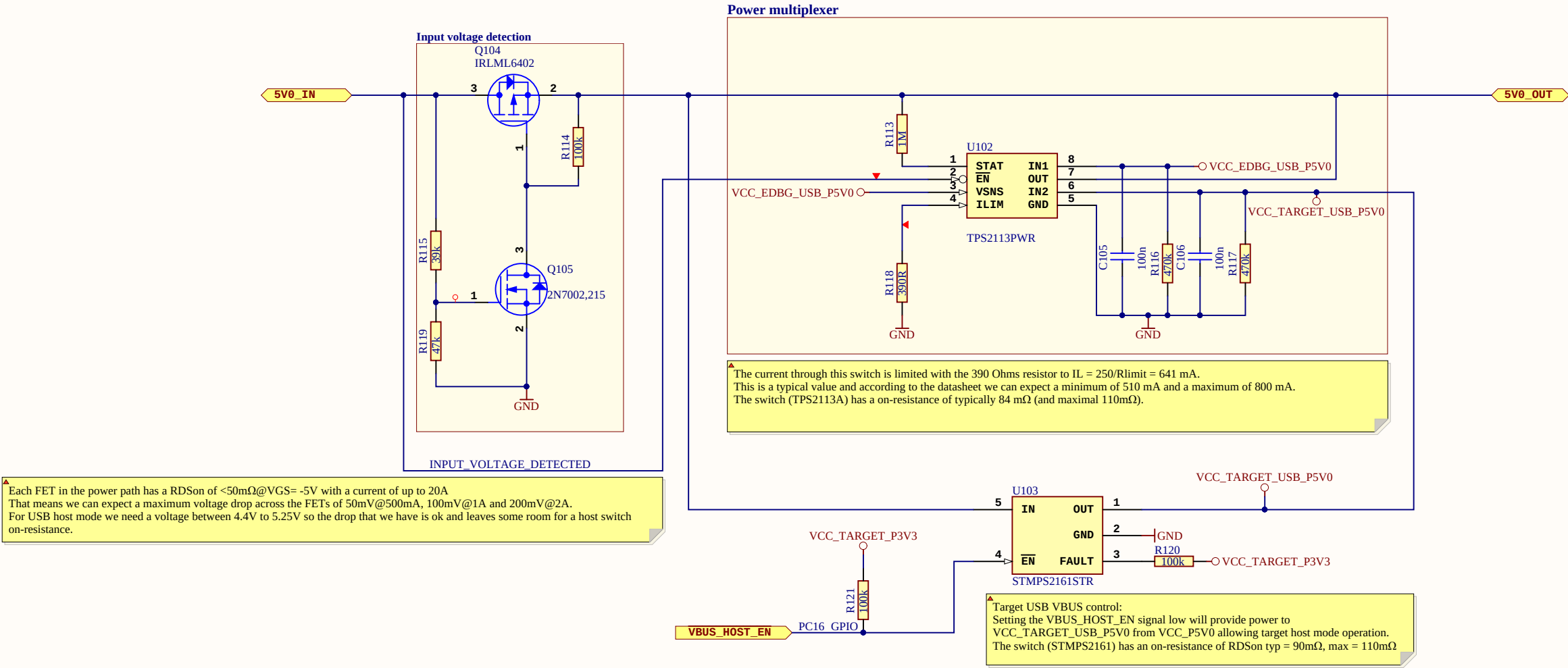
VCC_TARGET_USB_P5V0:
Target MCU USB power input. It is used to power the whole board when no other 5V power supply is present.

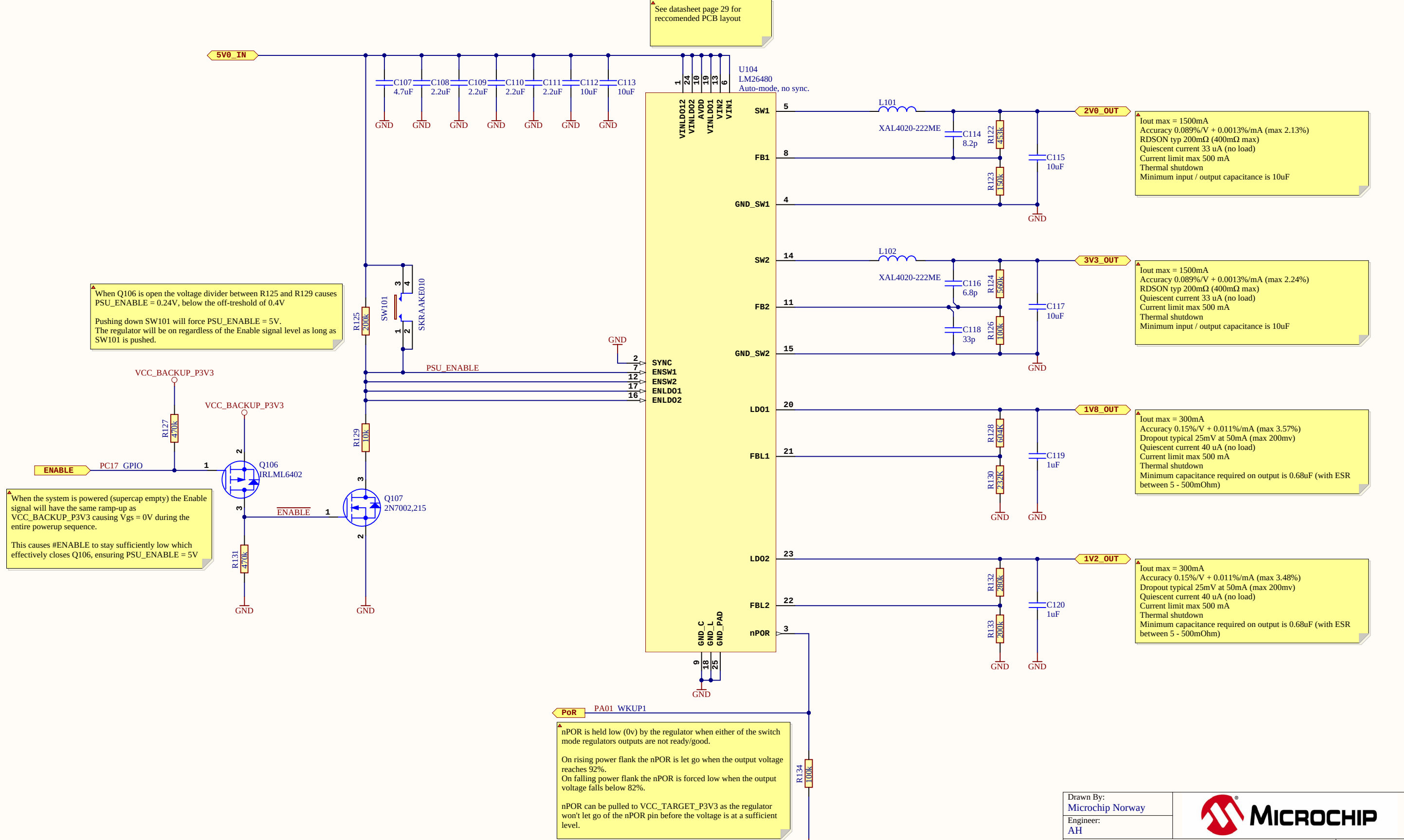
VCC_P3V3: Regulated 3.3V from VCC_P5V0
VCC_P2V0: Regulated 2.0V from VCC_P5V0
VCC_P1V8: Regulated 1.8V from VCC_P5V0
VCC_P1V2: Regulated 1.2V from VCC_P5V0

[illegible]

▲ VMAX is generated as a supply for U105 to make sure it's always referenced to the highest voltage of V_SUPERCAP and VCC_P5V0.

Drawn By: Microchip Norway		 MICROCHIP	
Engineer: AH			
Project Title <i>SAM V71 Xplained Ultra</i>			Designed with  Altium.com
Sheet Title Power supply			
Size A3	PCB Assembly Number: A09-2407 PCB Number: A08-2216	PCBA Revision: 12 PCB Revision: 4	
File: SAMV71_Xplained_Ultra_Power_Supply.SchDoc			Date: 07.09.2017 Page: 2 of 13





See datasheet page 29 for recommended PCB layout

When Q106 is open the voltage divider between R125 and R129 causes PSU_ENABLE = 0.24V, below the off-threshold of 0.4V
Pushing down SW101 will force PSU_ENABLE = 5V.
The regulator will be on regardless of the Enable signal level as long as SW101 is pushed.

When the system is powered (supercap empty) the Enable signal will have the same ramp-up as VCC_BACKUP_P3V3 causing Vgs = 0V during the entire powerup sequence.
This causes #ENABLE to stay sufficiently low which effectively closes Q106, ensuring PSU_ENABLE = 5V

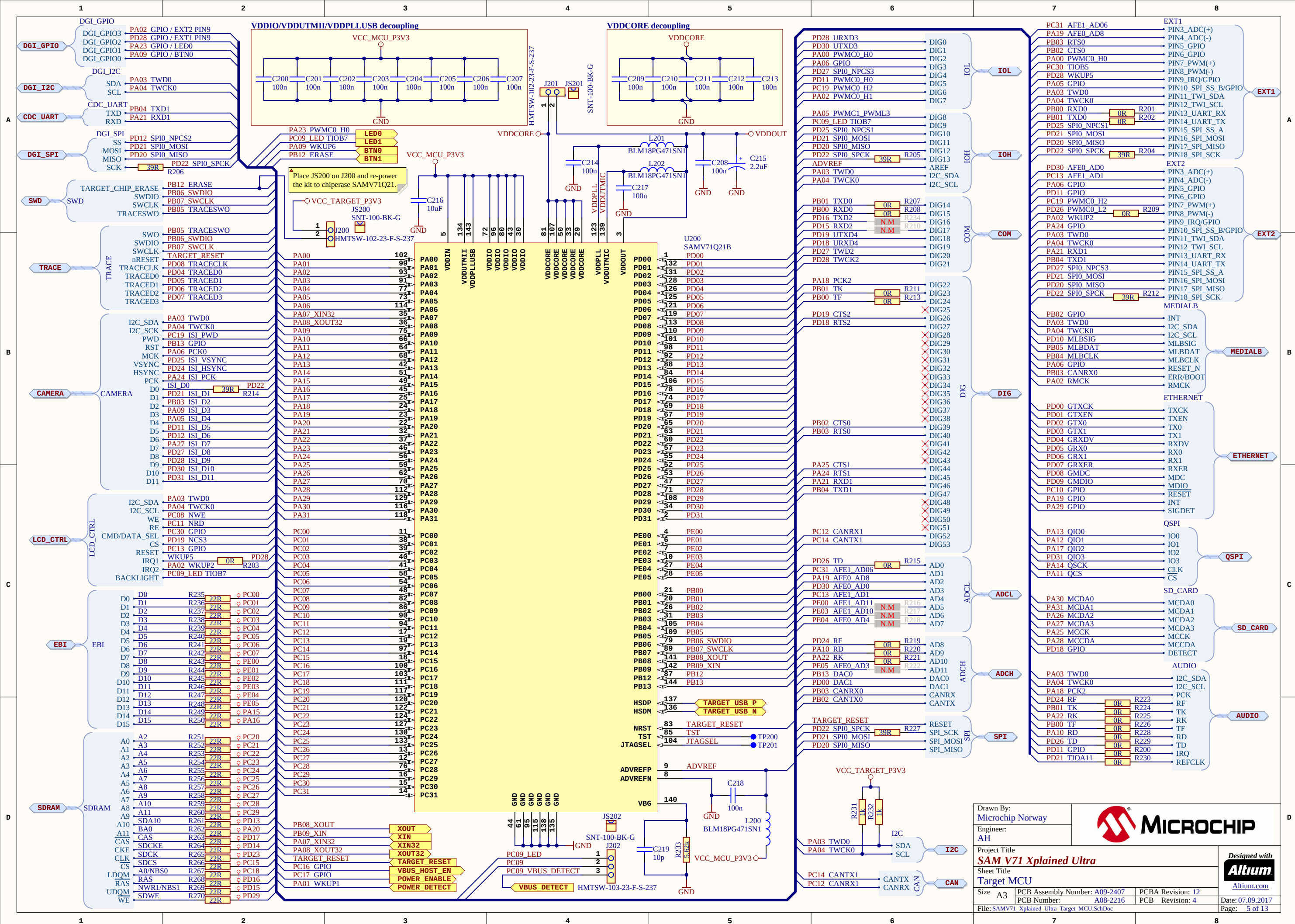
Iout max = 1500mA
Accuracy 0.089%/V + 0.0013%/mA (max 2.13%)
RDSOn typ 200mΩ (400mΩ max)
Quiescent current 33 uA (no load)
Current limit max 500 mA
Thermal shutdown
Minimum input / output capacitance is 10uF

Iout max = 1500mA
Accuracy 0.089%/V + 0.0013%/mA (max 2.24%)
RDSOn typ 200mΩ (400mΩ max)
Quiescent current 33 uA (no load)
Current limit max 500 mA
Thermal shutdown
Minimum input / output capacitance is 10uF

Iout max = 300mA
Accuracy 0.15%/V + 0.011%/mA (max 3.57%)
Dropout typical 25mV at 50mA (max 200mv)
Quiescent current 40 uA (no load)
Current limit max 500 mA
Thermal shutdown
Minimum capacitance required on output is 0.68uF (with ESR between 5 - 500mOhm)

Iout max = 300mA
Accuracy 0.15%/V + 0.011%/mA (max 3.48%)
Dropout typical 25mV at 50mA (max 200mv)
Quiescent current 40 uA (no load)
Current limit max 500 mA
Thermal shutdown
Minimum capacitance required on output is 0.68uF (with ESR between 5 - 500mOhm)

nPOR is held low (0v) by the regulator when either of the switch mode regulators outputs are not ready/good.
On rising power flank the nPOR is let go when the output voltage reaches 92%.
On falling power flank the nPOR is forced low when the output voltage falls below 82%.
nPOR can be pulled to VCC_TARGET_P3V3 as the regulator won't let go of the nPOR pin before the voltage is at a sufficient level.



32.768kHz +/-20PPM 7pF SMD
XC300

PA08_XOUT32

XOUT32

J300

C300
4.7p

GND

PA07_XIN32

XIN32

C301
4.7p

GND

PA09 WKUP6
PB12 ERASE

BTN0
BTN1

TP300

R300 39R

SW300

SKRAAKE010

R301 39R

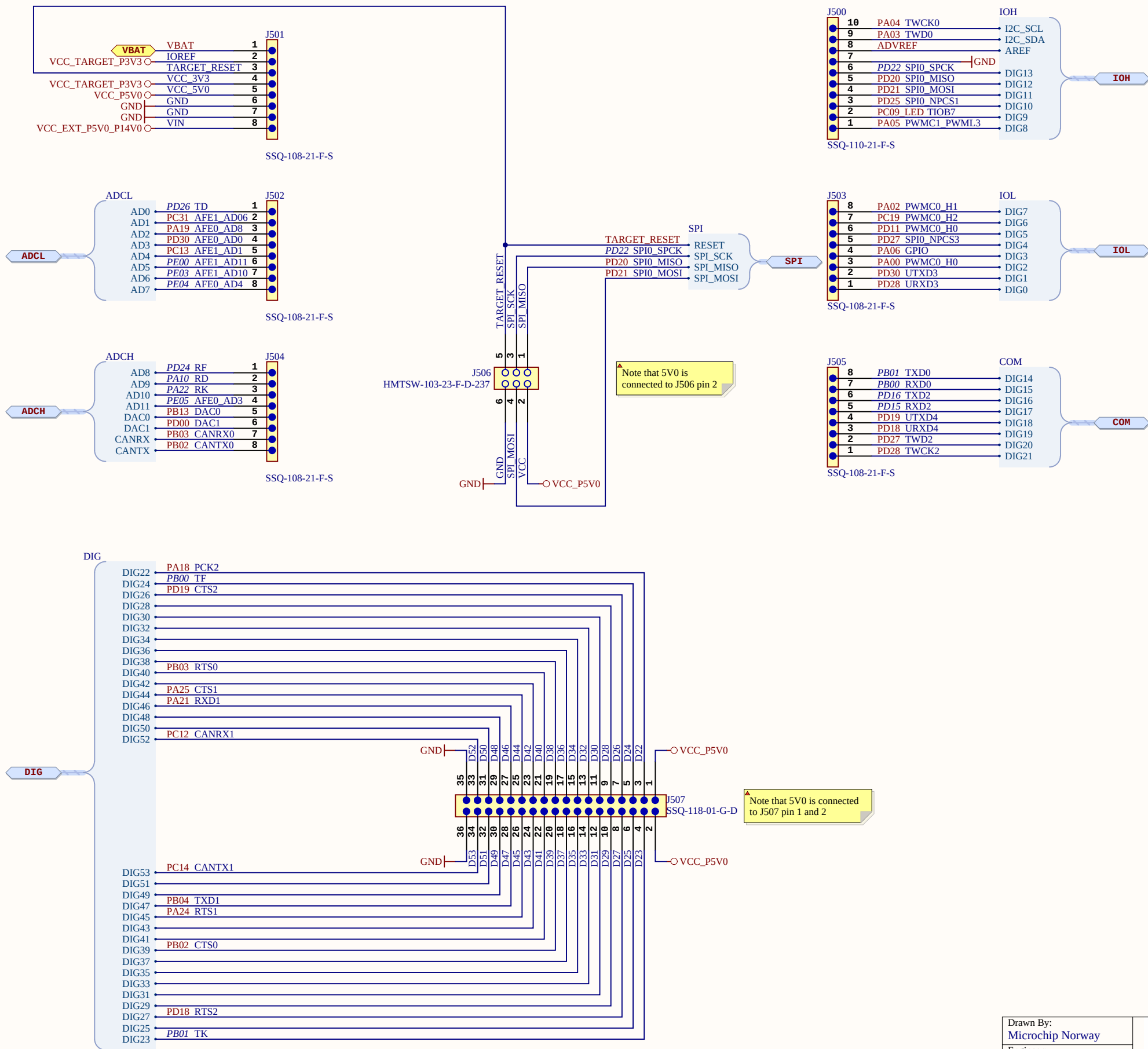
SW301

SKRAAKE010

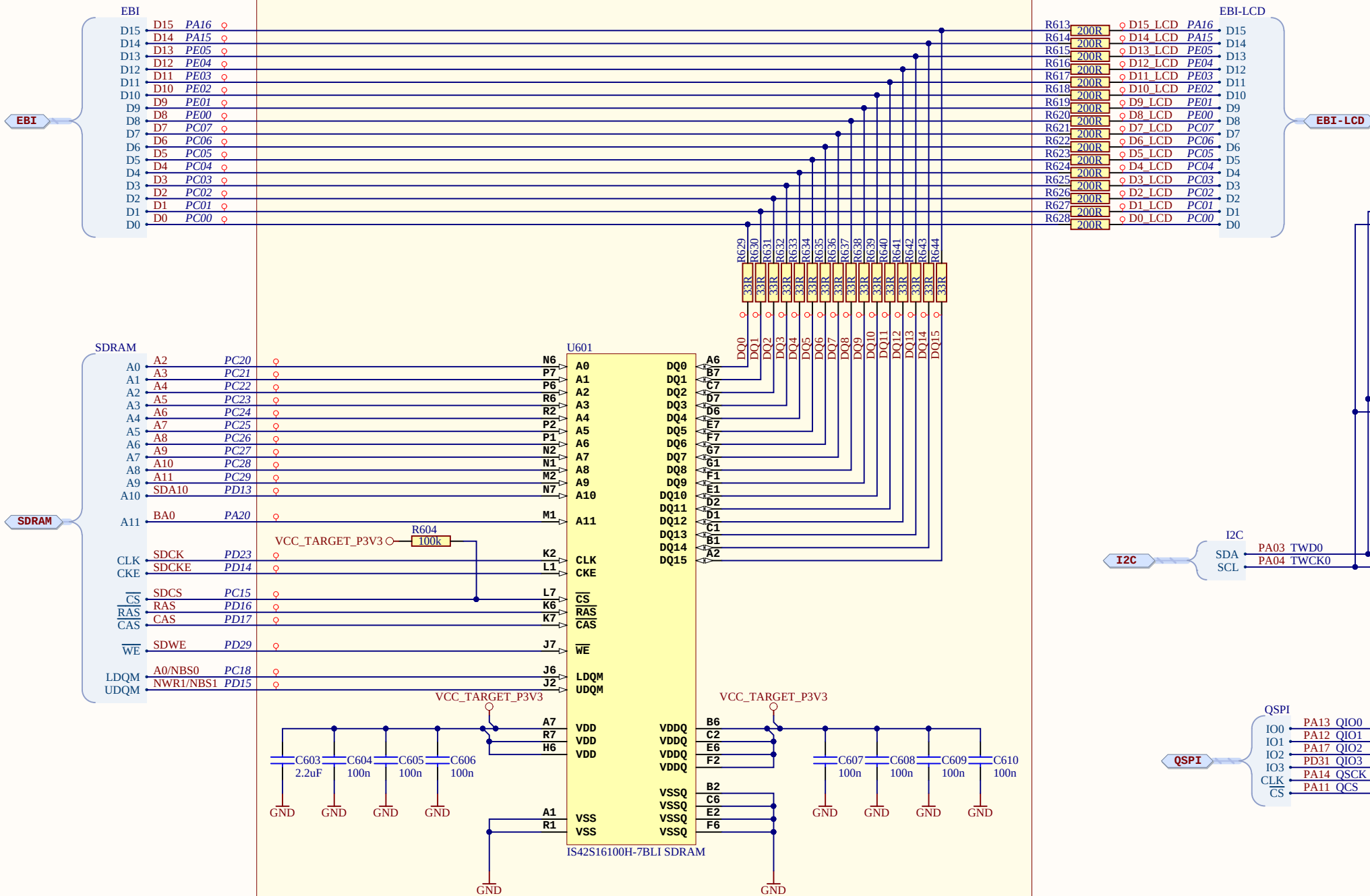
GND

[illegible]

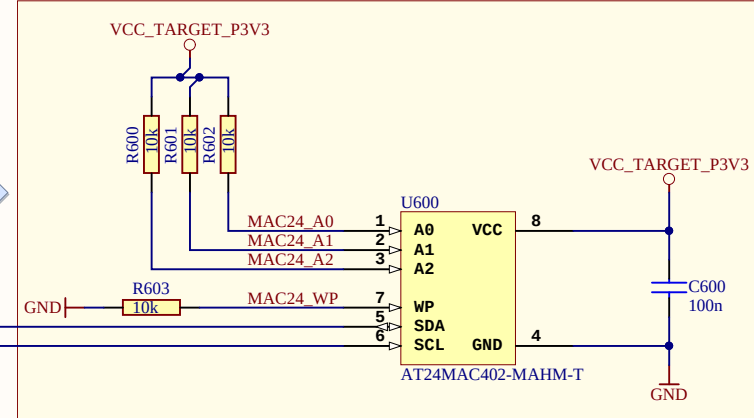
Designed with
Altium
Altium.com



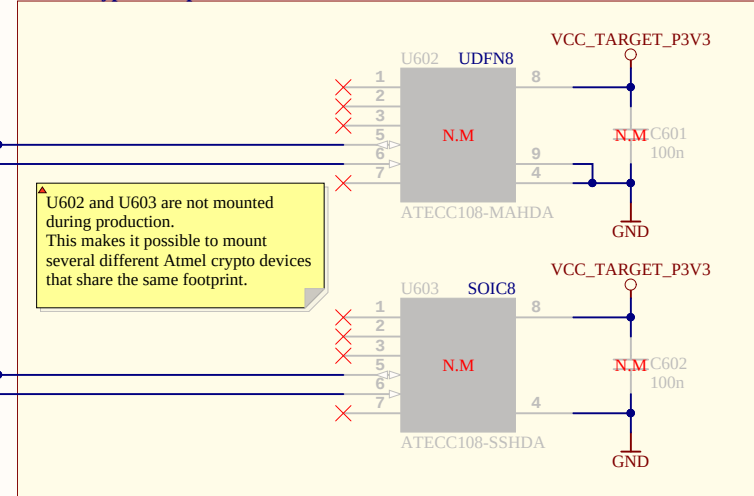
SDRAM (16MBit)



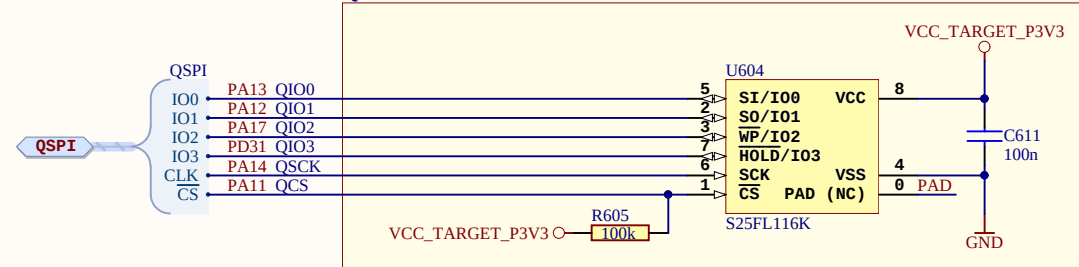
Serial EEPROM with EIA-48 MAC address



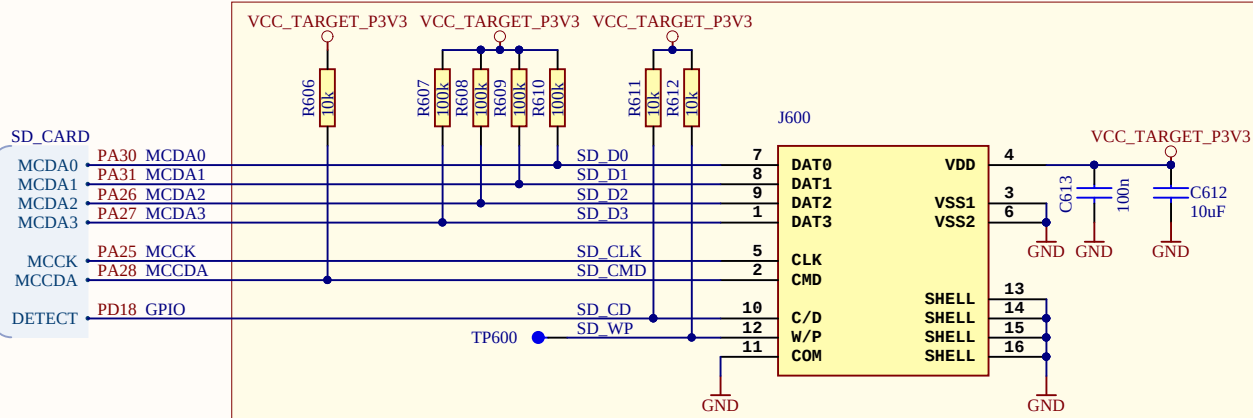
Atmel Crypto Footprints



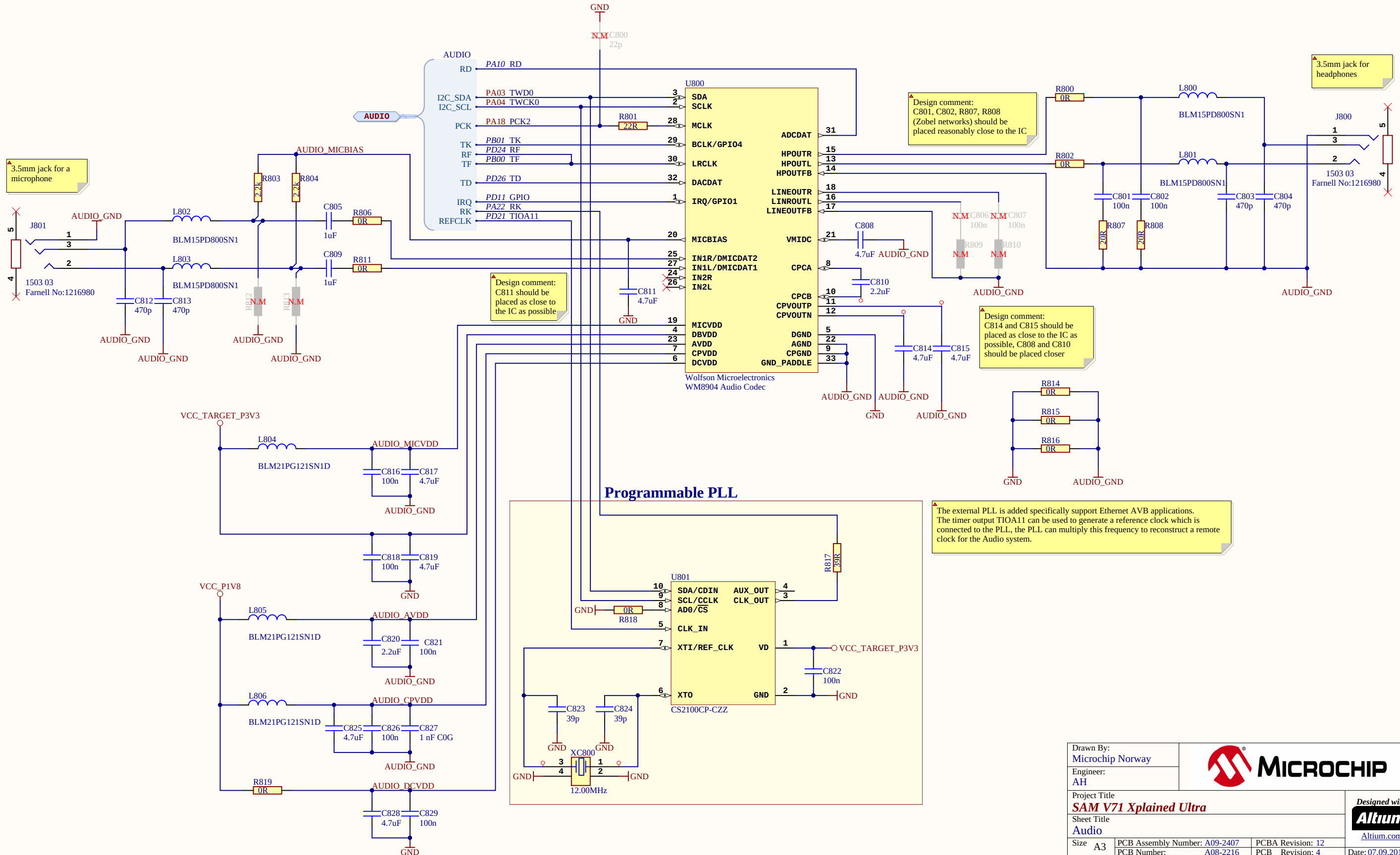
QSPI FLASH

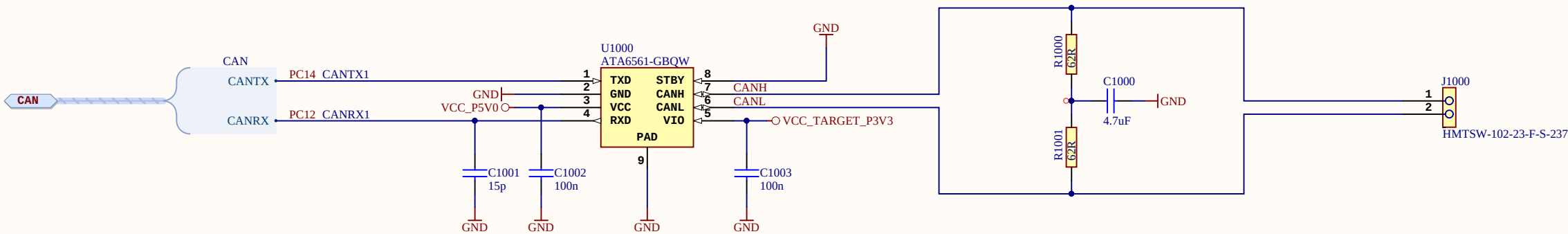


SD-CARD



C/D is connected to COM when a card is placed into the socket.
W/P is connected to COM when the write protect slider is in protect position.





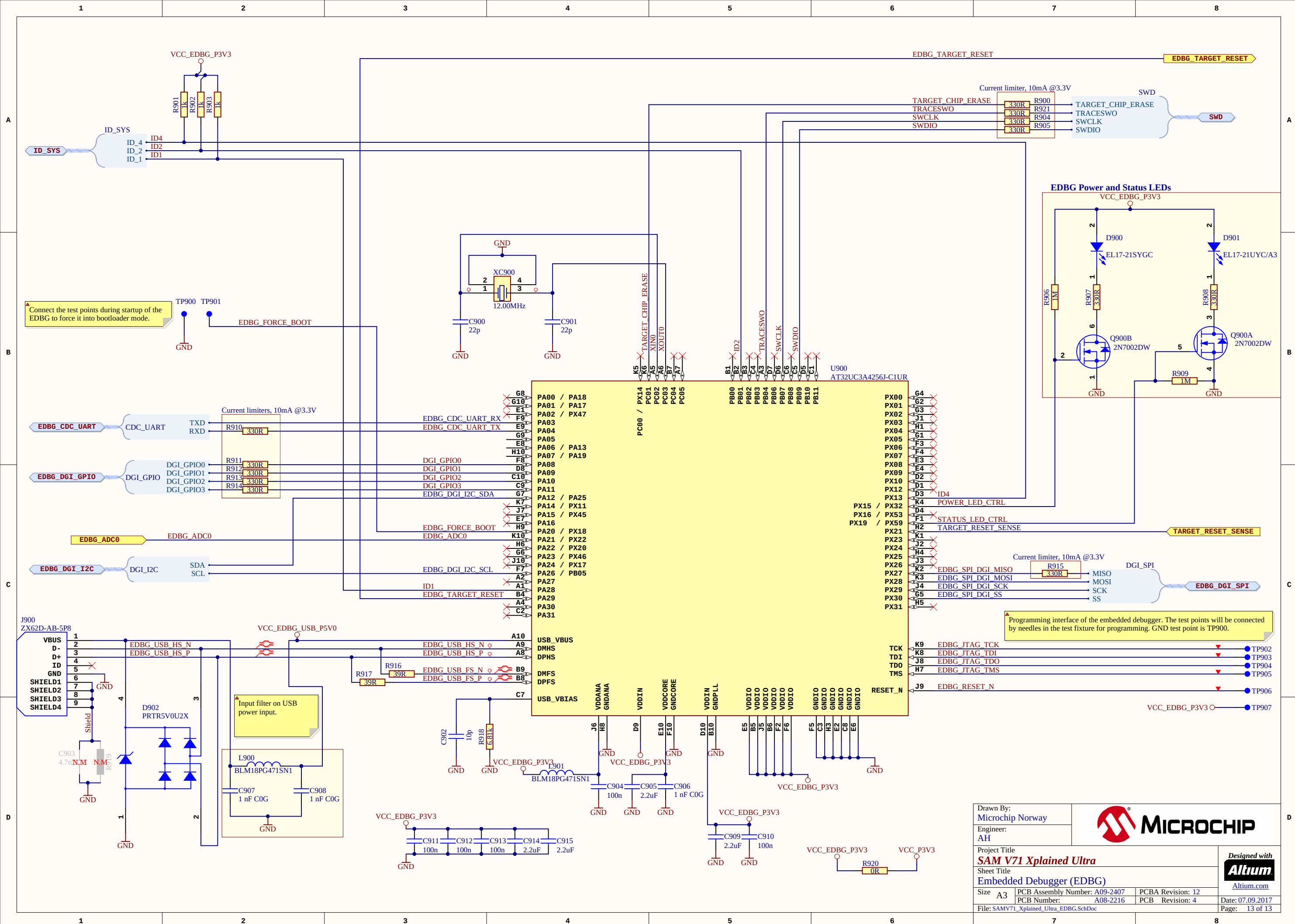
Drawn By:
Microchip Norway
Engineer:
AH

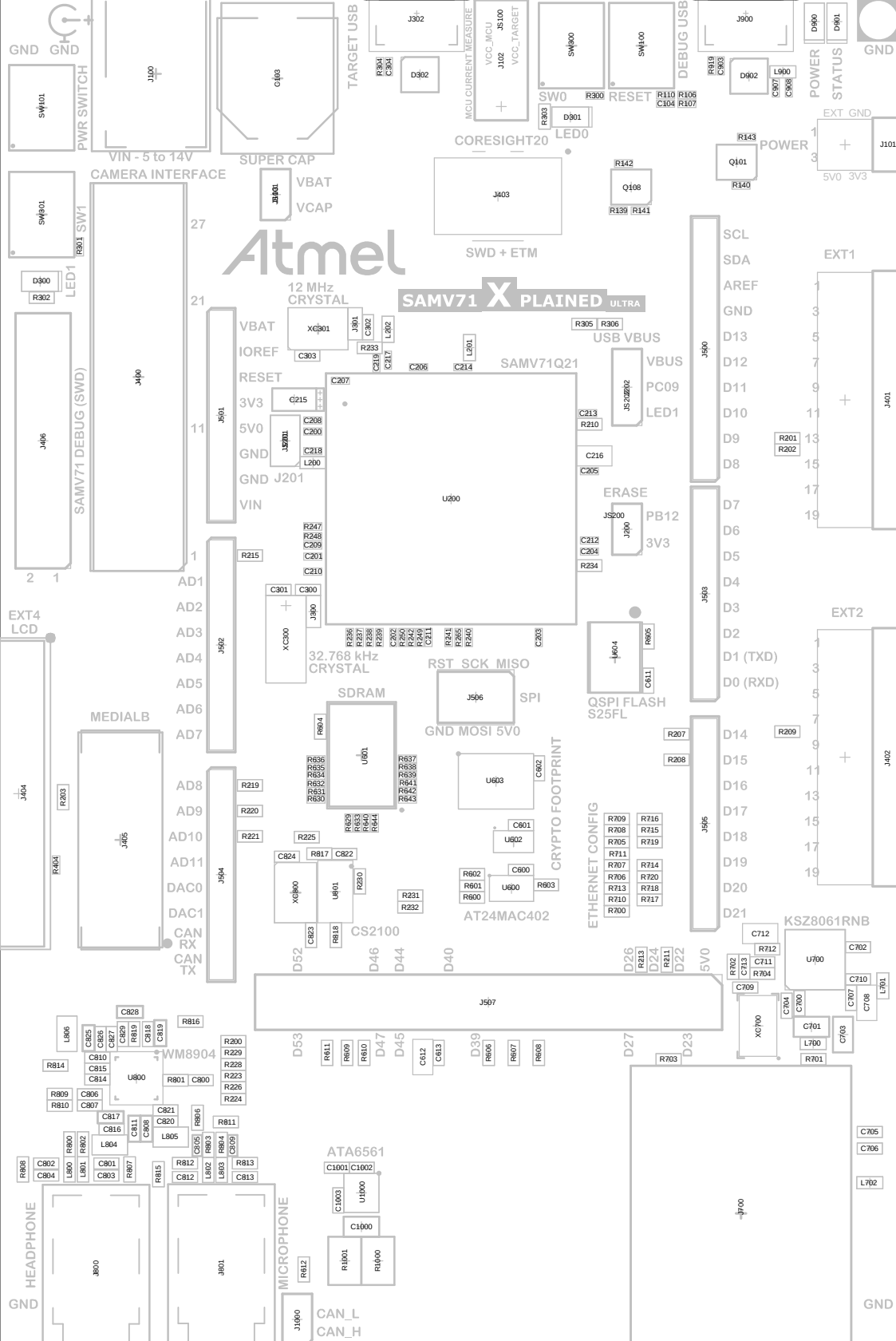


Project Title
SAM V71 Xplained Ultra
Sheet Title
CAN

Designed with
Altium
Altium.com

Size A3	PCB Assembly Number: A09-2407	PCBA Revision: 12	Date: 07.09.2017
	PCB Number: A08-2216	PCB Revision: 4	Page: 12 of 13
File: SAMV71_Xplained_Ultra_CAN.SchDoc			





Atmel

SAMV71 X PLAINED ULTRA

12 MHz CRYSTAL

32.768 kHz CRYSTAL

SDRAM

GND MOSI 5V0

SPI

CRYPTO FOOTPRINT

ERASE

QSPI FLASH S25FL

AT24MAC402

CS2100

WM8904

ATA6561

KSZ8061RNB

HEADPHONE

MICRAPHONE

CAMERA INTERFACE

TARGET USB

DEBUG USB

CORESIGHT20

POWER STATUS

EXT1

EXT2

EXT3

EXT4

EXT5

EXT6

EXT7

EXT8

EXT9

EXT10

EXT11

EXT12

EXT13

EXT14

EXT15

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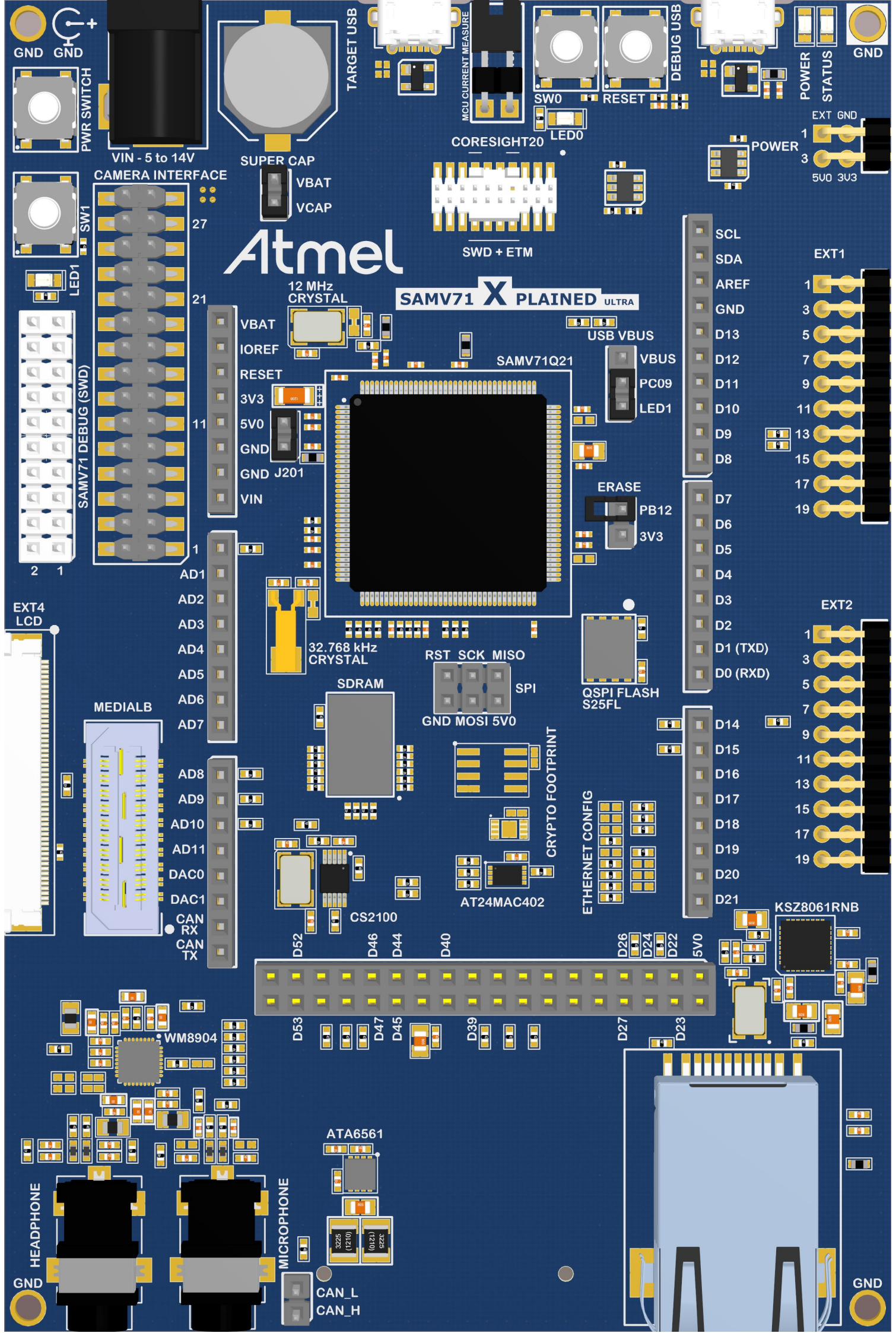
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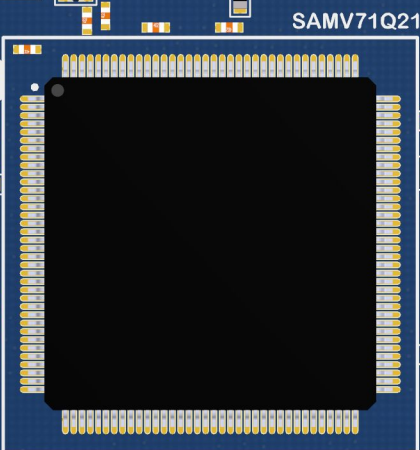
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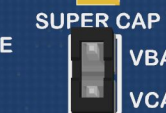
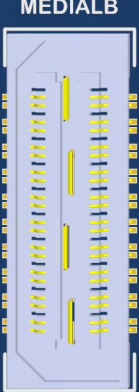
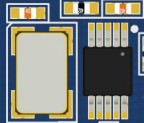
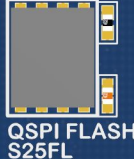


Atmel

SAMV71 X PLAINED ULTRA

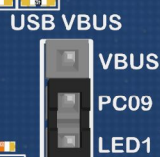


32.768 kHz CRYSTAL



VBAT
VCAP

VBAT
IOREF
RESET
3V3
5V0
GND
GND J201
VIN



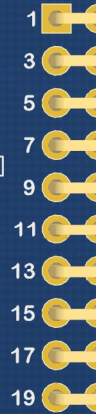
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
DAC0
DAC1
CAN RX
CAN TX



EXT1



EXT2



CAN_L
CAN_H

MICROPHONE

HEADPHONE



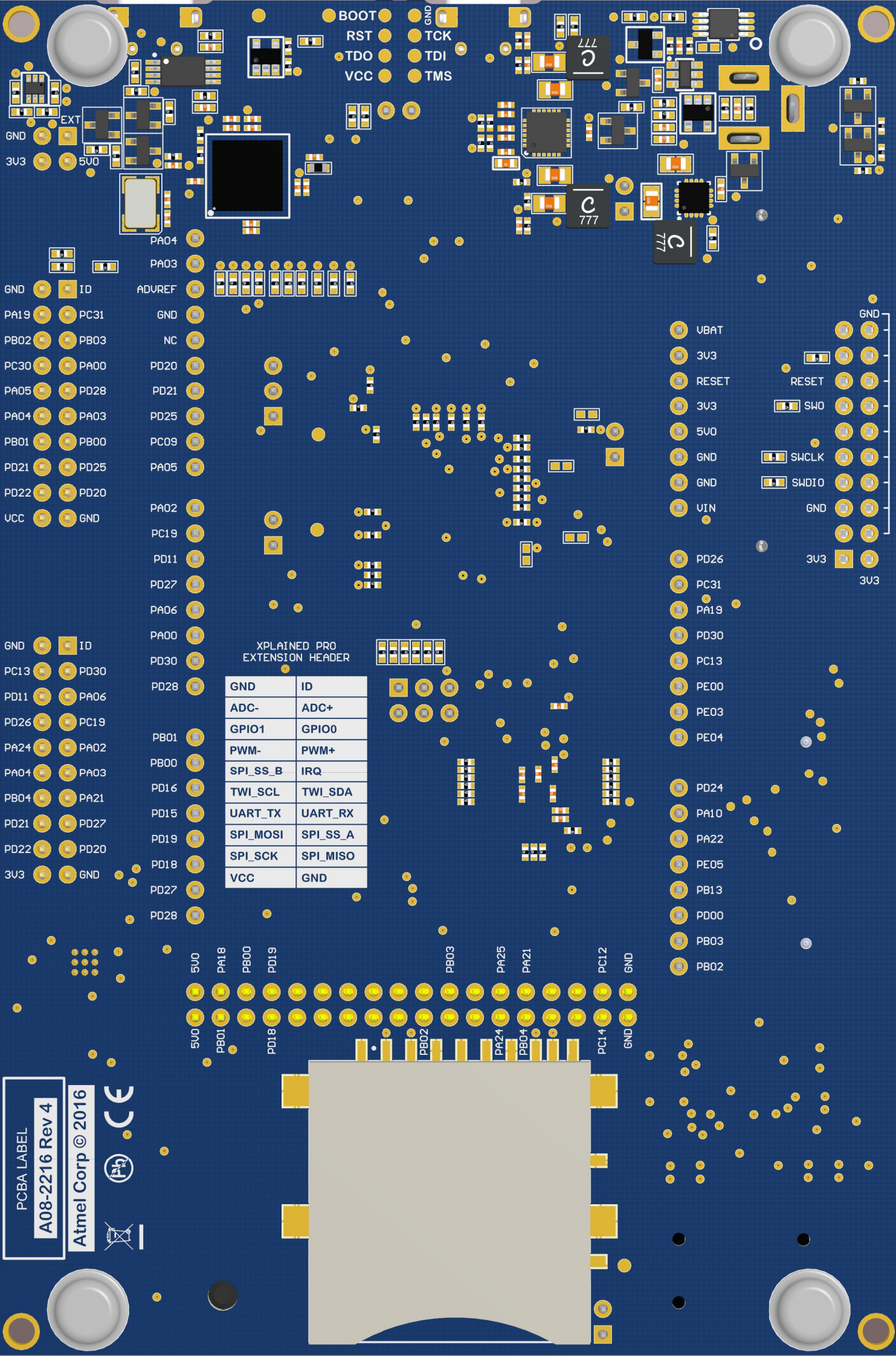
PCBA LABEL
A08-2216 Rev 4

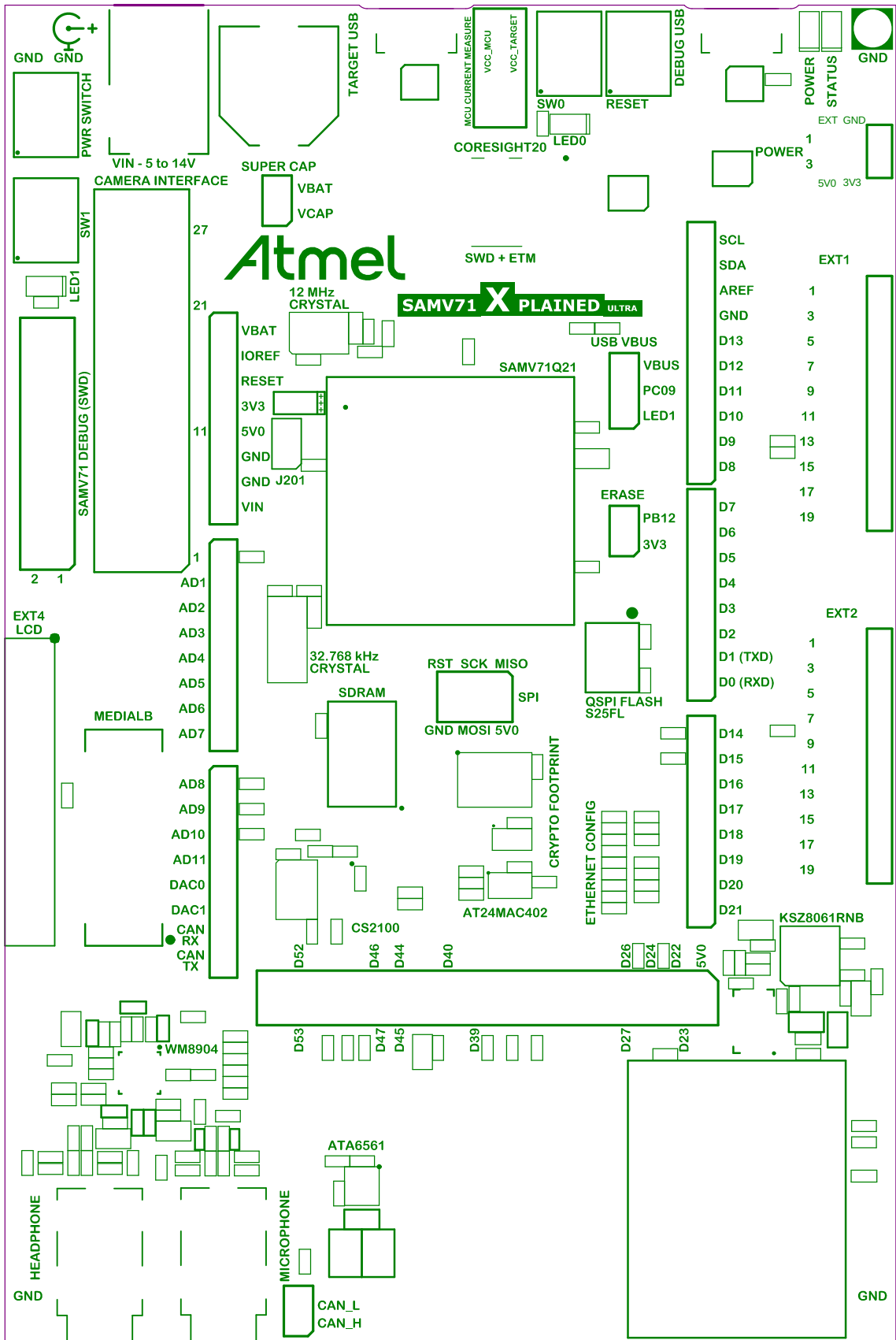
Atmel Corp © 2016

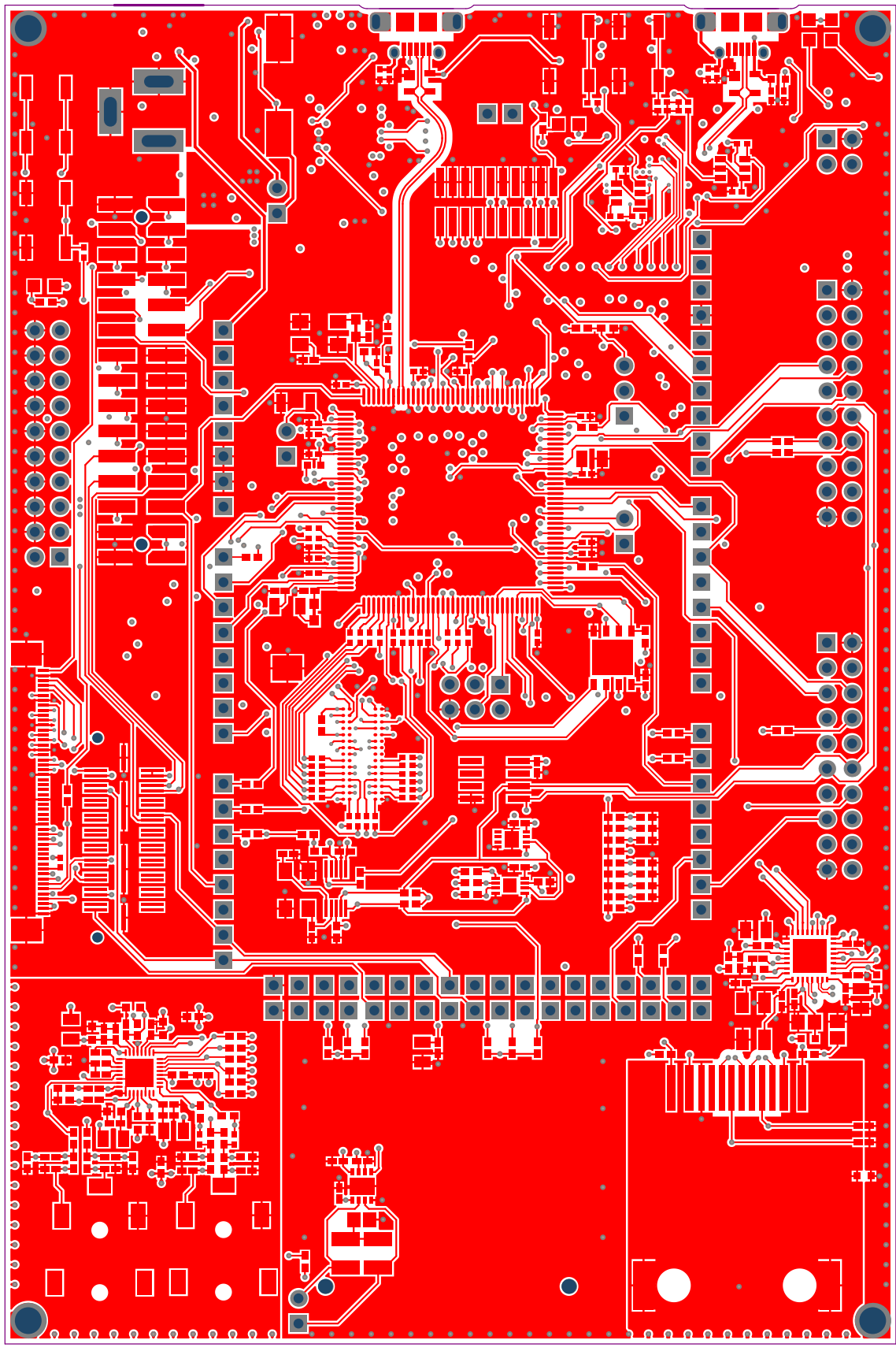


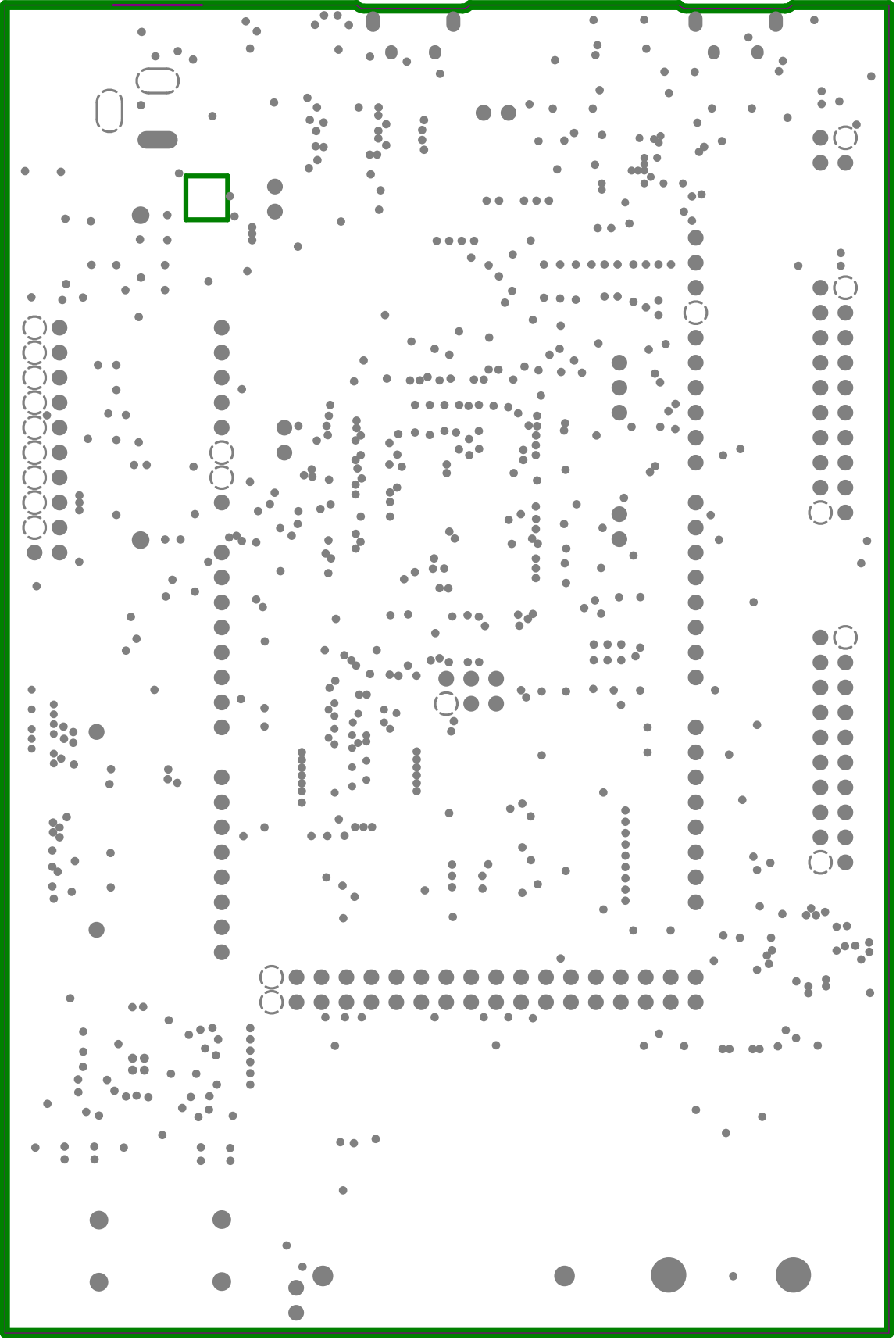
GND	ID
ADC-	ADC+
GPIO1	GPIO0
PWM-	PWM+
SPI_SS_B	IRQ
TWI_SCL	TWI_SDA
UART_TX	UART_RX
SPI_MOSI	SPI_SS_A
SPI_SCK	SPI_MISO
VCC	GND

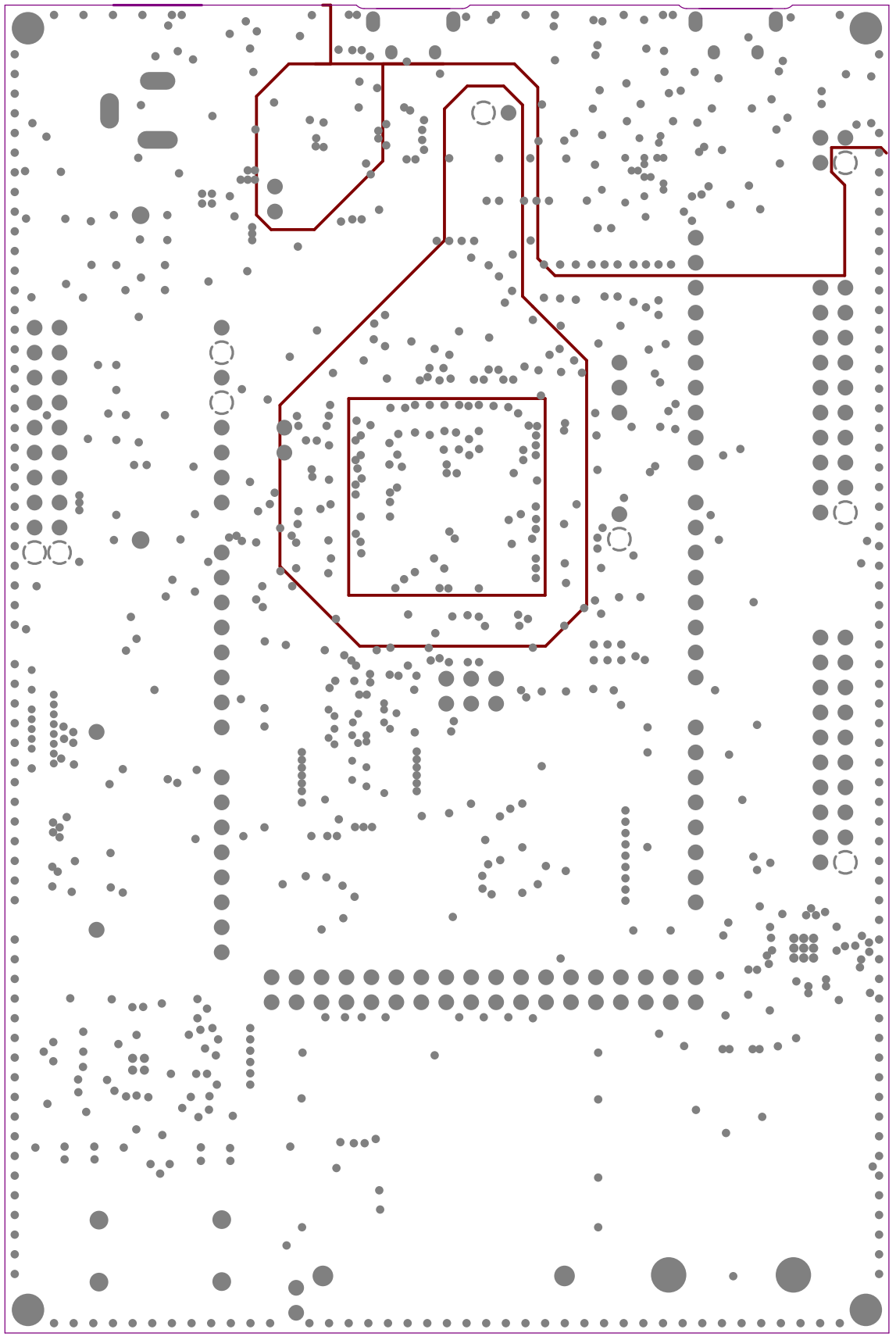
XPLAINED PRO
EXTENSION HEADER

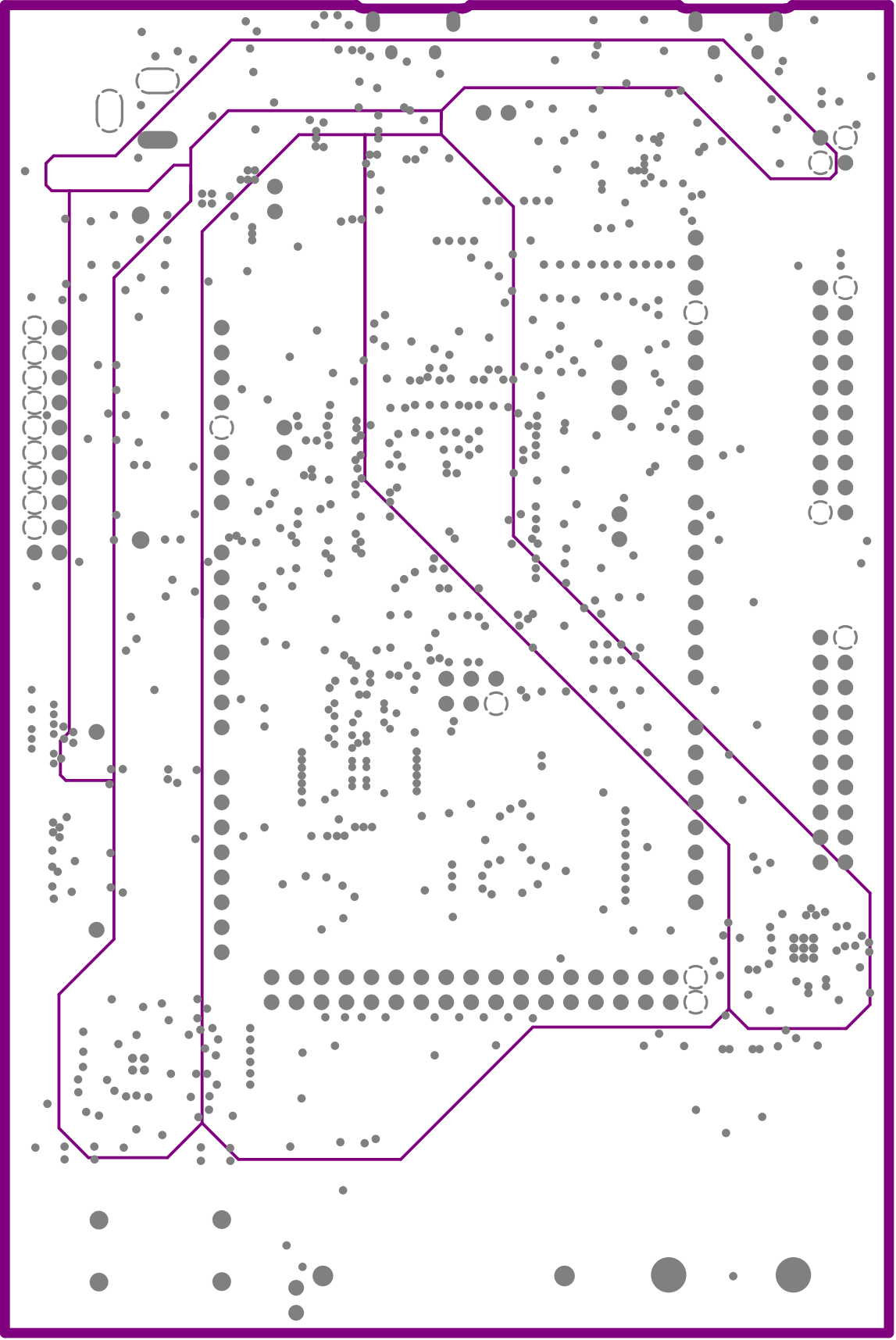


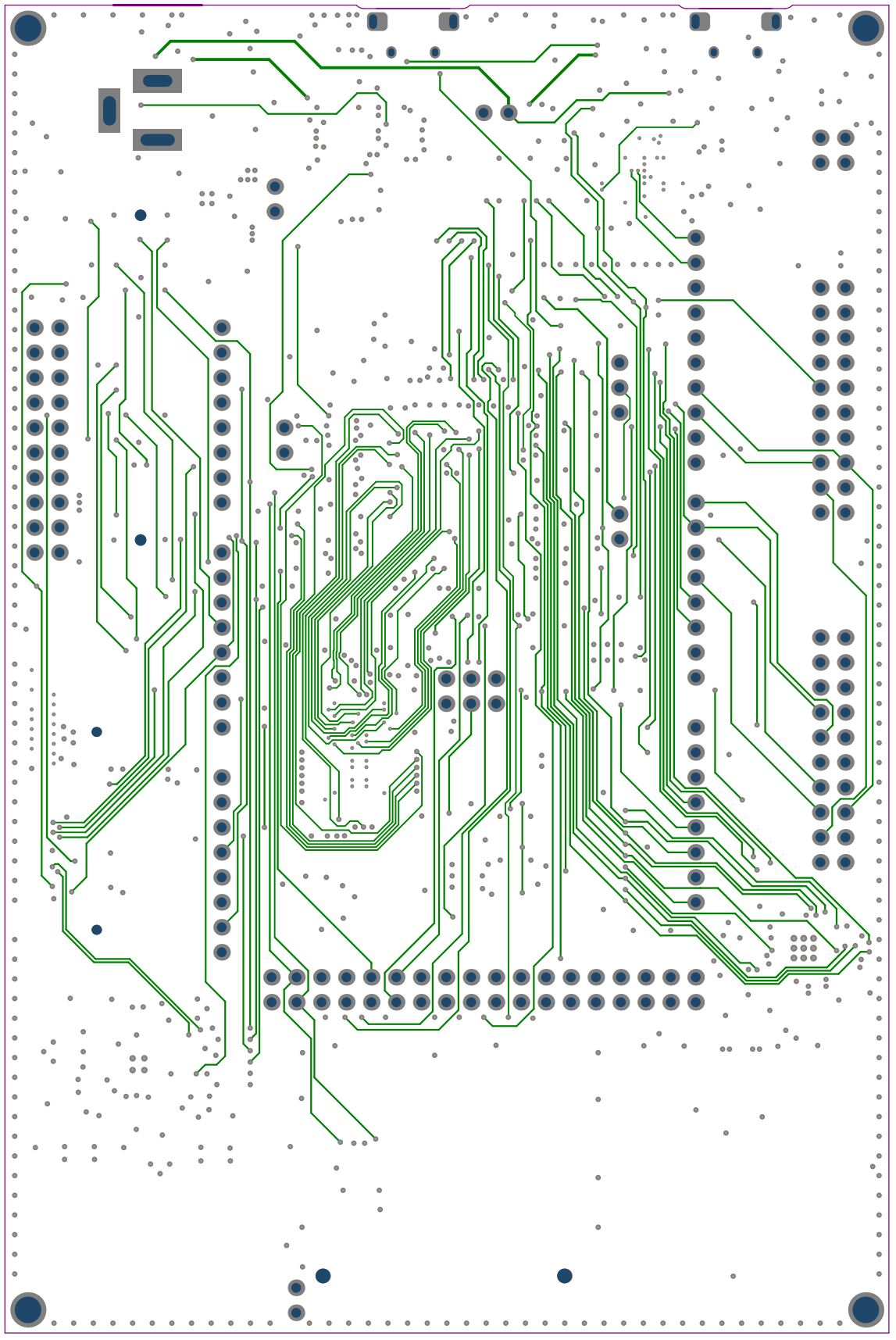


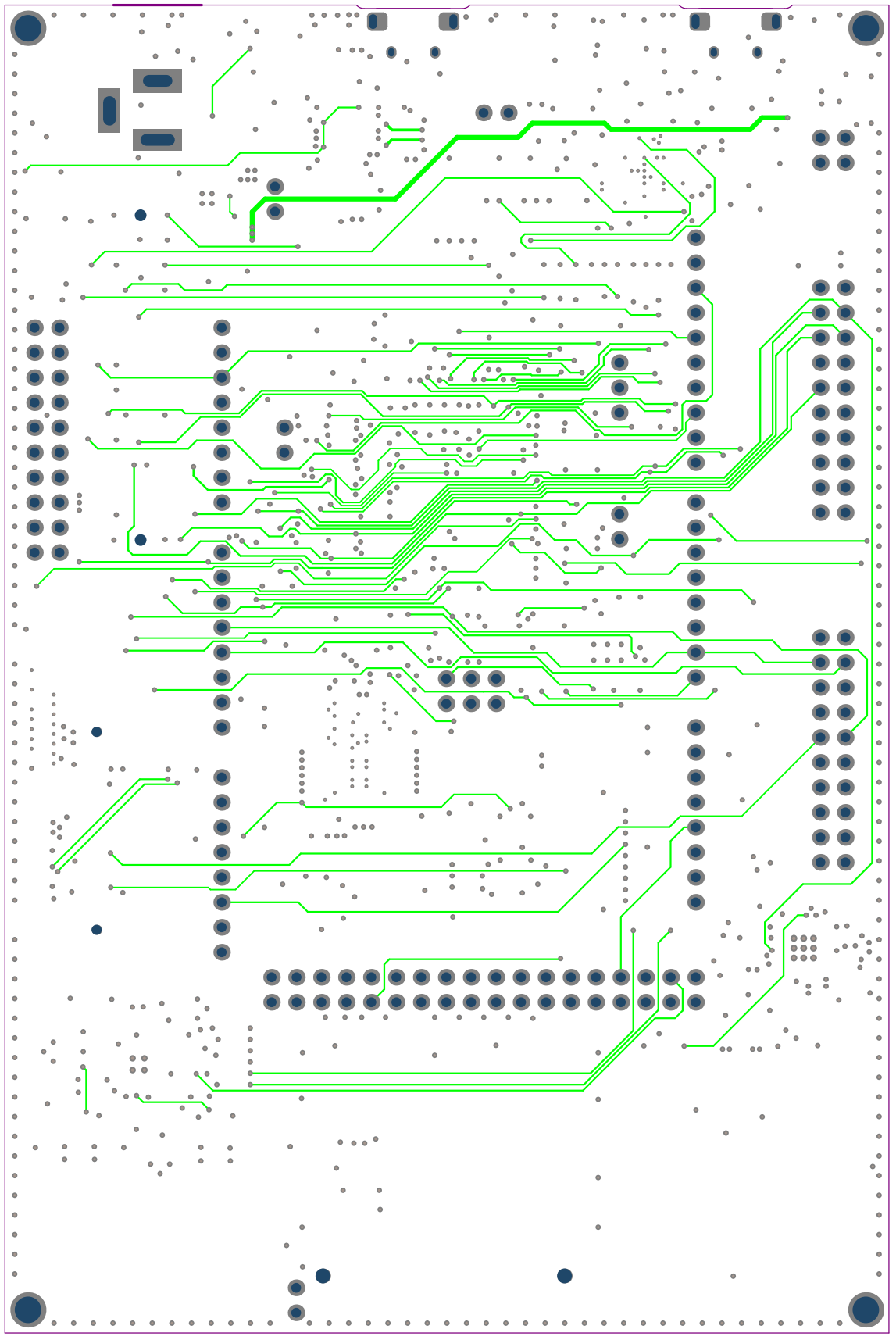


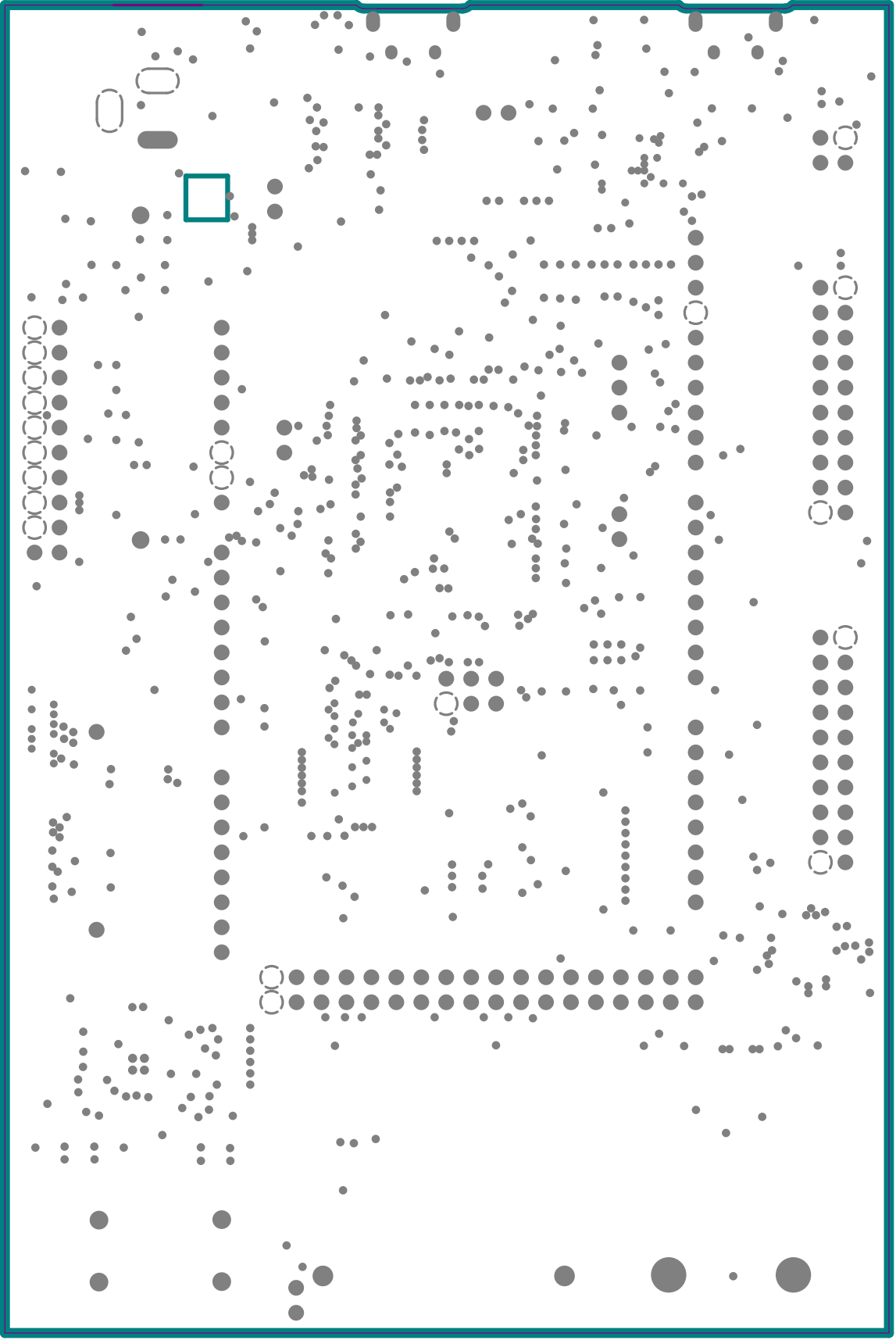


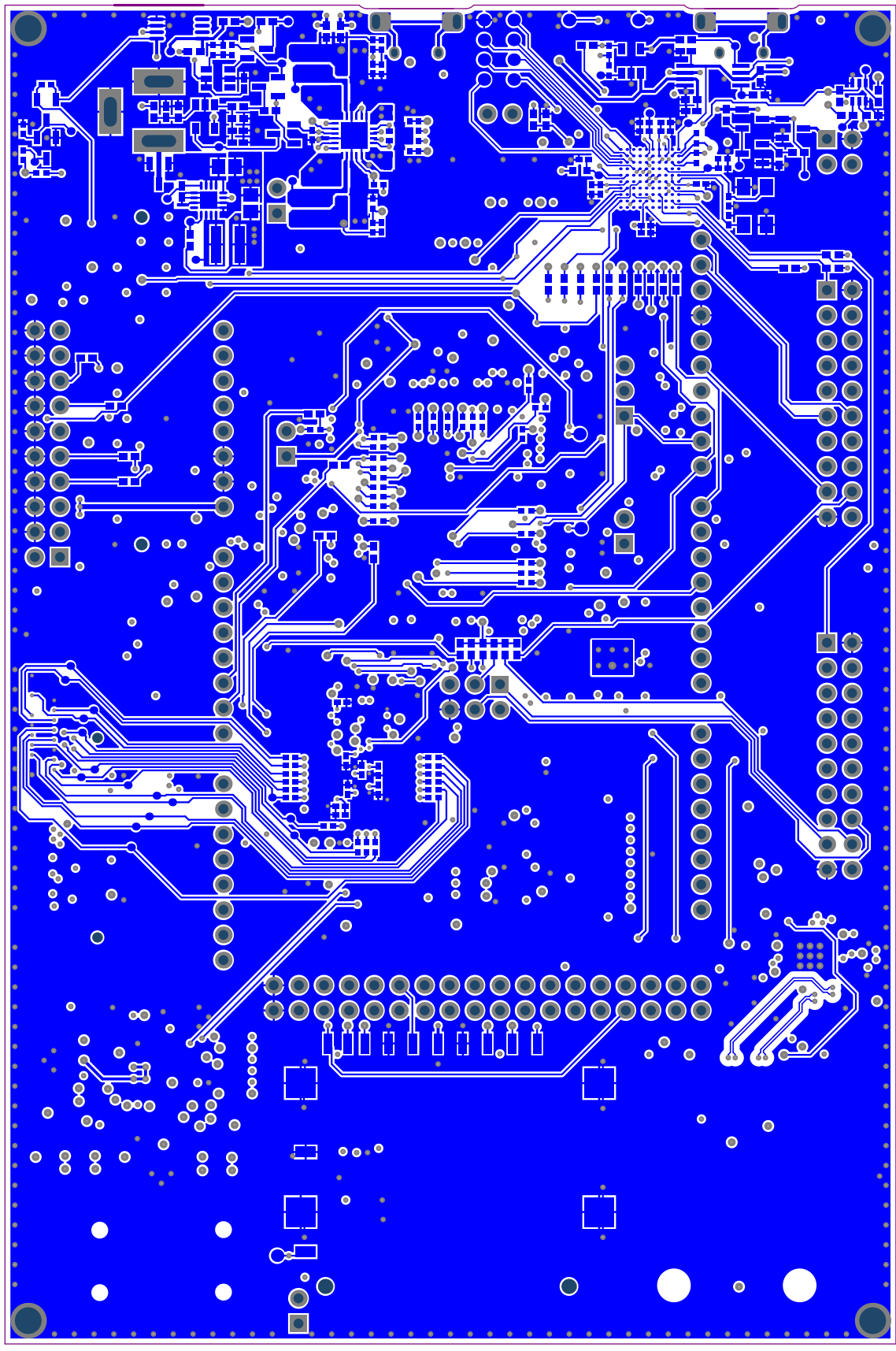


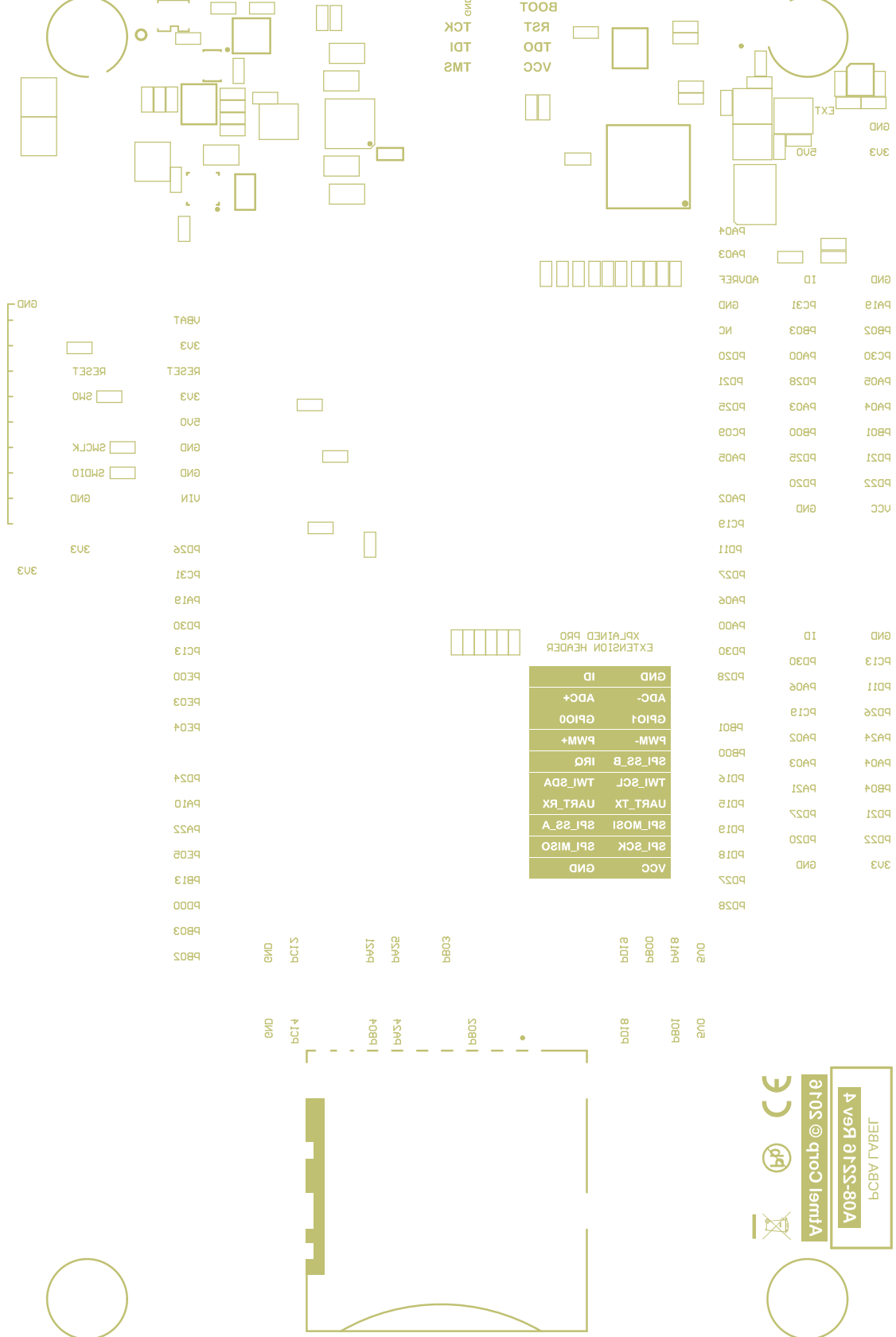












Bill of Materials Fitted For Variant [Default_assembly] of Project [SAMV71_Xplained_Ultra.PrjPCB] (No PCB Document Selected)

SAMV71_Xplained_Ultra_PriPCB

SAMV71_Xplained_Ultra_PriPCB

Default assembly



Approved	Notes