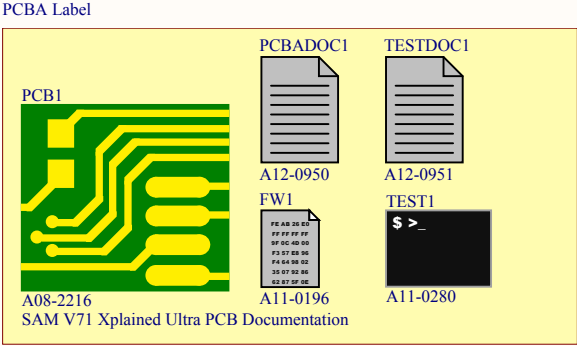
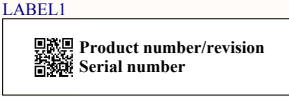
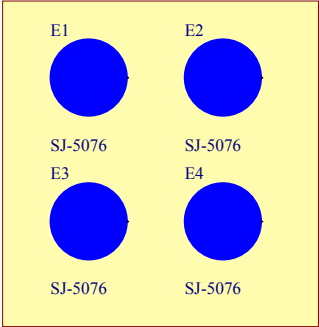
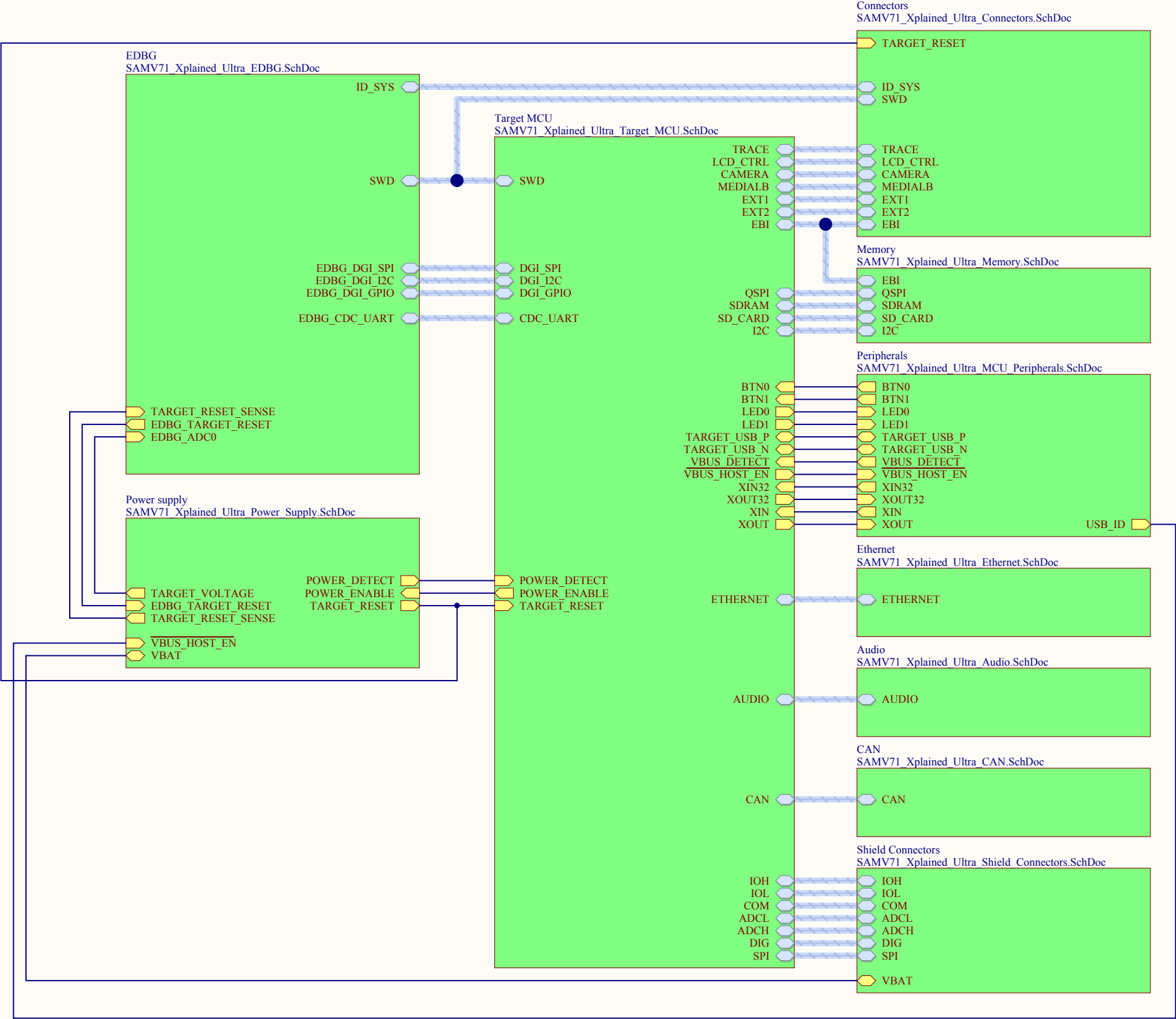


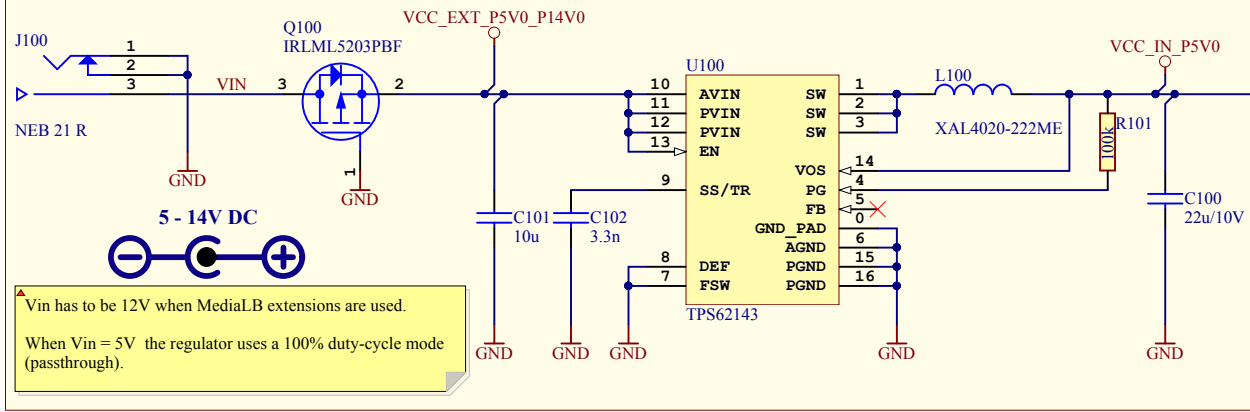
SAM V71 Xplained ULTRA



ATMEL Norway	*				
Vestre Rosten 79	*				
N-7075 TILLER	*				
NORWAY					
Date:	24.08.2016	16:04:46	PAGE:	1 of 13	
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TITLE: Top Level Schematics					
SAMV71_Xplained_Ultra_TopLevel.SchDoc					



5V to 14V input, 5V out Power Supply



Power inputs to SAM V71 Xplained Ultra:
VCC_EXT_P5V0_P14V0:
2.1mm power jack with positive center. This voltage is used to generate VCC_EXT_P5V0, the regulator supports 5V to 17V input voltage. If MediaLB is not used the input voltage can be 17V.

VCC_EXT_P5V0:
This power input can be used to power the whole board and it has a higher priority as the USB power inputs. Connect a power supply if a target MCU with USB host is present and VCC_EXT_P5V0_P17V0 is not used. 4.3V to 5.5V is possible but for USB host operation and in case on-board devices use this voltage it should be 5V +-2%.

VCC_EDBG_USB_P5V0:
EDBG USB power input. This supply is used when VCC_EXT_P5V0 is not present.

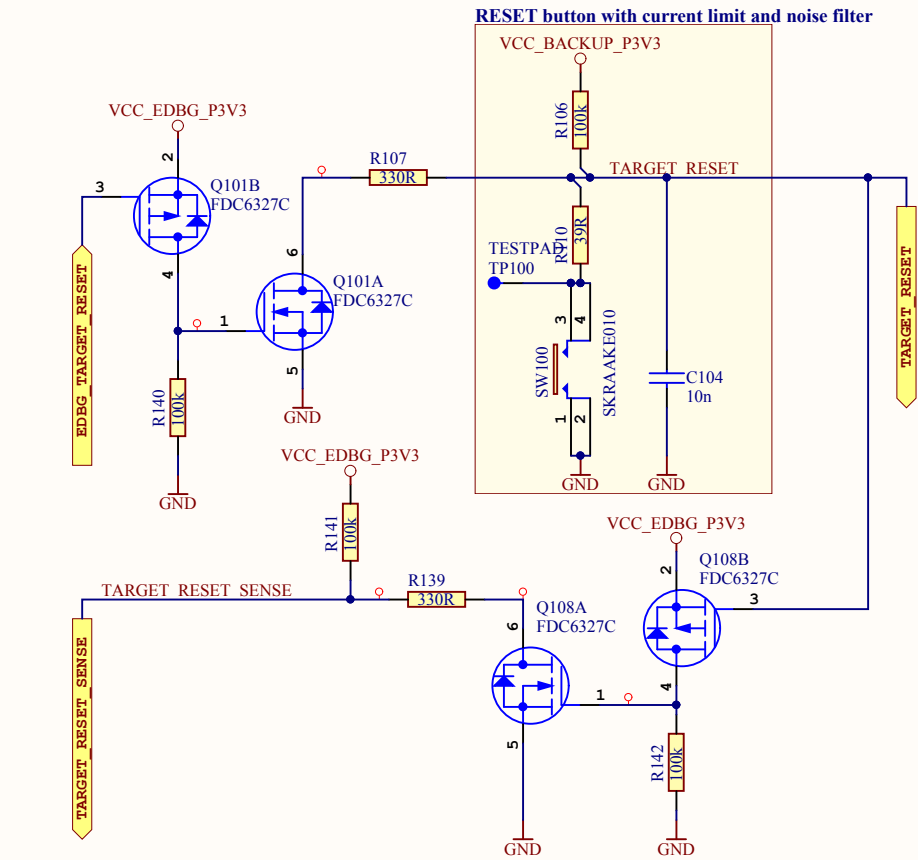
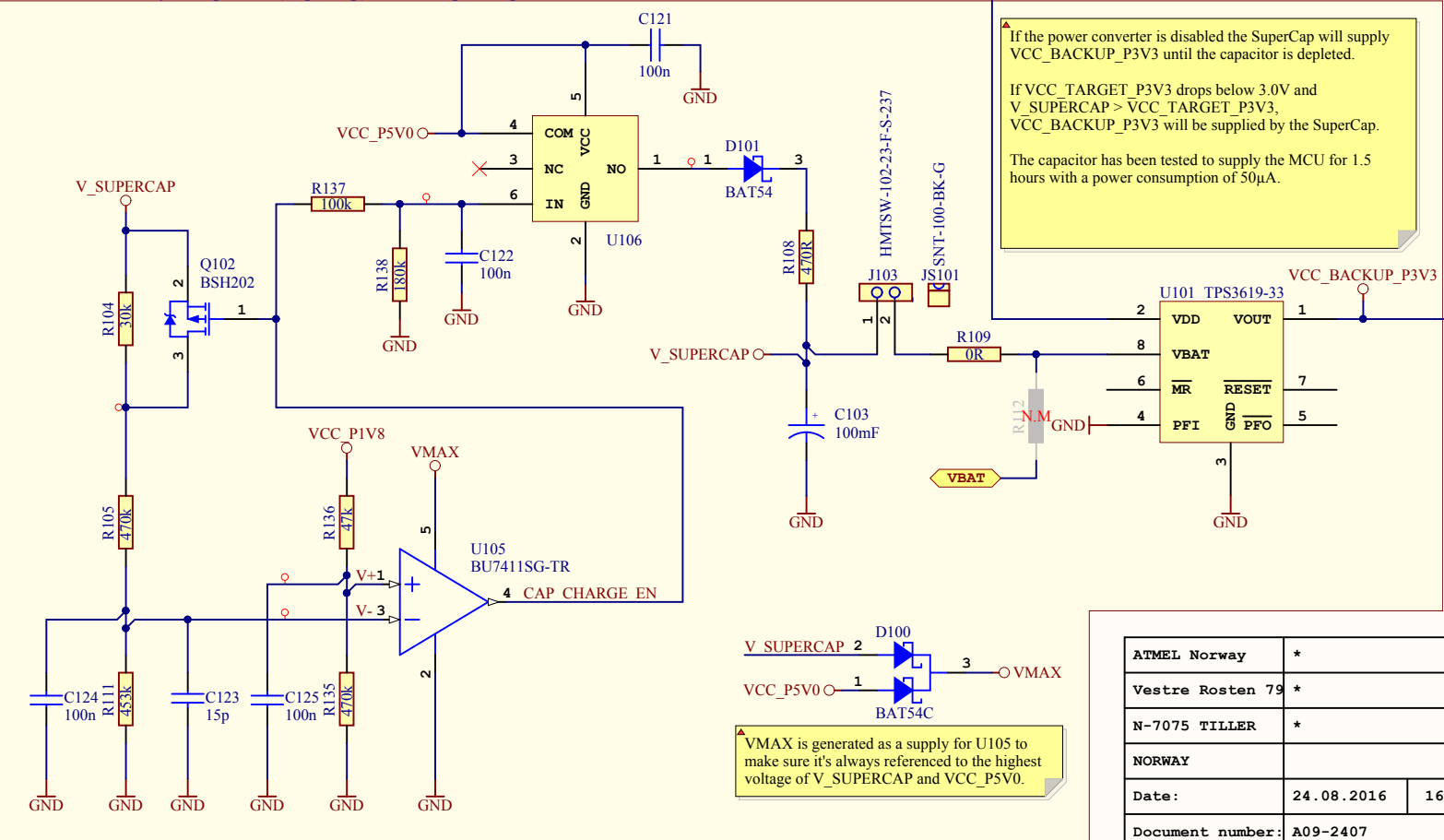
VCC_TARGET_USB_P5V0:
Target MCU USB power input. It is used to power the whole board when no other 5V power supply is present.

Other voltages:
VCC_P5V0:
This supply is connected to either VCC_EXT_P5V0, VCC_EDBG_USB_P5V0 or VCC_TARGET_USB_P5V0, based on the availability and priority of these supplies.

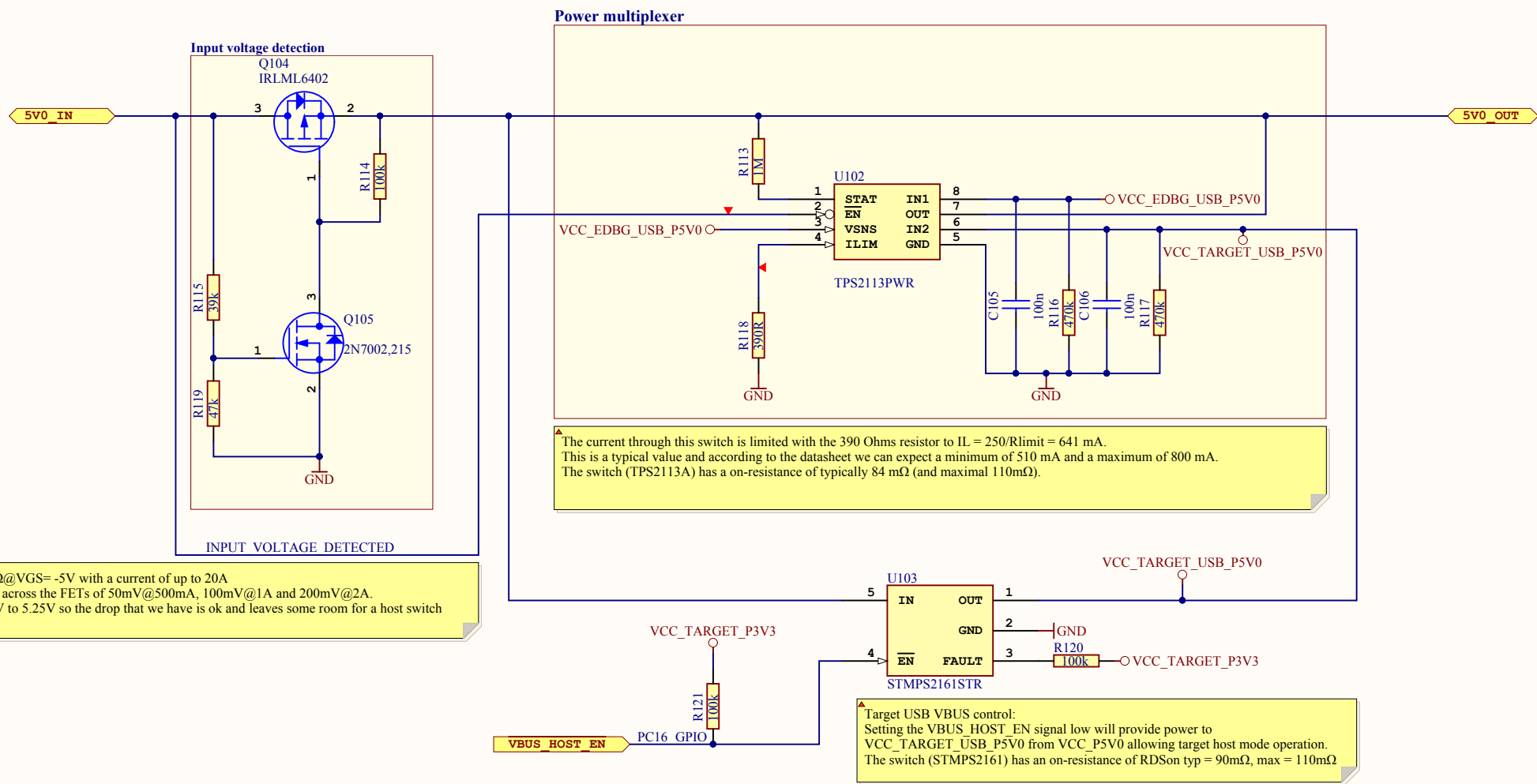
VCC_P3V3: Regulated 3.3V from VCC_P5V0
VCC_P2V0: Regulated 2.0V from VCC_P5V0
VCC_P1V8: Regulated 1.8V from VCC_P5V0
VCC_P1V2: Regulated 1.2V from VCC_P5V0

VCC_TARGET_P3V3: Target supply voltage (target MCU, peripherals, connectors and SuperCap charge)
VCC_BACKUP_P3V3: Powers target MCU, can be supplied from either VCC_TARGET_P3V3 or V_SUPERCAP.
V_SUPERCAP: The SuperCap is charged to 3.52V from VCC_P5V0 when that voltage is present. V_SUPERCAP is used to supply target MCU when the voltage regulator for VCC_P3V3 is turned off, intended for sleep mode and currents below 100µA.

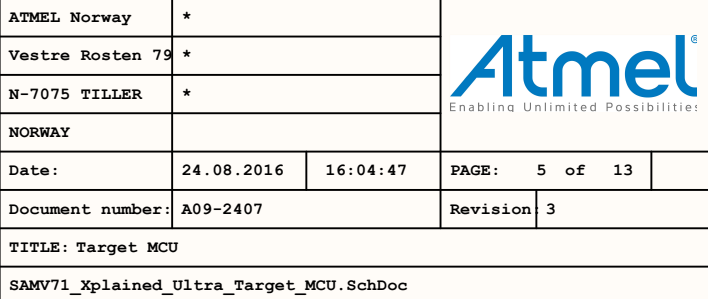
Electric Double-Layer Capacitor (Supercap) for backup voltage

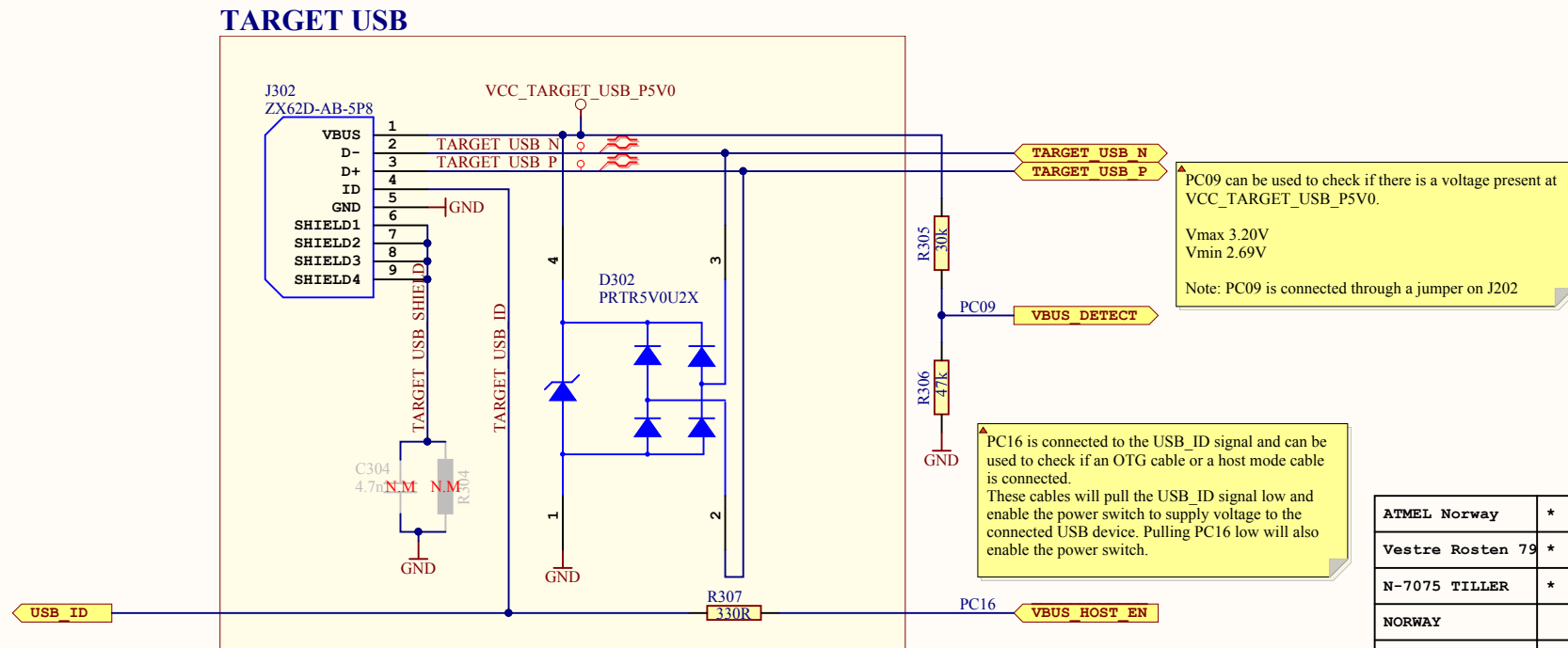
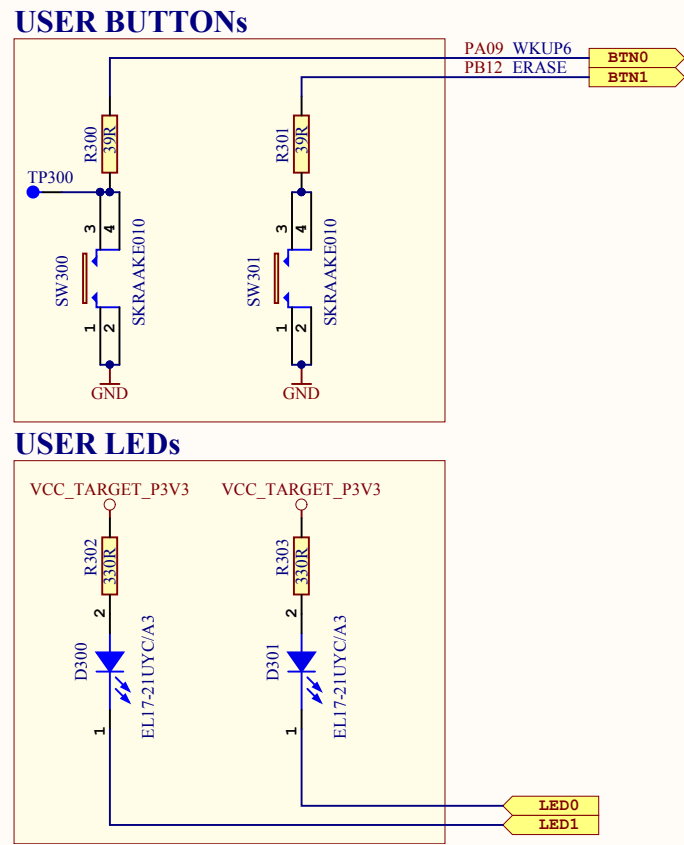
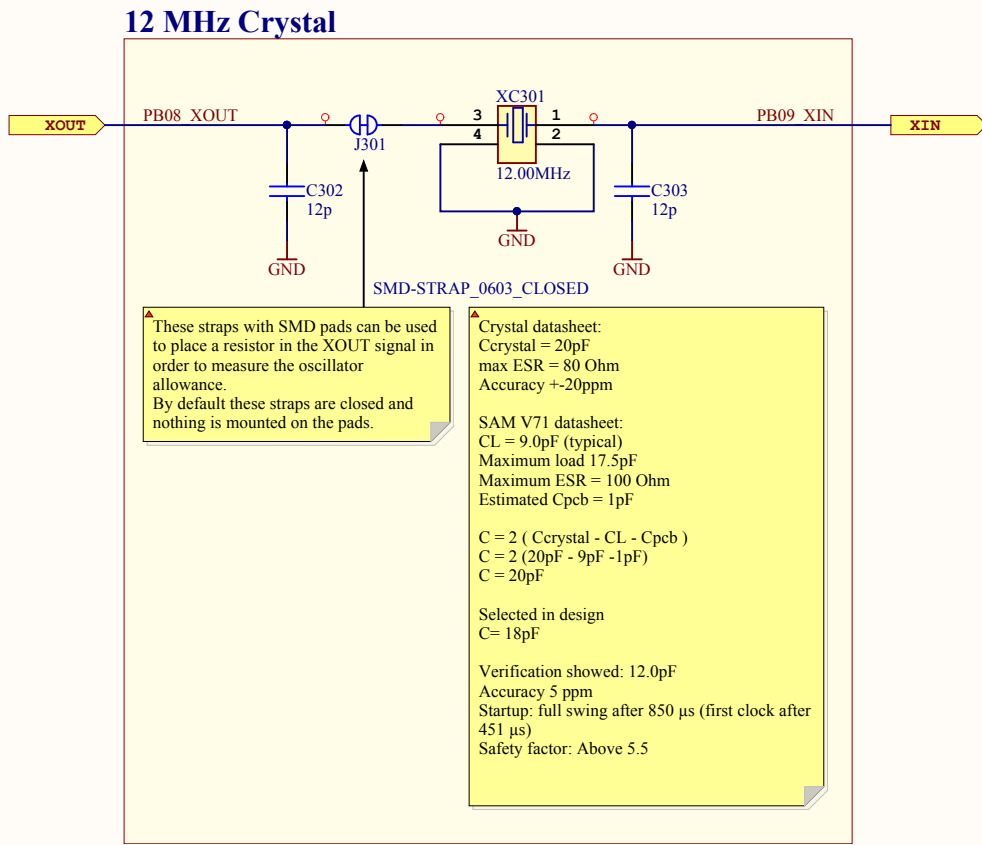
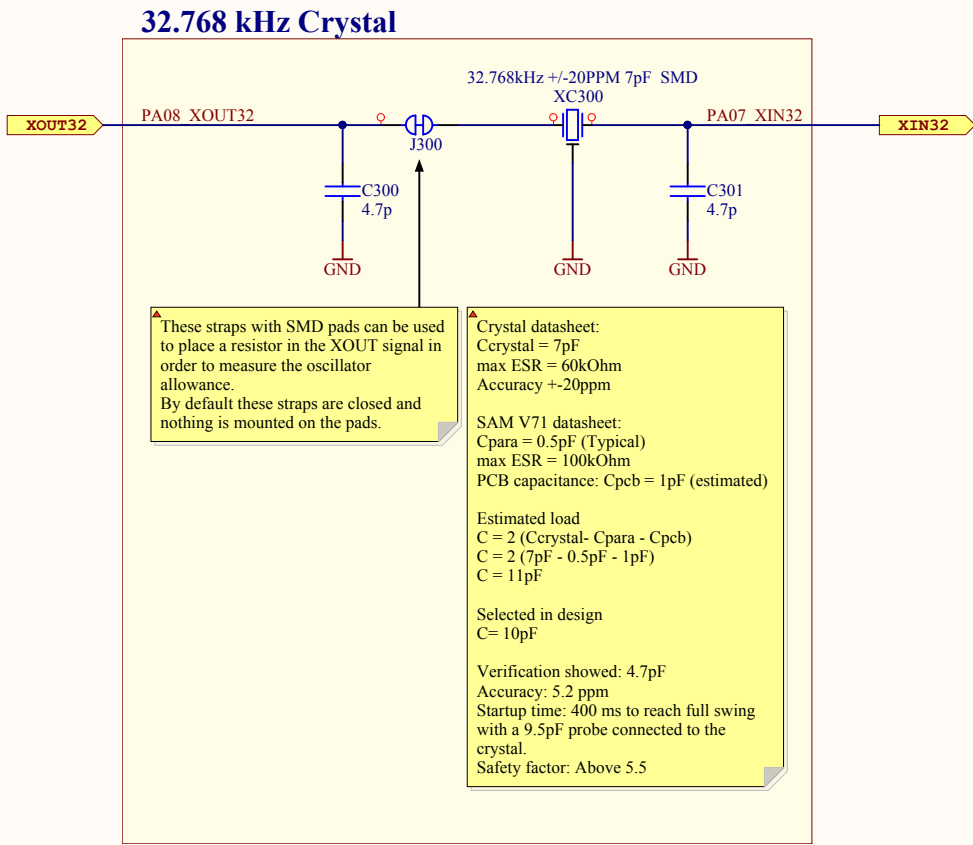


ATMEL Norway	*	 Enabling Unlimited Possibilities!		
Vestre Rosten 79	*			
N-7075 TILLER	*			
NORWAY				
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SAMV71_Xplained_Ultra_Power_Supply.SchDoc				

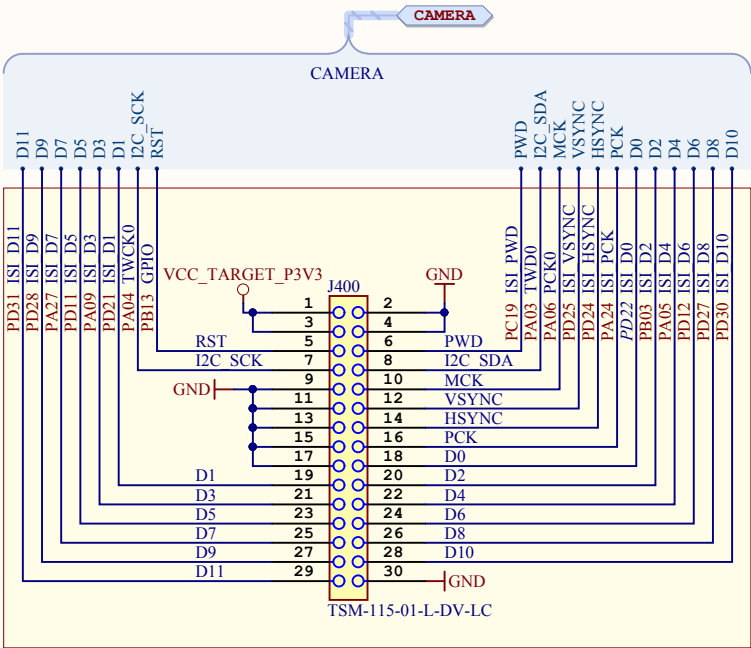


ATMEL Norway	*		 Enabling Unlimited Possibilities	
Vestre Rosten 79	*			
N-7075 TILLER	*			
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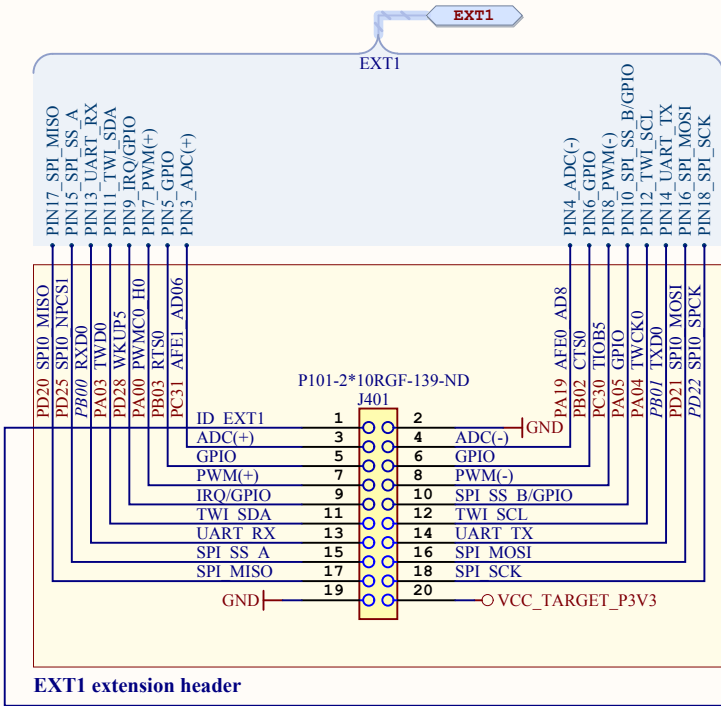




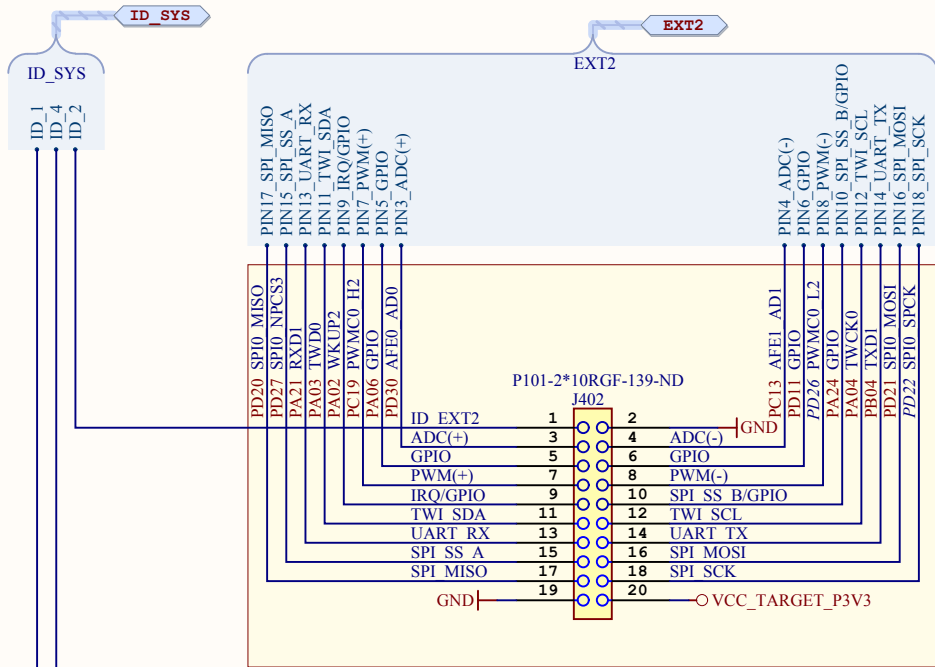
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N-7075 TILLER	*			
NORWAY				
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SAMV71_Xplained_Ultra_MCU_Peripherals.SchDoc				



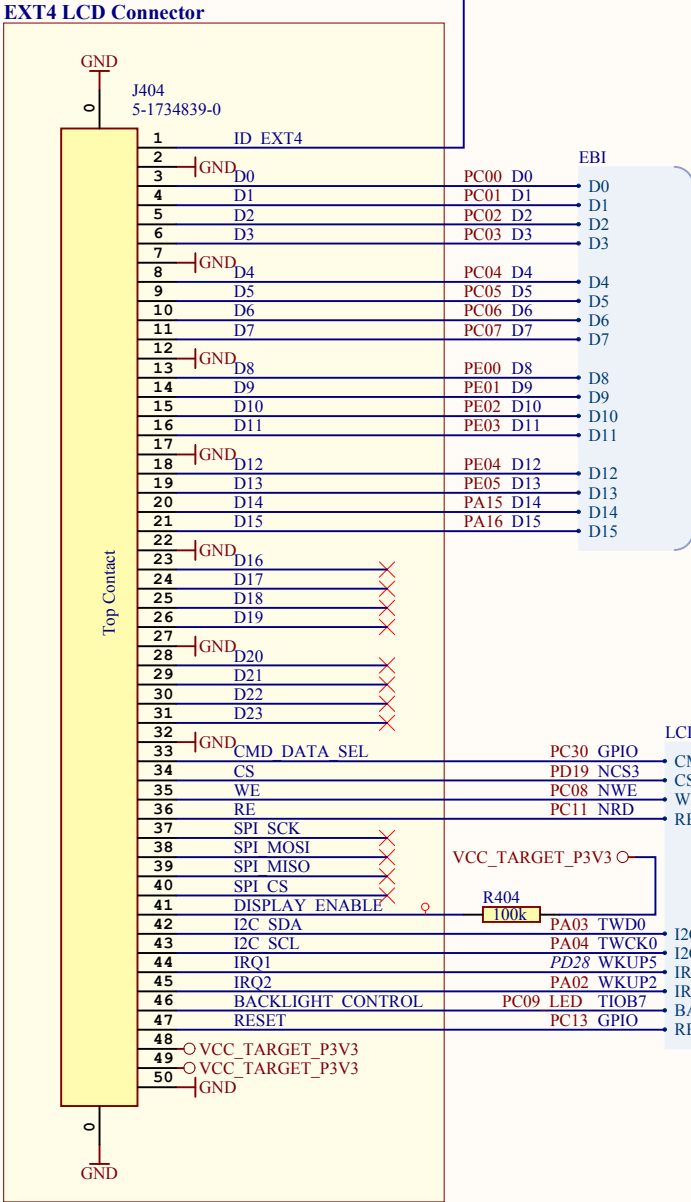
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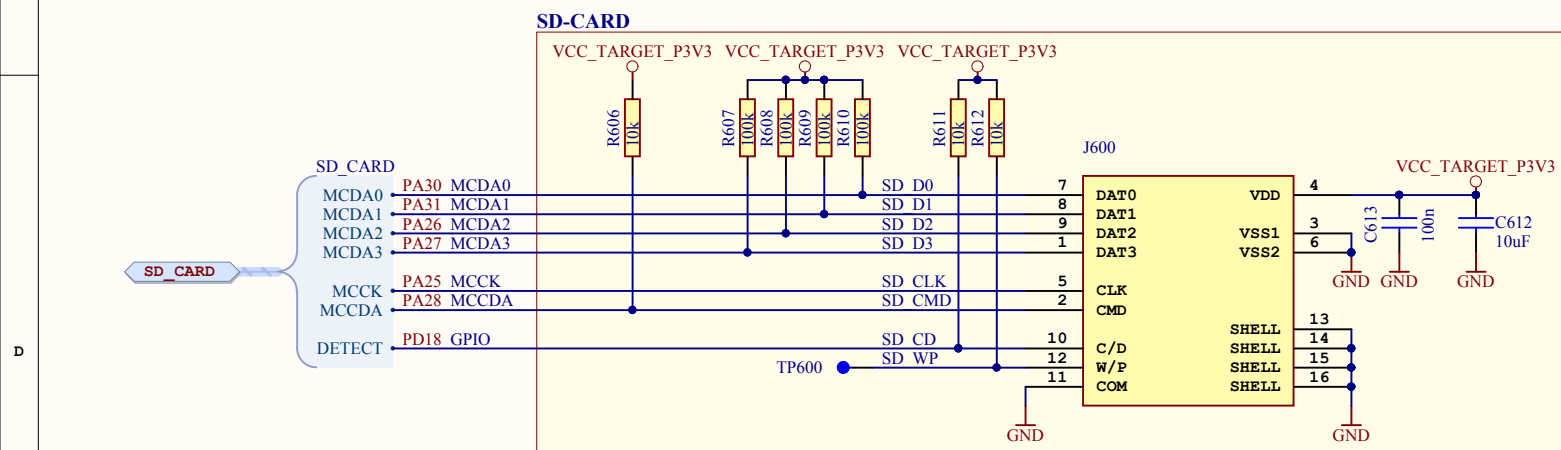
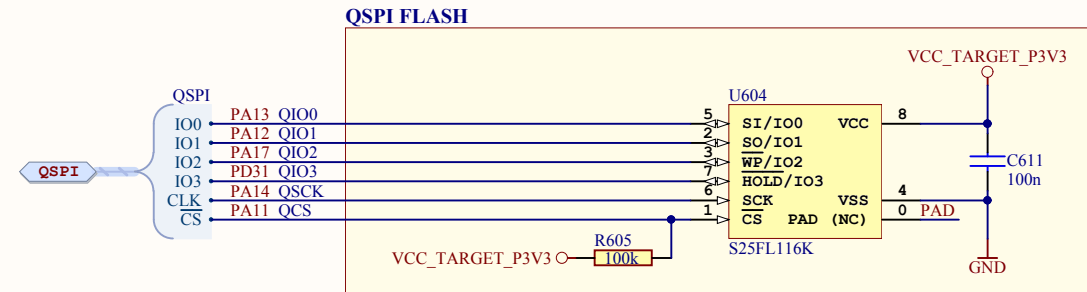
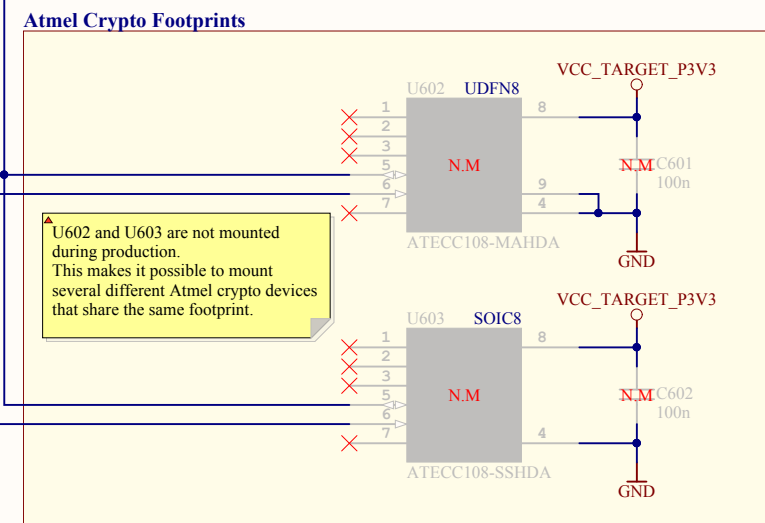
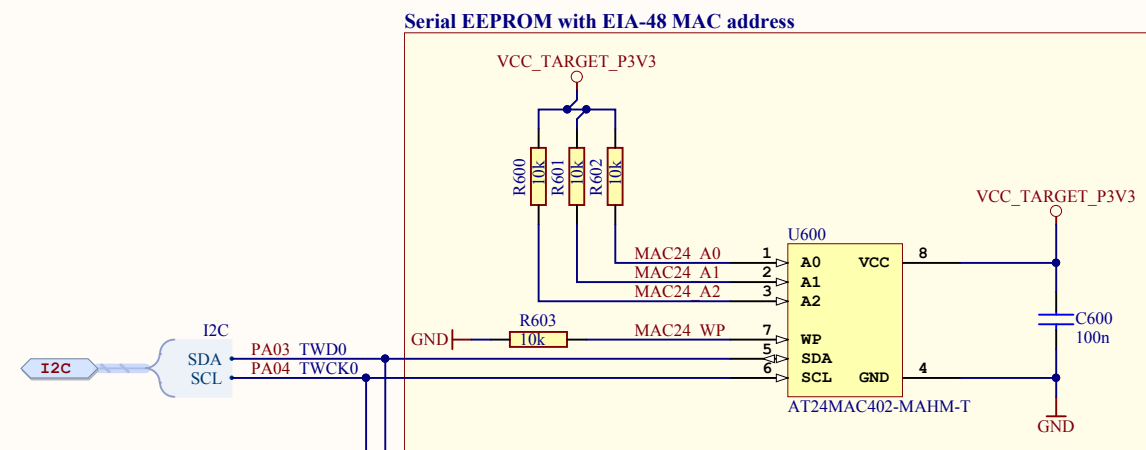
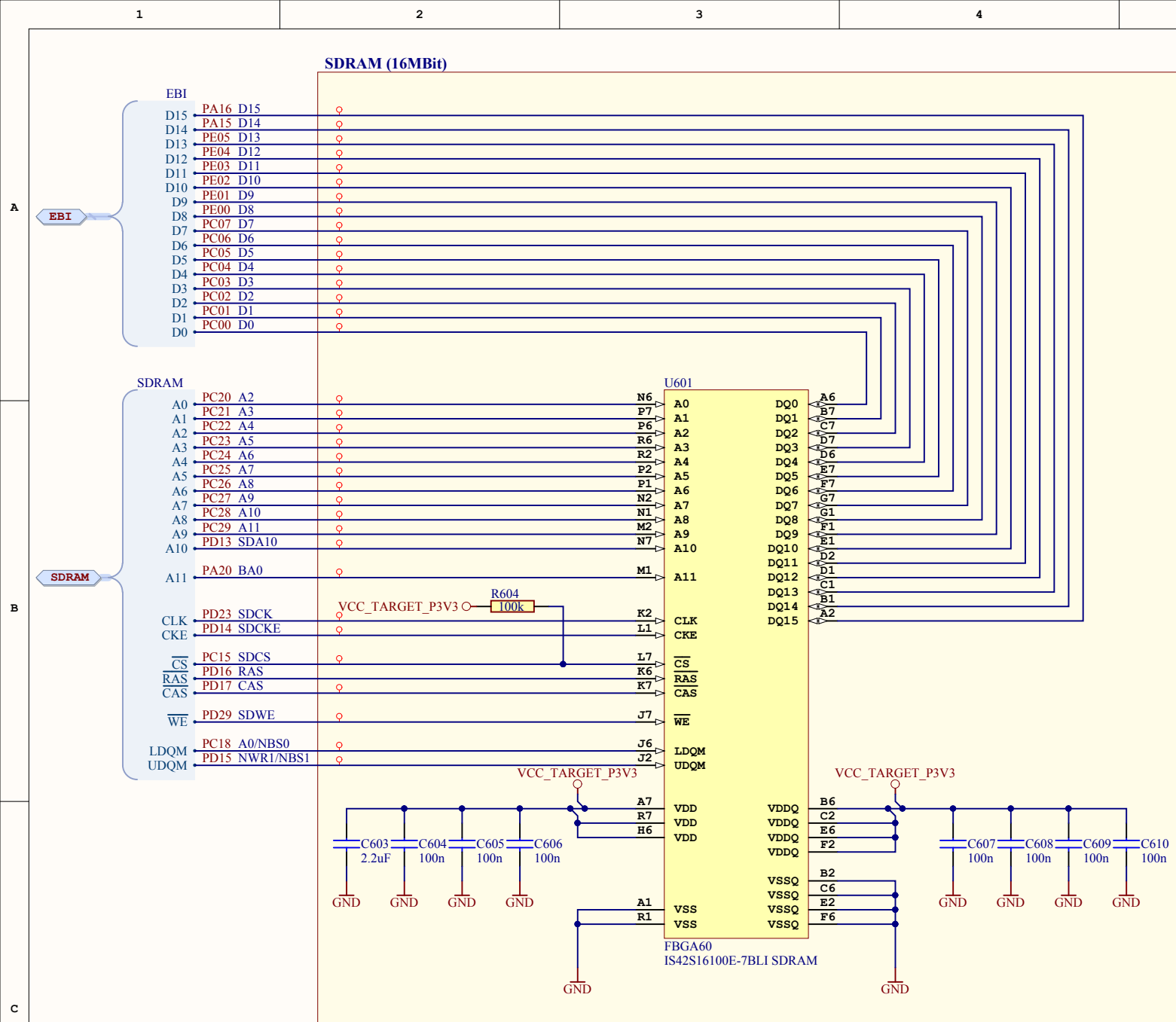


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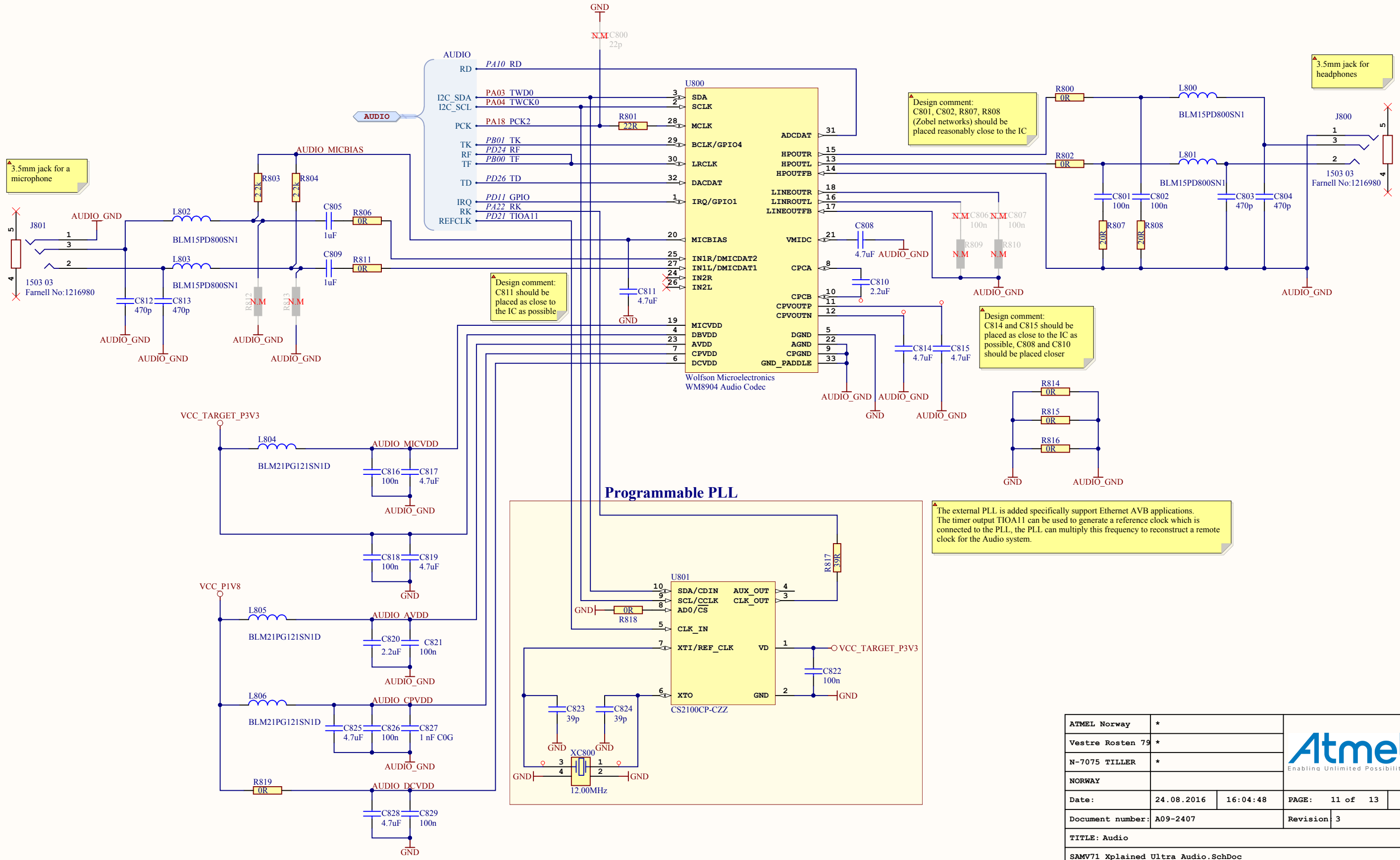


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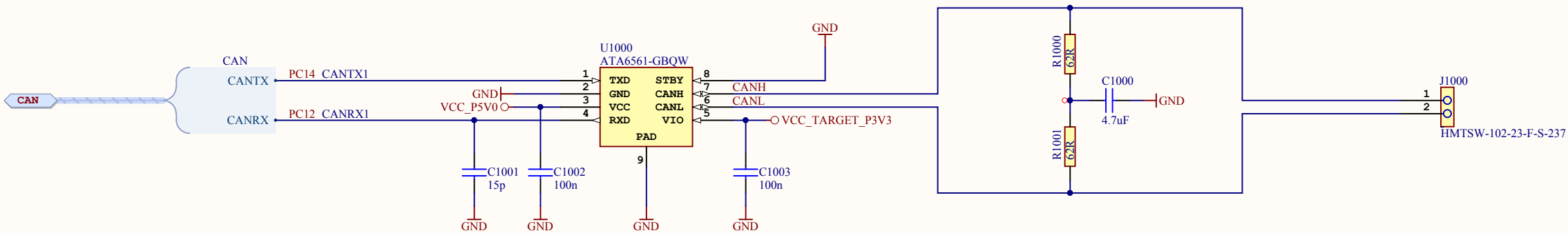




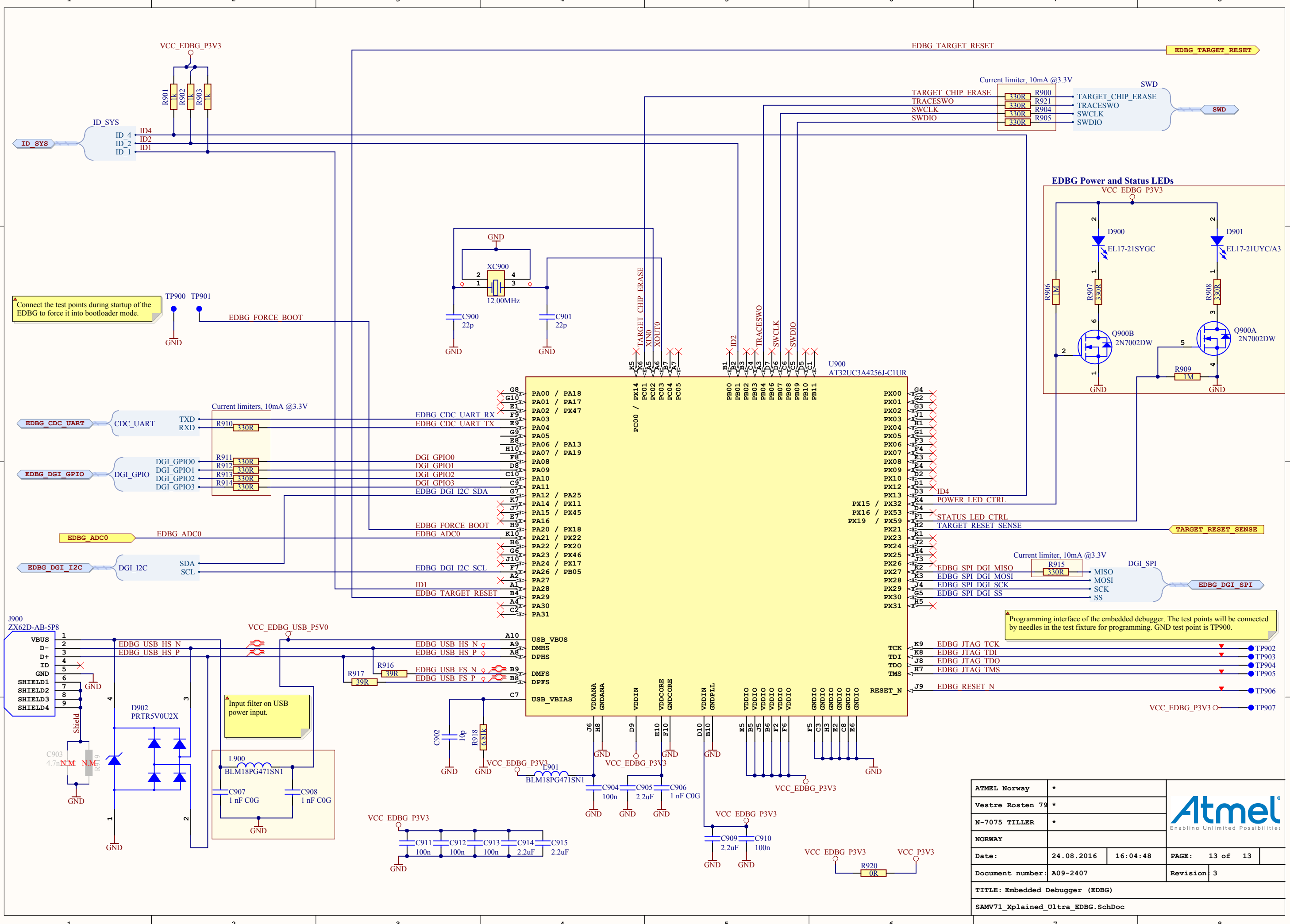
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Vestre Rosten 79	*			
N-7075 TILLER	*			
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SAMV71_Xplained_Ultra_Memory.SchDoc				



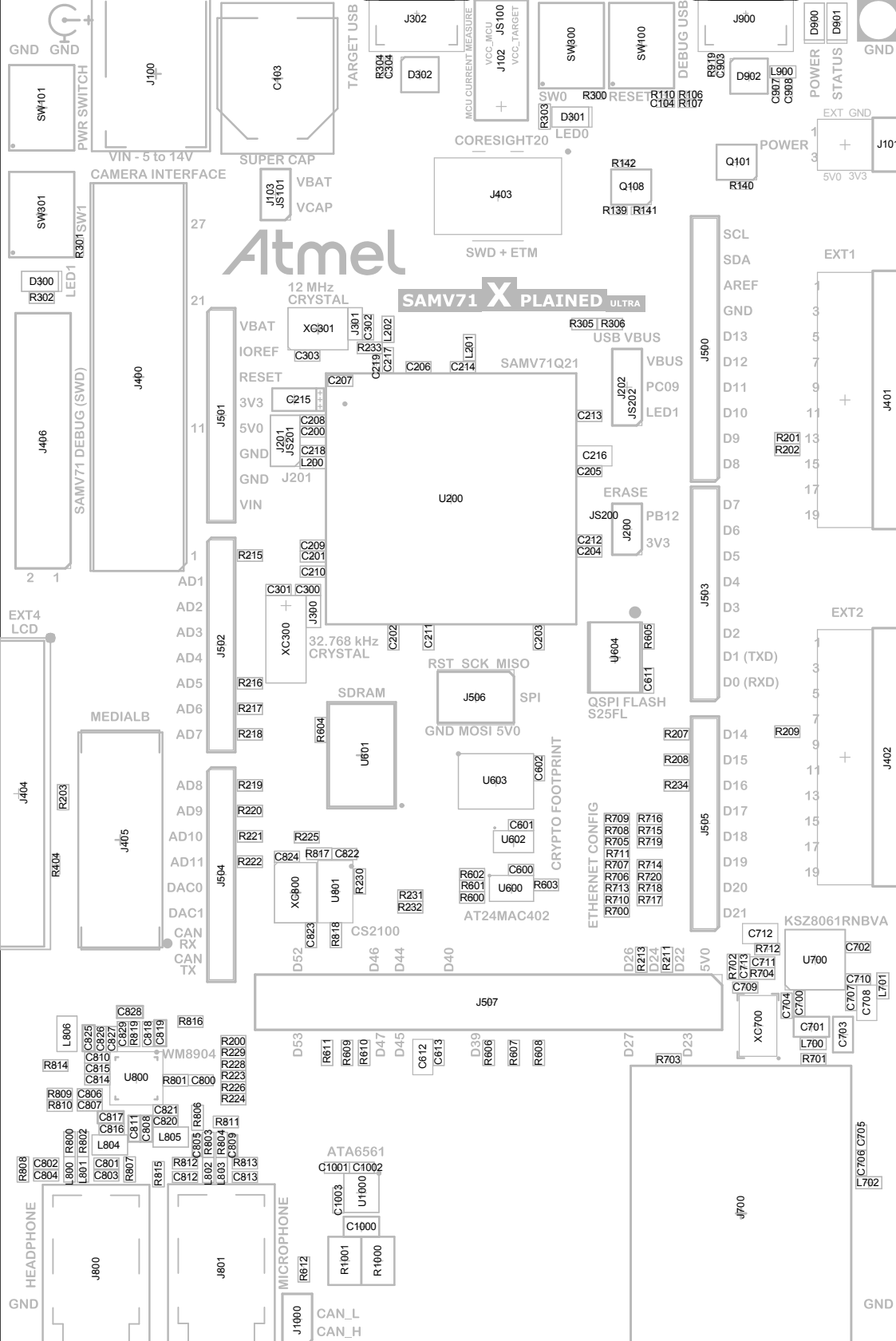
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N-7075 TILLER		*			
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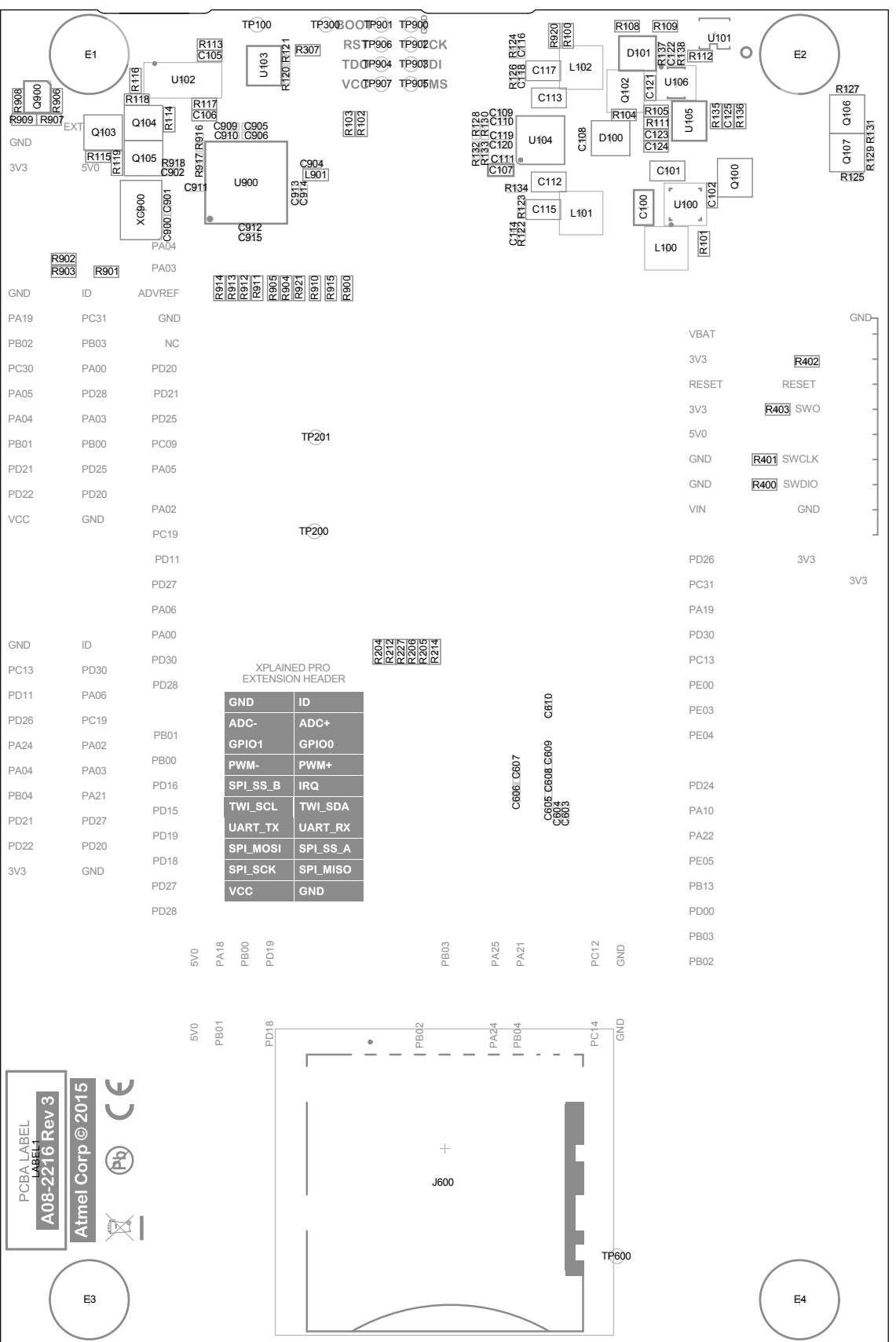


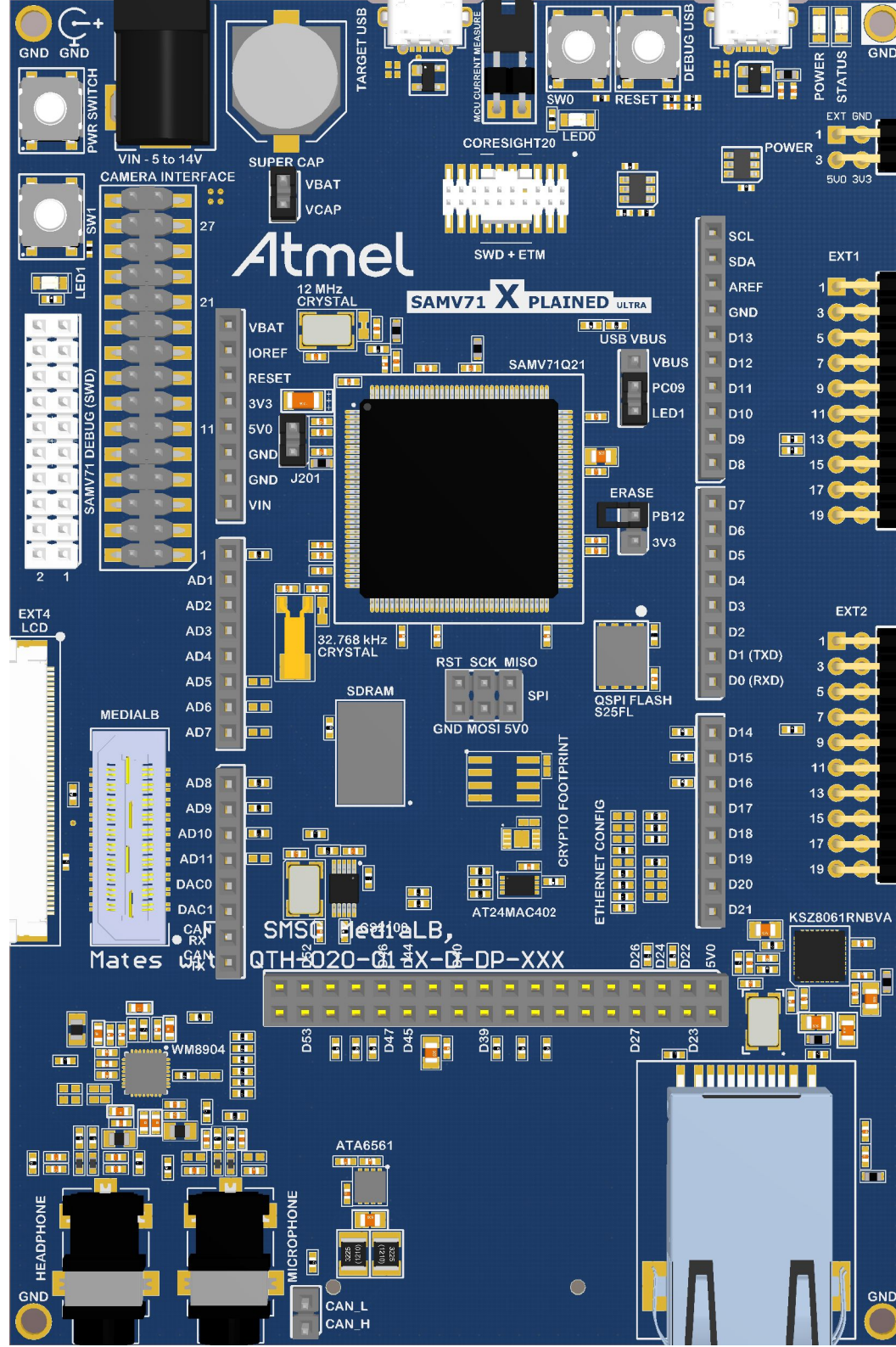
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N-7075 TILLER		*			
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Document number:	A09-2407		Revision:	3	
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SAMV71_Xplained_Ultra_CAN.SchDoc					

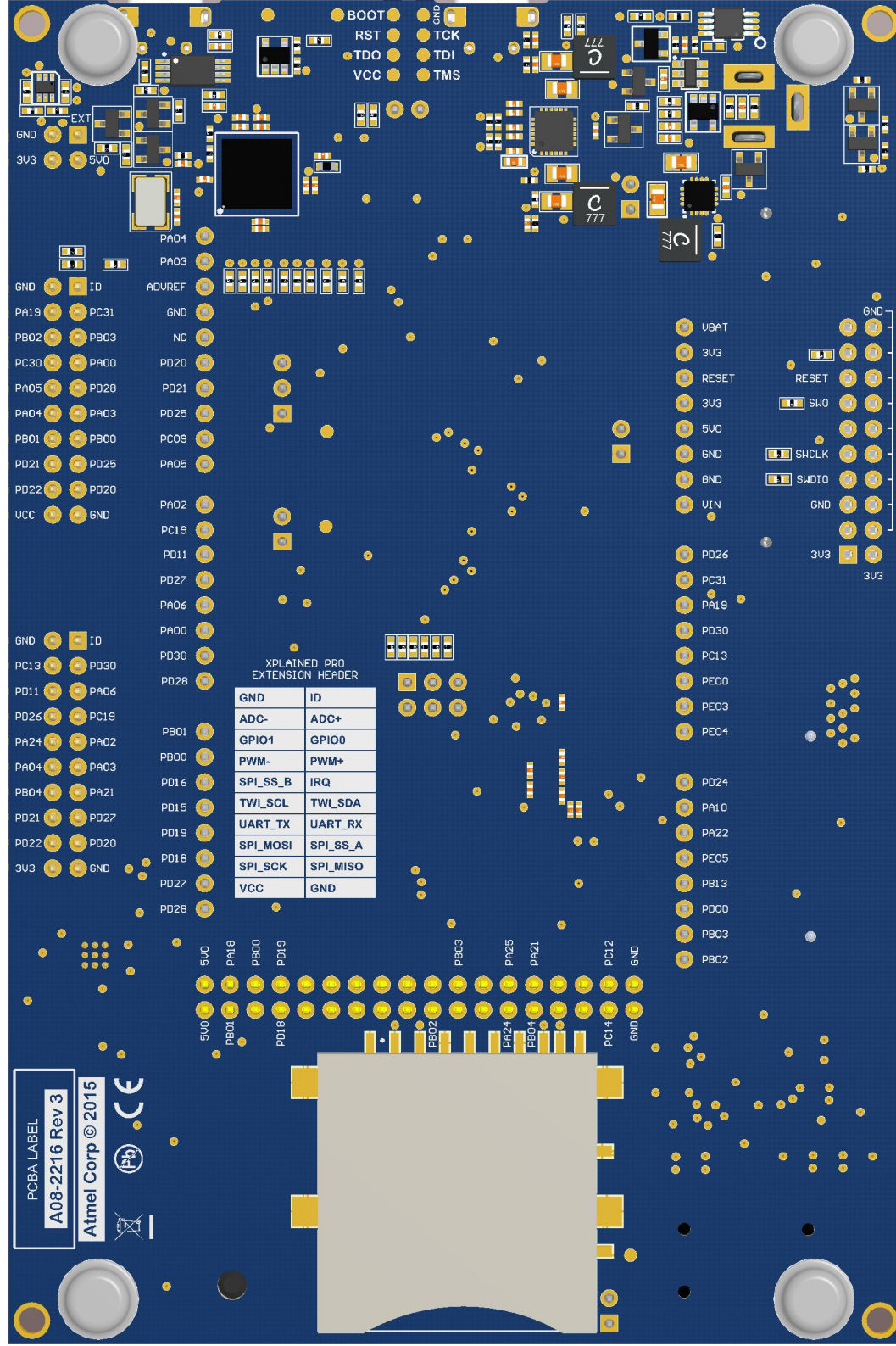


ATMEL Norway		*			
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N-7075 TILLER		*			
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Document number:	A09-2407		Revision:	3	
TITLE: Embedded Debugger (EDBG)					
SAMV71_Xplained_Ultra_EDBG.SchDoc					









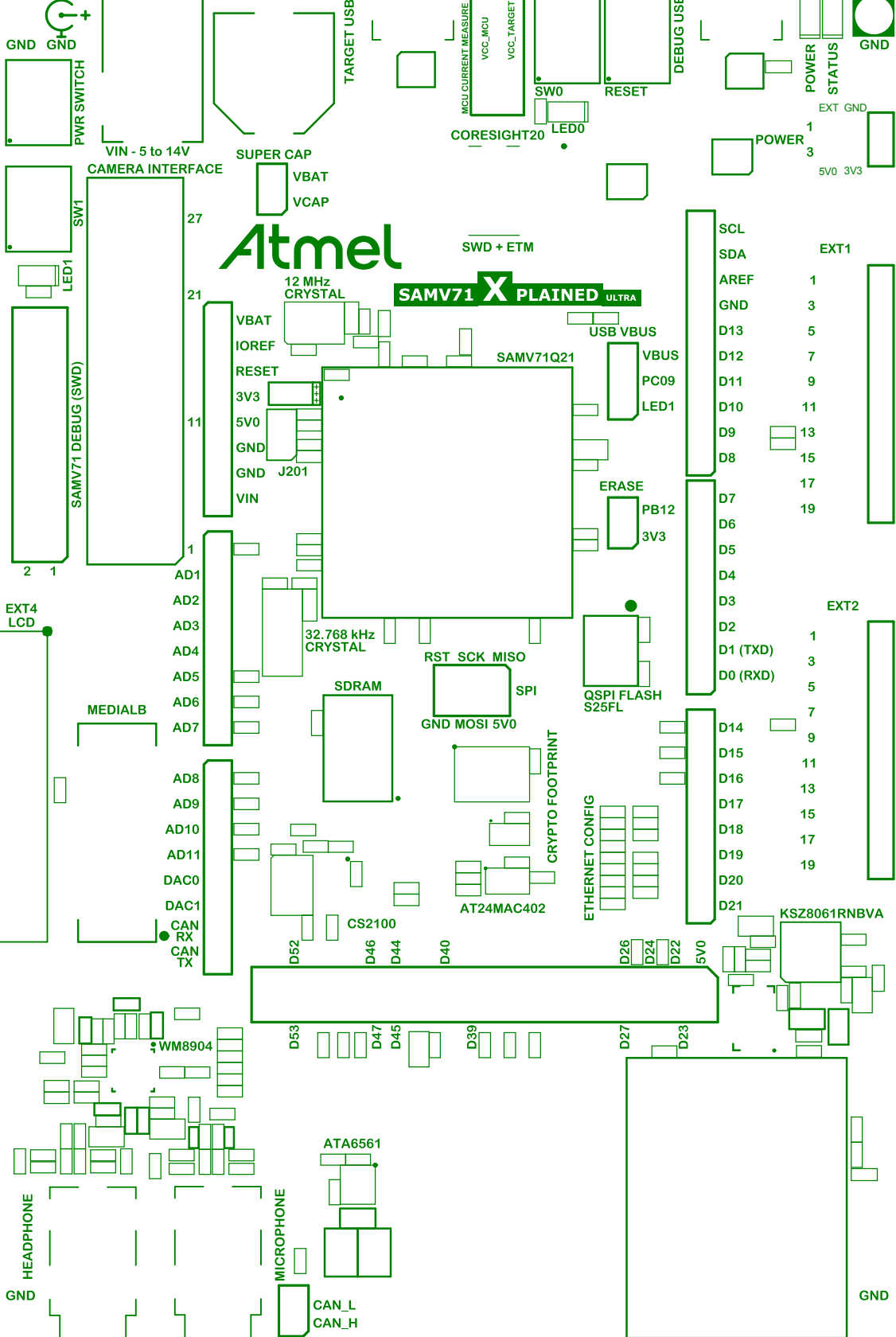
PCBA LABEL
A08-2216 Rev 3

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XPLAINED PRO
EXTENSION HEADER

GND	ID
ADC-	ADC+
GPIO1	GPIO0
PWM-	PWM+
SPI_SS_B	IRQ
TWI_SCL	TWI_SDA
UART_TX	UART_RX
SPI_MOSI	SPI_SS_A
SPI_SCK	SPI_MISO
VCC	GND



Atmel

SAMV71 X PLAINED ULTRA

SWD + ETM

SAMV71Q21

32.768 kHz CRYSTAL

SDRAM

RST SCK MISO
SPI
GND MOSI 5V0

QSPI FLASH
S25FL

CRYPTO FOOTPRINT

AT24MAC402

CS2100

KSZ8061RNBVA

WM8904

ATA6561

CAN_L
CAN_H

SCL
SDA
AREF
GND
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1 (TXD)
D0 (RXD)

EXT1
1
3
5
7
9
11
13
15
17
19

EXT2
1
3
5
7
9
11
13
15
17
19

POWER
1
3
5V0 3V3

EXT GND

POWER
STATUS
GND

DEBUG USB

RESET

SW0

LED0

CORESIGHT20

MCU CURRENT MEASURE
VCC_MCU
VCC_TARGET

TARGET USB

SUPER CAP
VBAT
VCAP

VIN - 5 to 14V

CAMERA INTERFACE

SW1

SAMV71 DEBUG (SWD)

LED1

GND GND

PWR SWITCH

EXT4
LCD

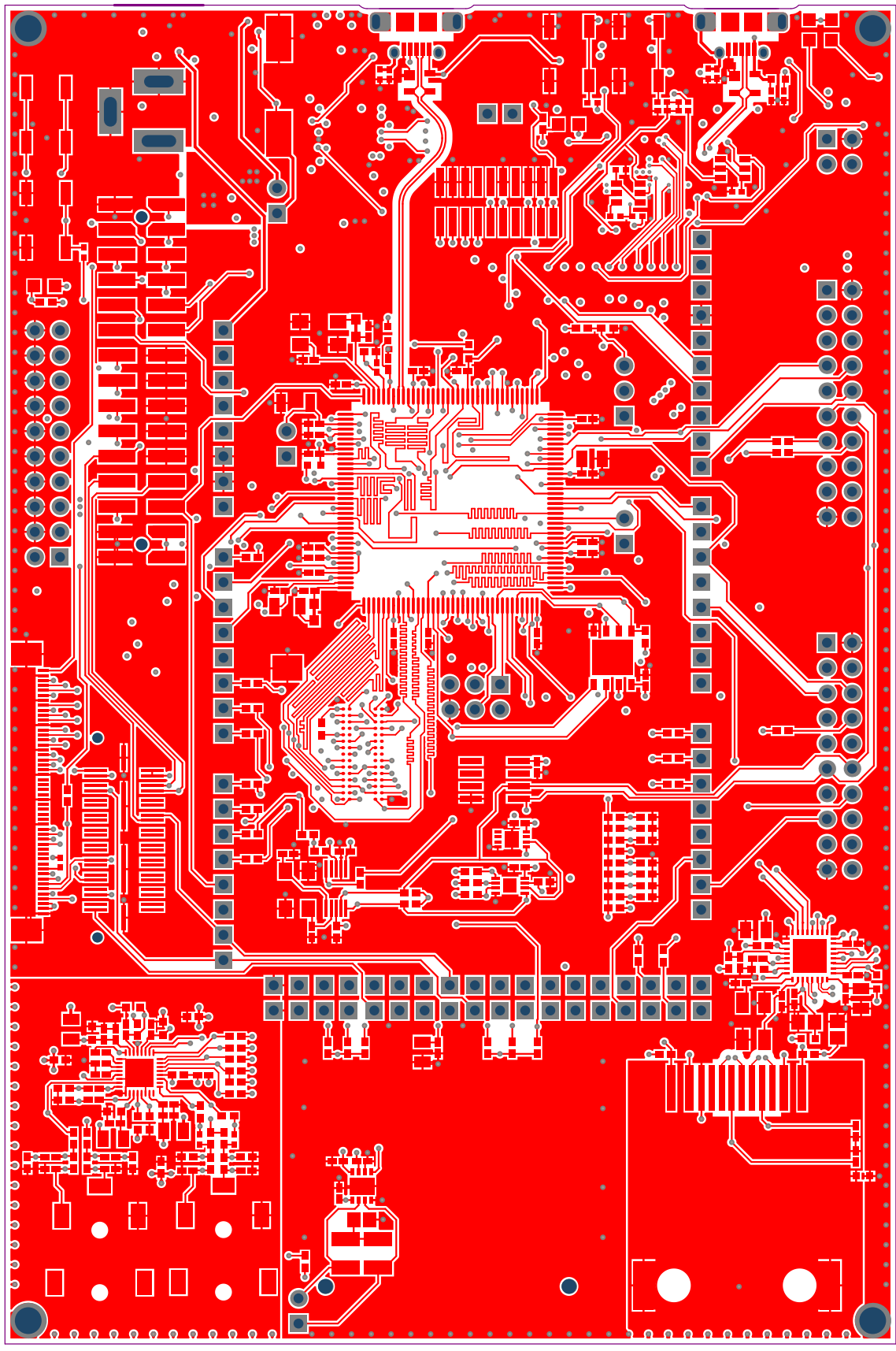
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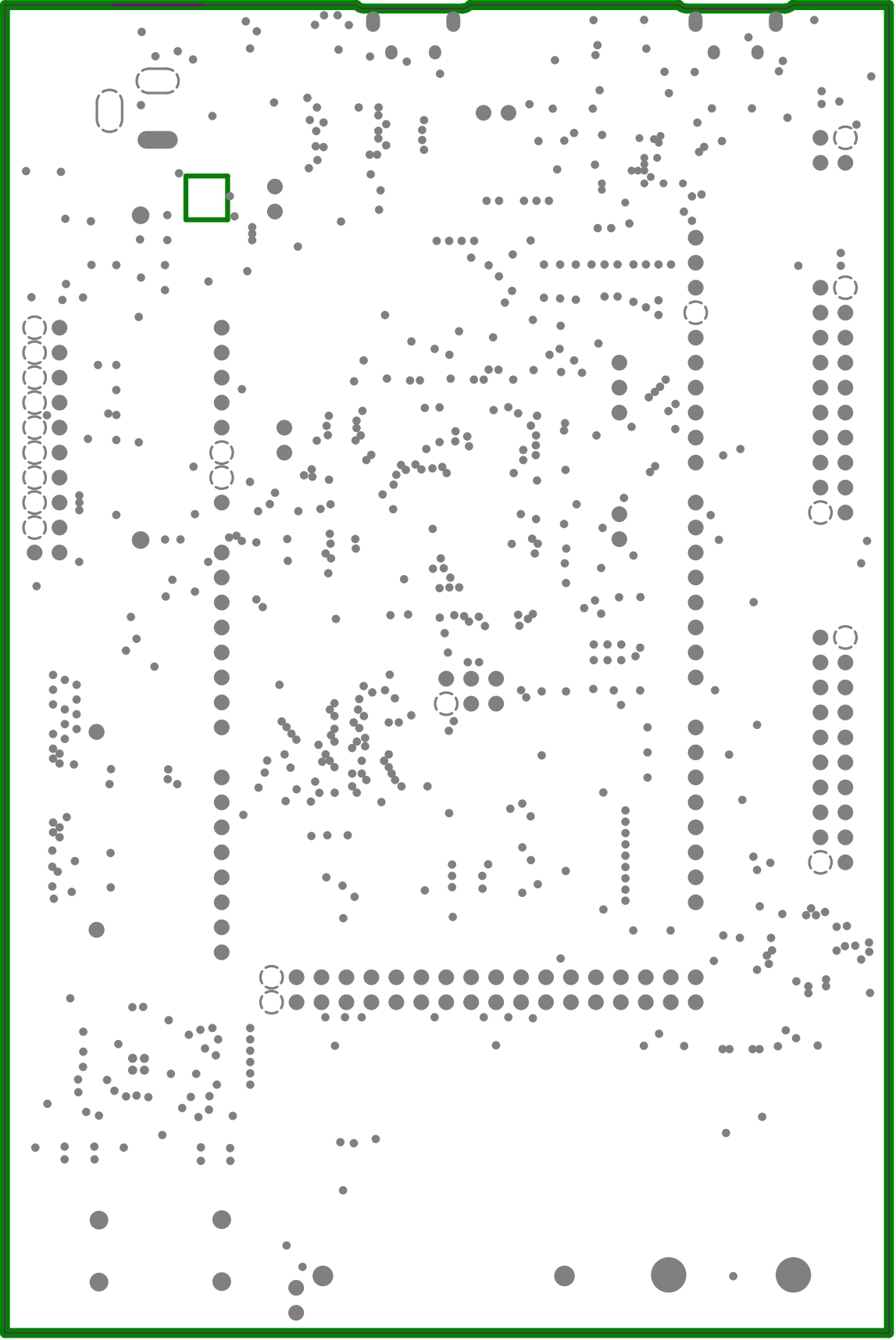
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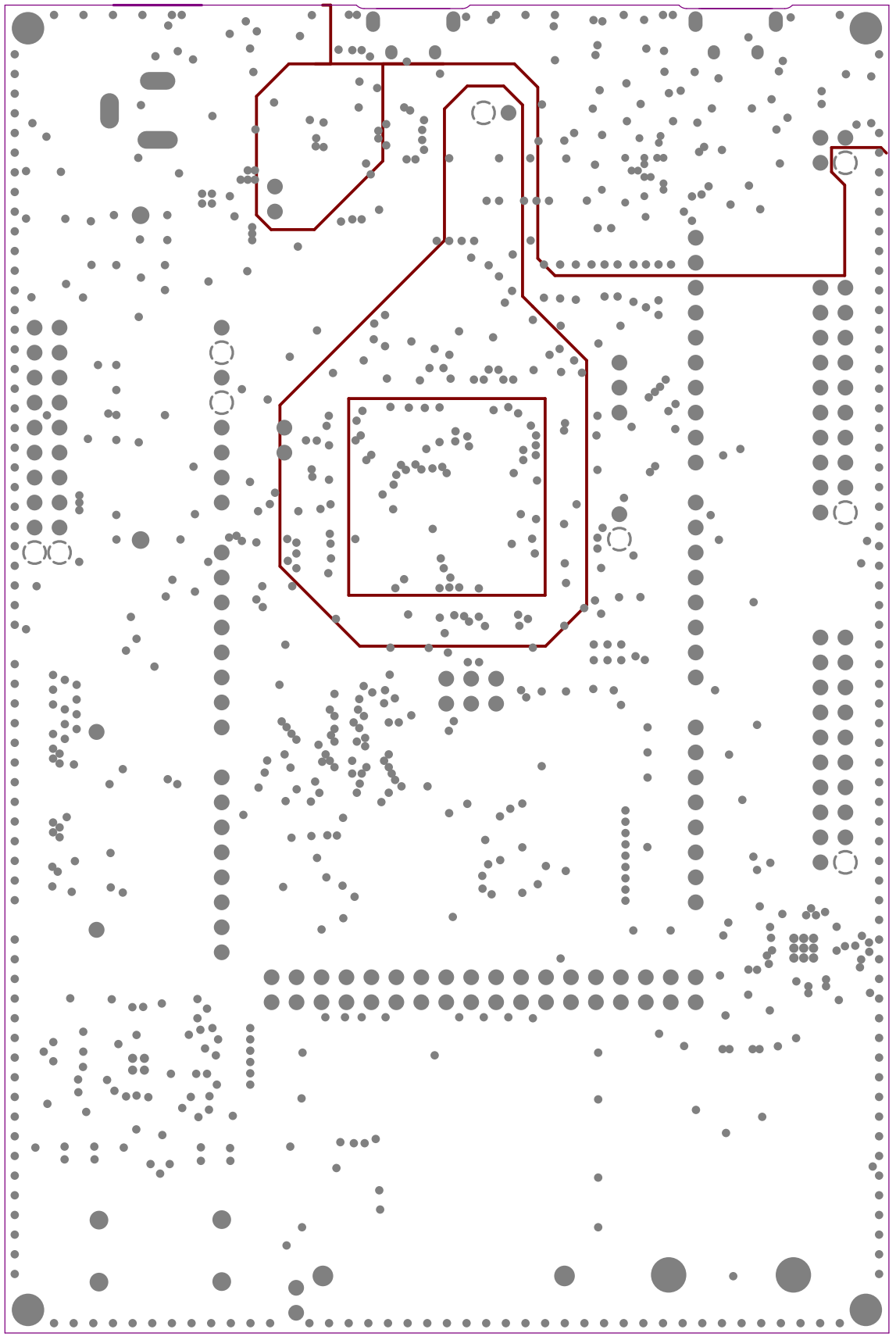
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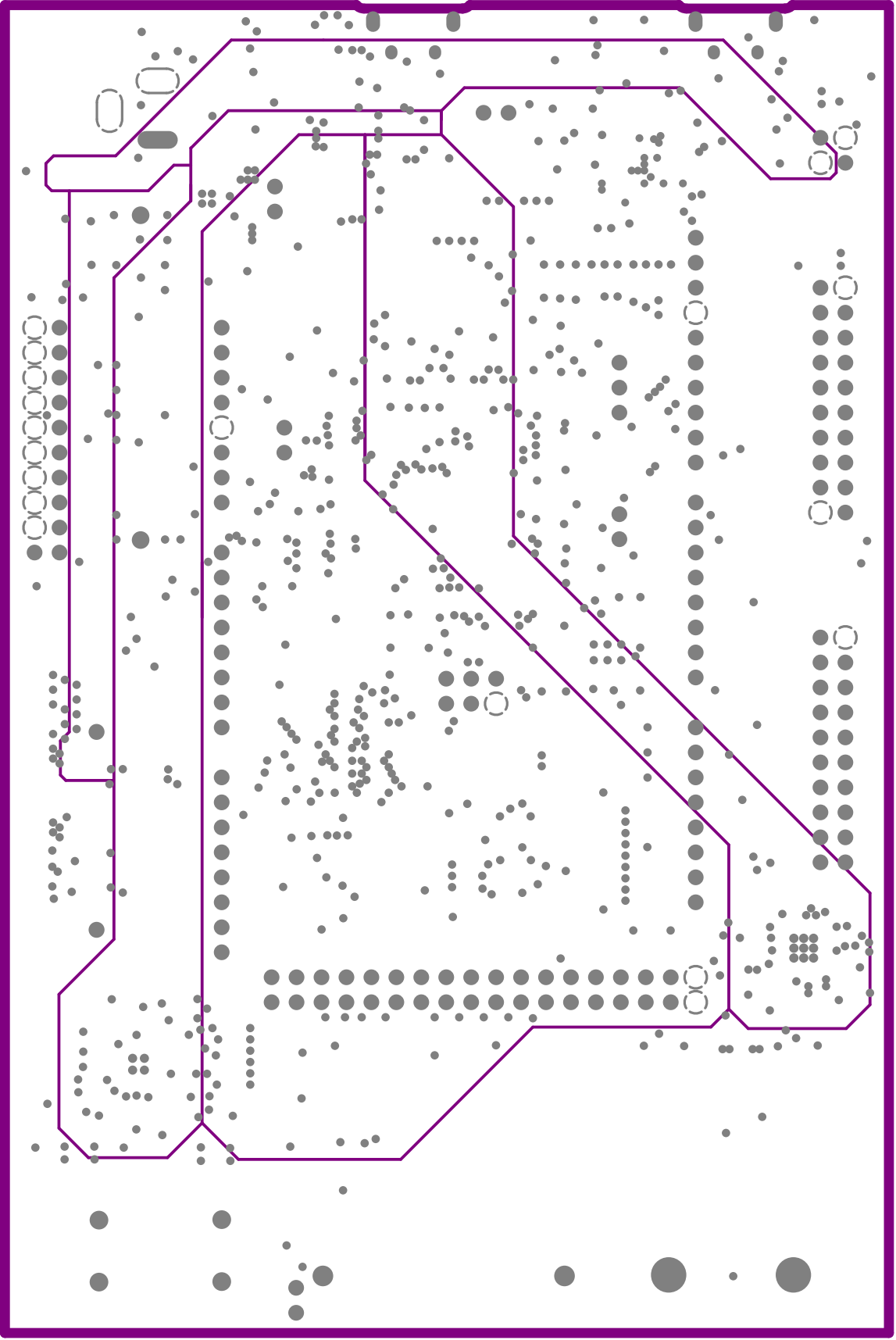
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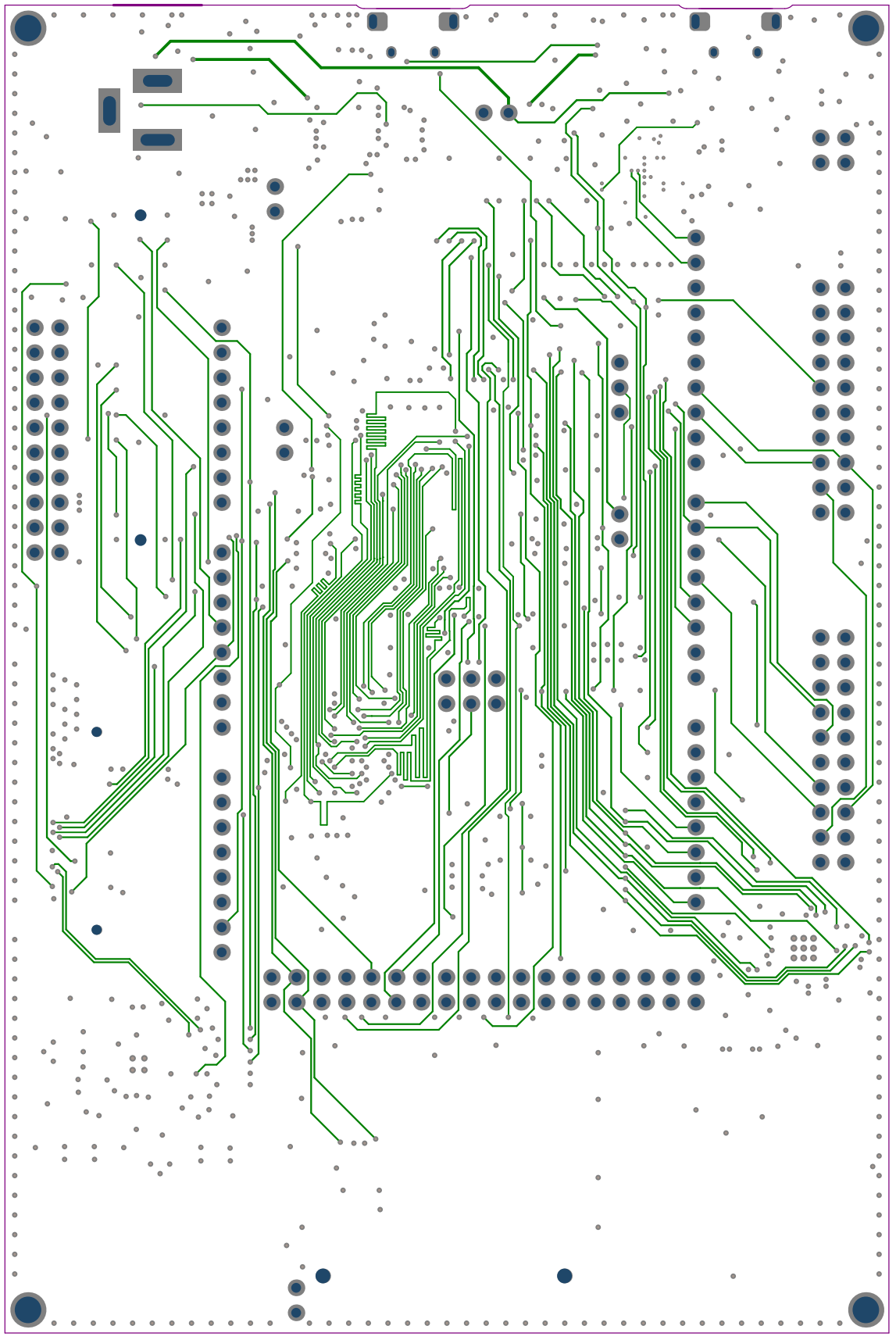
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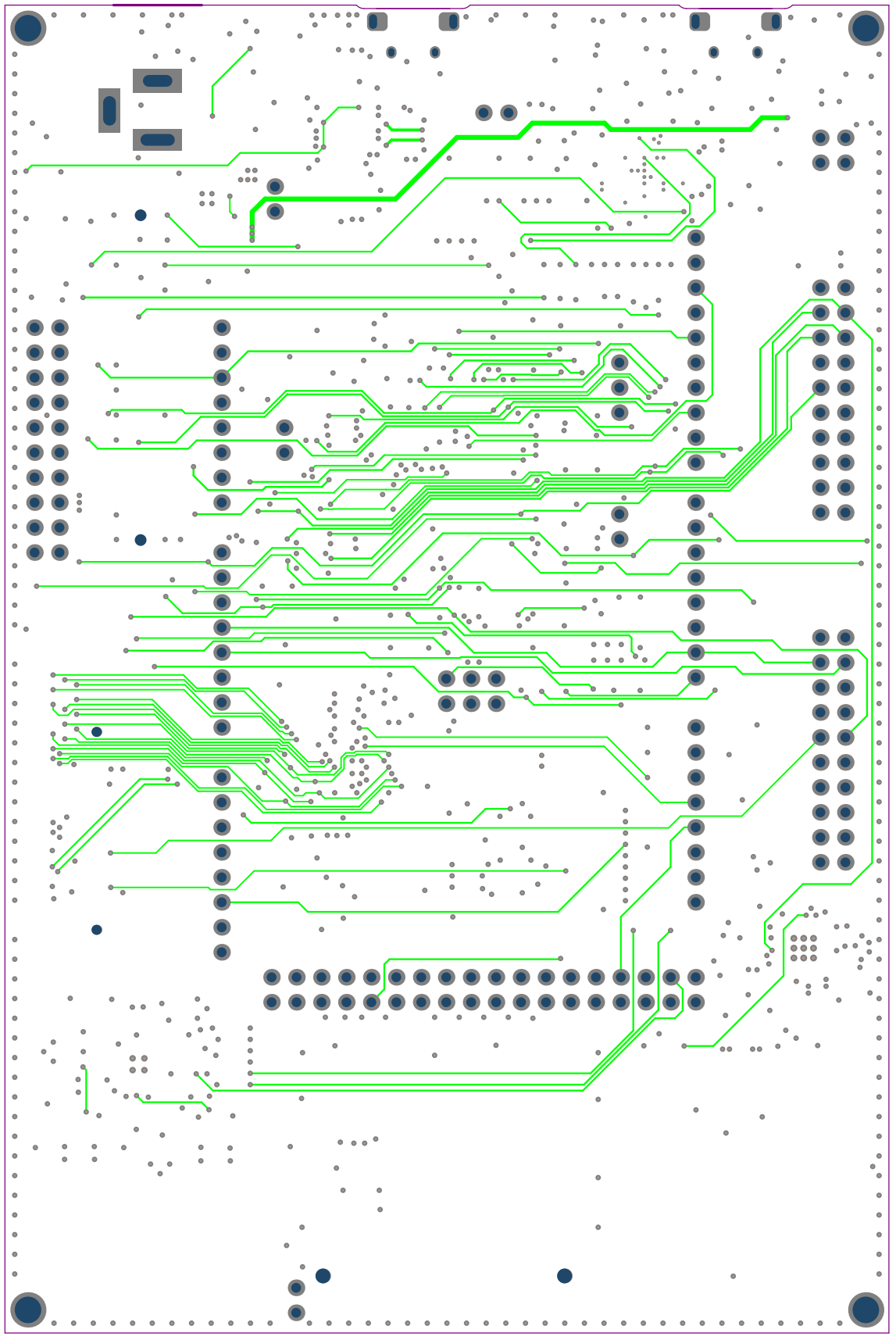


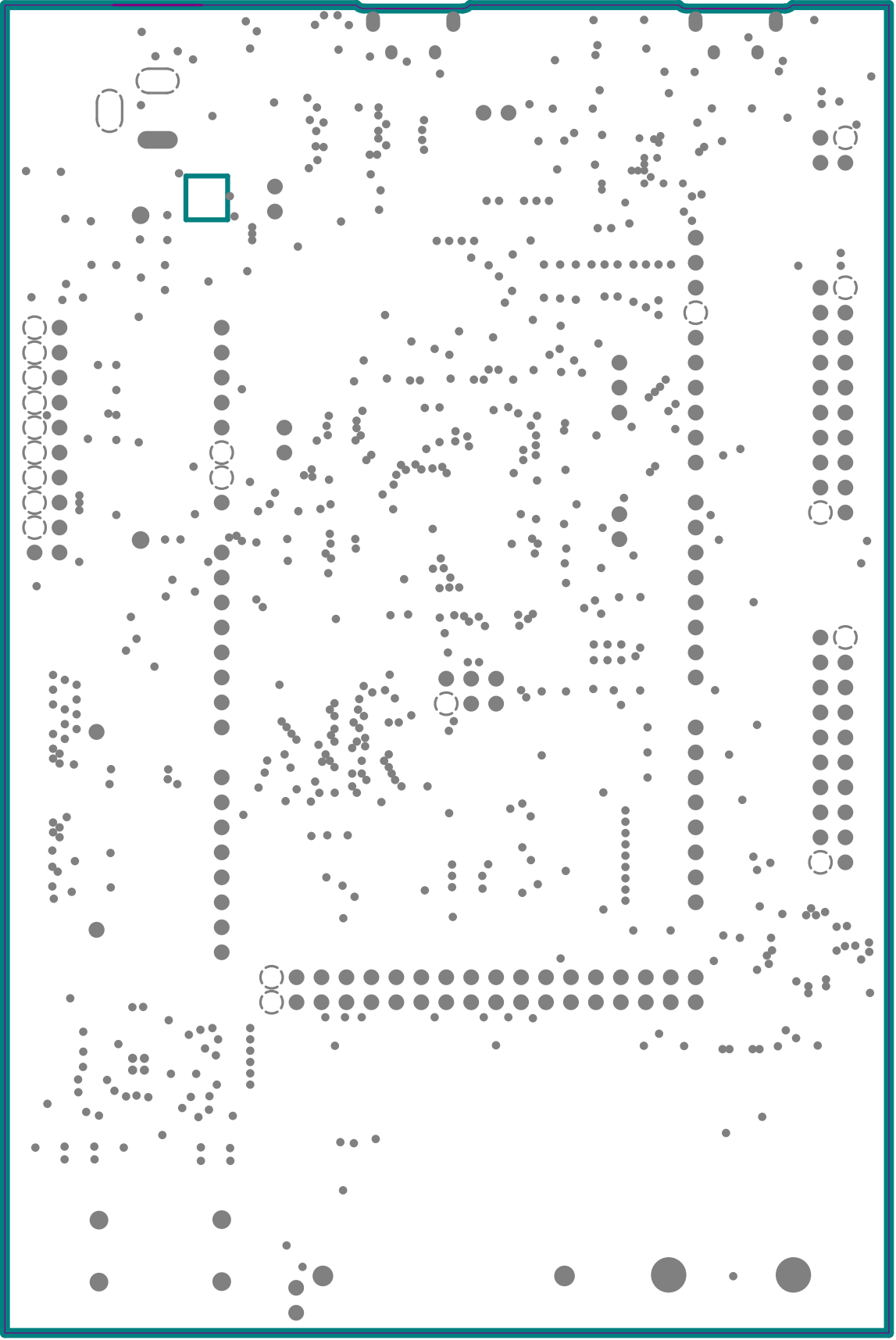


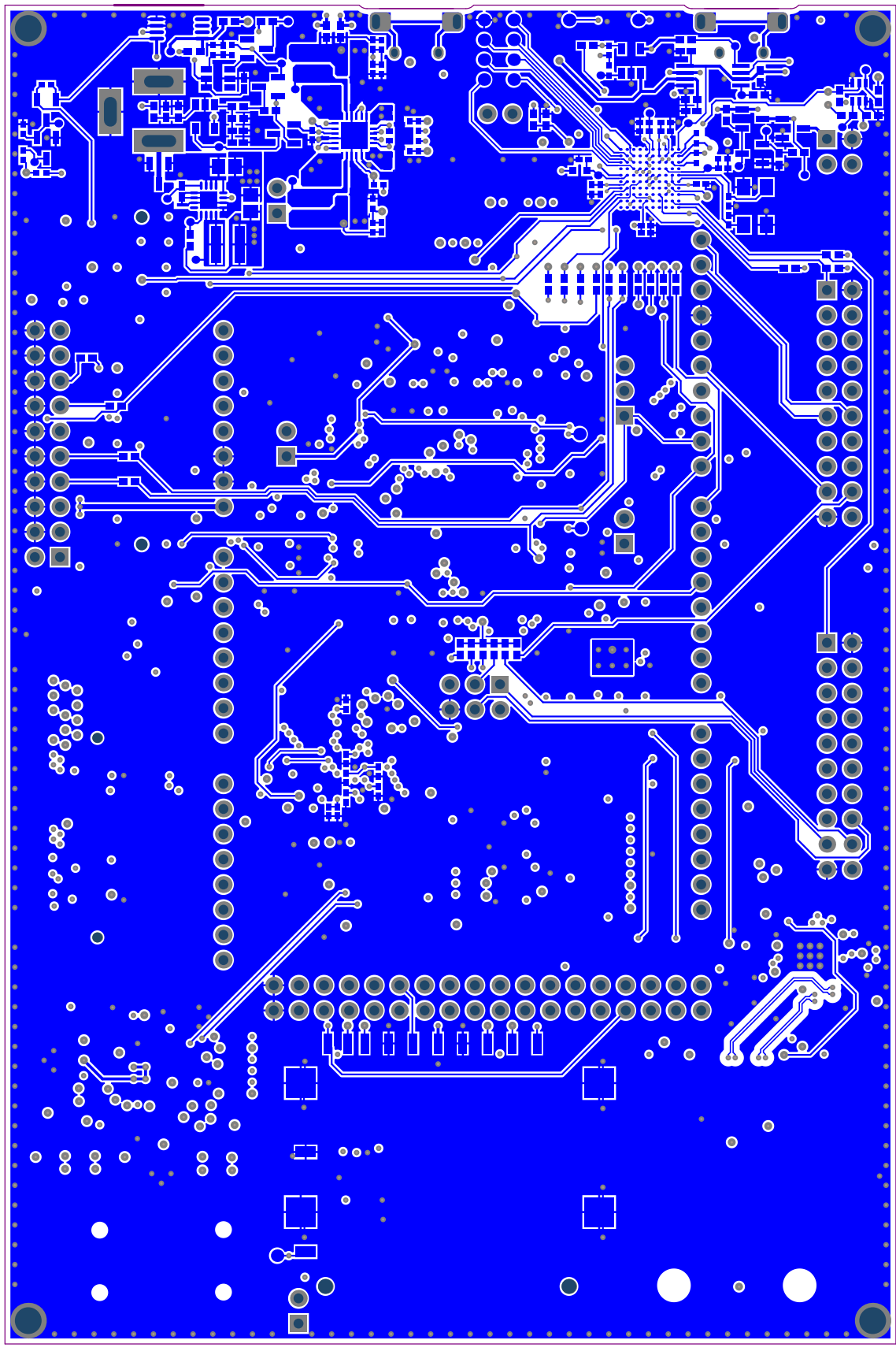












Top Level Schematics

Report Date: 24.08.2016
Print Date: 24.08.2016

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16:05:24



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Approved		Notes