LPS331AP

MEMS pressure sensor
260-1260 mbar absolute digital output barometer

Target specification

Features

- Piezoresistive pressure sensor
- 260-1260 mbar absolute pressure range
- Low power consumption
- Low noise (0.02 mbar RMS)
- 20 cm resolution
- Embedded offset and span temperature compensation
- SPI and I^2C interfaces
- Supply voltage 1.8 V to 3.6 V
- High overpressure capability: 20x Full scale
- High shock survivability (10000 g)
- Small and thin package
- ECOPACK® Lead-free compliant

Applications

- Altimeter and barometer for portable devices
- GPS applications
- Weather station equipment
- Sport watches

Description

The LPS331AP is an ultra compact absolute piezoresistive pressure sensor. It includes a monolithic sensing element and an IC interface able to take the information from the sensing element and to provide a digital signal to the external world.

HCLGA-16 3x3x1.2 mm

The sensing element consists of a suspended membrane realized inside a single mono-silicon substrate. It is capable to detecting pressure and is manufactured using a dedicated process developed by ST, called *VENSENS*.

The *VENSENS* process allows to build a mono-silicon membrane above an air cavity with controlled gap and defined pressure.
The membrane is very small compared to the traditionally built silicon micromachined membranes. Membrane breakage is prevented by intrinsic mechanical stoppers.

The IC interface is manufactured using a standard CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

LPS331AP is available in a small plastic land grid array (HCLGA) package and it is guaranteed to operate over a temperature range extending from -20 °C to +85 °C. The package is holed to allow external pressure to reach the sensing element.

The LPS331AP belongs to a family of products suitable for a variety of applications.

Table 1. Device summary

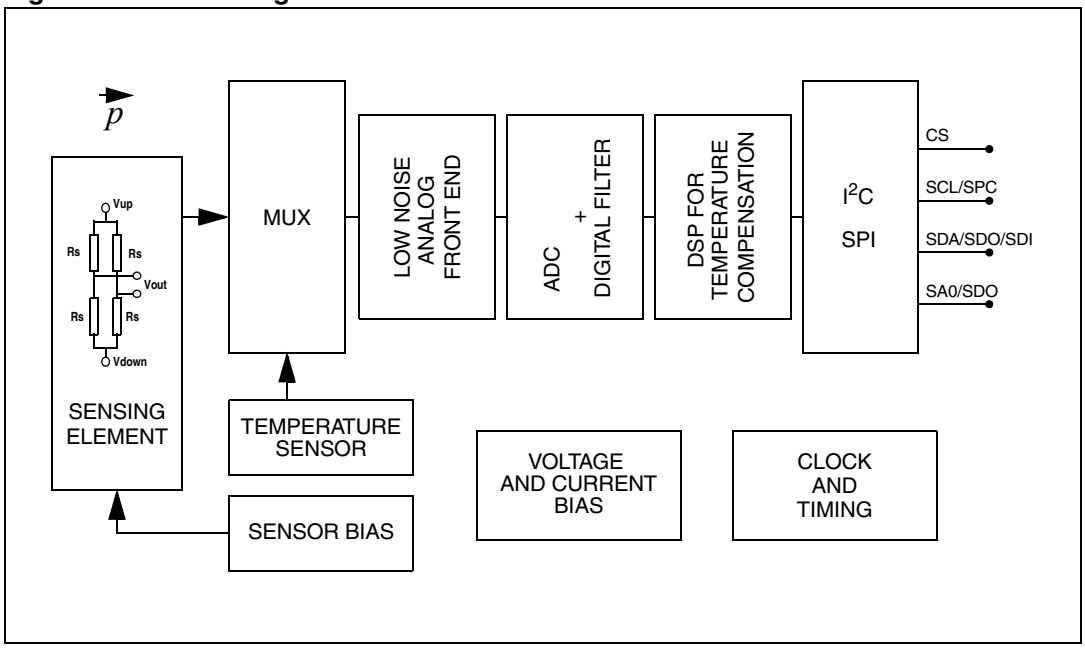
Part number	Temperature range [°C]	Package	Packing
LPS331AP	-20 to +105	HCLGA-16	Tray
LPS331APTR			Tape and reel

Contents

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection

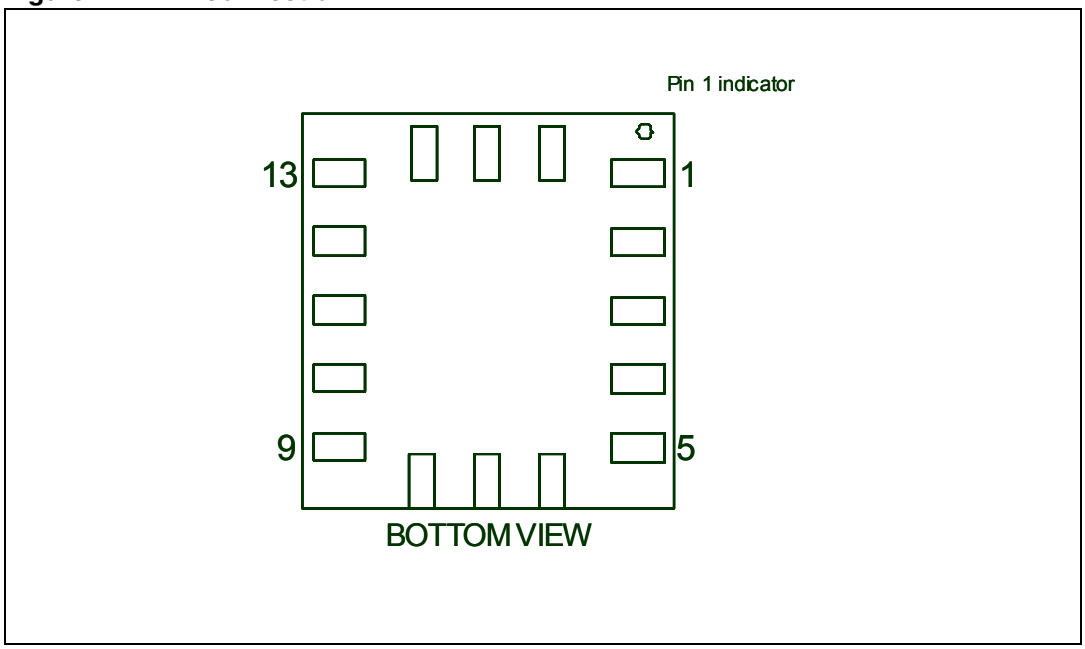


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	NC	Not connected
3	NC	Not connected
4	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
5	GND	0V supply
6	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
7	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
8	CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
9	INT1	Interrupt 1 (or data ready)
10	Reserved	Connect to GND
11	INT2	Interrupt 2 (or data ready)
12	GND	0 V supply
13	GND	0 V supply
14	Vdd	Power supply
15	Reserved	Connect to Vdd
16	GND	0 V supply

2 Mechanical and electrical specifications

Conditions @ Vdd = 2.5 V, T = 25 °C, unless otherwise noted.

2.1 Mechanical characteristics

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Top	Operating temperature range		-20		105	°C
Tfull	Full accuracy temperature range		5		70	°C
Pop	Operating pressure range		260		1260	mbar
Pbits	Pressure output data			24		bits
Pres(2)	Pressure resolution			0.01		mbar/LSB
Paccrel	Relative accuracy pressure	P=260 to 1260 mbar T= 25°C		+/-0.1		mbar
Pacc	Absolute accuracy pressure	P = 260 to 1260 mbar T = +5 ~ +70 °C		+/-5		mbar
Pnoise	Pressure noise		See *Table 15.*			mbar RMS
Tbits	Temperature output data			16		bits
Tres	Temperature Resolution			0.01		°C
Tnoise	Temperature Noise		See *Table 16.*			
Tacc	Absolute accuracy temperature @3.3V	T= +5~+70		+/-2		°C

1. Typical specifications are not guaranteed
2. Parameter given as standard deviation value

2.2 Electrical characteristics

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.8		3.6	V
Idd	Supply current @ ODRp 1 Hz and ODRt = 1Hz		see *Table 5*			µA
IddPdn	Supply current in power-down mode T = 25 °C			1		µA

1. Typical specifications are not guaranteed

Table 5. Supply current @ODRp 1 Hz, ODRt 1 Hz

Symbol	Noise RMS	Min	Typ	Max	Unit
Idd	0.160 mbar		6.0		µA
	0.080 mbar		8.0		
	0.040 mbar		15.0		
	0.030 mbar		25.0		
	0.020 mbar		45.0		

2.3 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin	-0.3 to Vdd +0.3	V
P	Overpressure	20	bar
T_{STG}	Storage temperature range	-40 to +125	°C


This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part


This is an ESD sensitive device, improper handling can cause permanent damage to the part

3 Functionality

The LPS331AP is a high resolution, digital output pressure sensor packaged in an HCLGA holed package. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface able to take the information from the sensing element to the external world, as a digital signal.

3.1 Sensing element

An ST proprietary process is used to obtain a mono-silicon µ-sized membrane for MEMS pressure sensors, without requiring substrate to substrate bonding.
When pressure is applied, membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances, whose output signal is converted by the IC interface.

Intrinsic mechanical stoppers prevent breakage in case of pressure overstress, ensuring measurement repeatability.

The pressure inside the buried cavity under the membrane is constant and controlled by process parameters.

To be compatible with traditional packaging technologies, a silicon holed cap is placed on top of the sensing element. During moulding phase this opening is covered by a dedicated protection to avoid membrane blocking.
The package design leaves the holed cap exposed, allowing ambient pressure to reach the sensing element.

3.2 IC interface

The complete measurement chain consists of a low-noise capacitive amplifier, which converts the resistive unbalance of the MEMS sensor into an analog voltage signal, and of an analog-to-digital converter, which translates the produced signal into a digital bitstream.

The converter is coupled with a dedicated reconstruction filter which removes the high frequency components of the quantization noise and provides low rate and high resolution digital words.

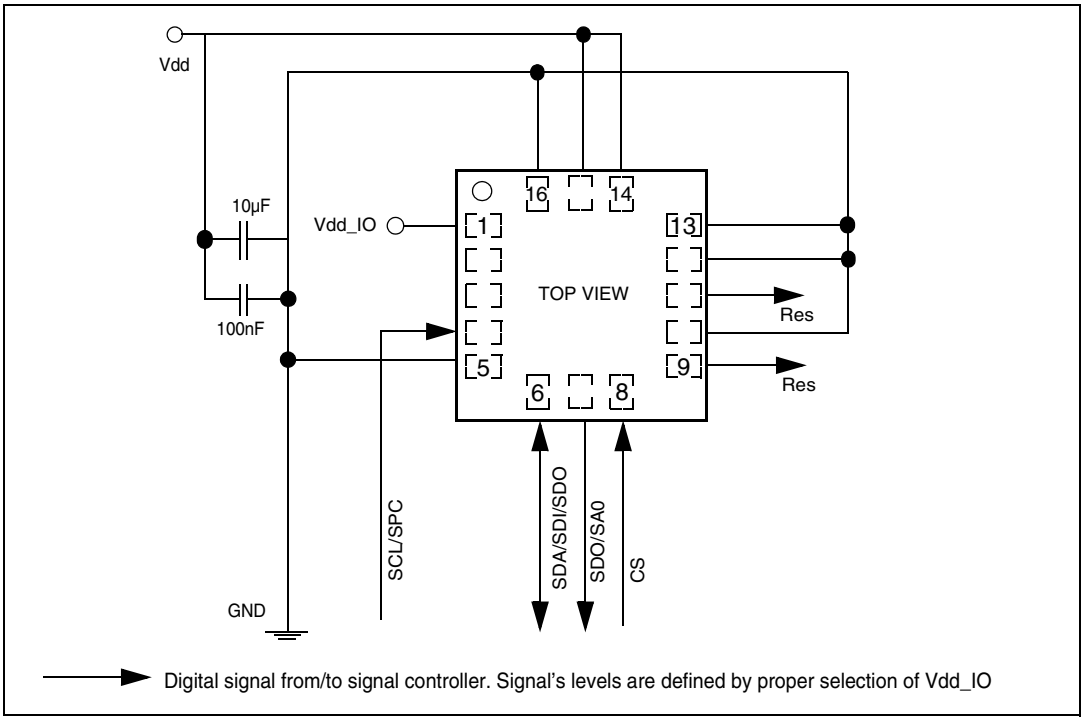
The pressure data can be accessed through an I^2C/SPI interface making the device particularly suitable for direct interfacing with a micro controller.

3.3 Factory calibration

The IC interface is factory calibrated at two temperatures and two pressures for sensitivity and accuracy.
The trimming values are stored inside the device by a non volatile structure. Any time the device is turned on, the trimming parameters are downloaded into the registers to be employed during normal operation. This allows the user to employ the device without requiring any further calibration.

4 Application hints

Figure 3. LPS331AP electrical connection



The device core is supplied through the Vdd line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to the supply pad of the device (common design practice).

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface. When using the I²C, CS must be tied high.

4.1 Soldering information

The HCLGA package is compliant with the ECOPACK® standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020C.

5 Digital interfaces

5.1 I²C serial interface

The registers embedded inside the LPS331AP may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, CS line must be tied high (i.e. connected to Vdd_IO).

Table 7. Serial interface pin description

Pin name	Pin description
CS	SPI enable I²C/SPI mode selection (1: I²C mode; 0: SPI enabled)
SCL/ SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA/ SDI/ SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0/ SDO	I²C less significant bit of the device address (SA0) SPI serial data output (SDO)

5.2 I²C serial interface

The LPS331AP I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in the table *Table 8.*

Table 8. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the Serial DAta line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd_IO through a pull-up resistor embedded inside the LPS331AP. When the bus is free both the lines are high.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

5.2.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LPS331AP is 101110xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is '1' (address 1011101b), otherwise if the SA0 pad is connected to ground, the LSb value is '0' (address 1011100b). This solution permits to connect and address two different LPS331APs to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LPS331AP behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address (SUB) will be transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is '1', the SUB (register address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 9* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 9. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	101110	0	1	10111001 (B9h)
Write	101110	0	0	10111000 (B8h)
Read	101110	1	1	10111011 (BBh)
Write	101110	1	0	10111010 (BAh)

Table 10. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 11. Transfer when master is writing multiple bytes to slave:

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 12. Transfer when master is receiving (reading) one byte of data from slave:

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 13. Transfer when Master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

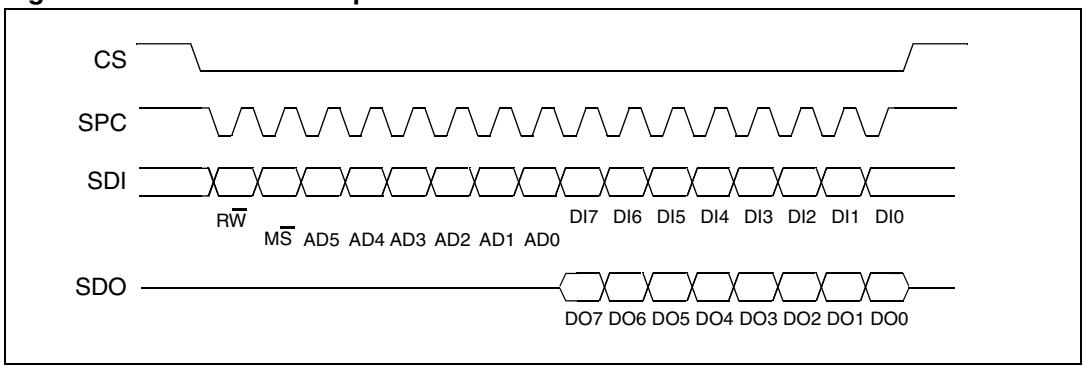
In the presented communication format MAK is Master acknowledge and NMAK is no master acknowledge.

5.3 SPI bus interface

The LPS331AP SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 4. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and

SDO are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

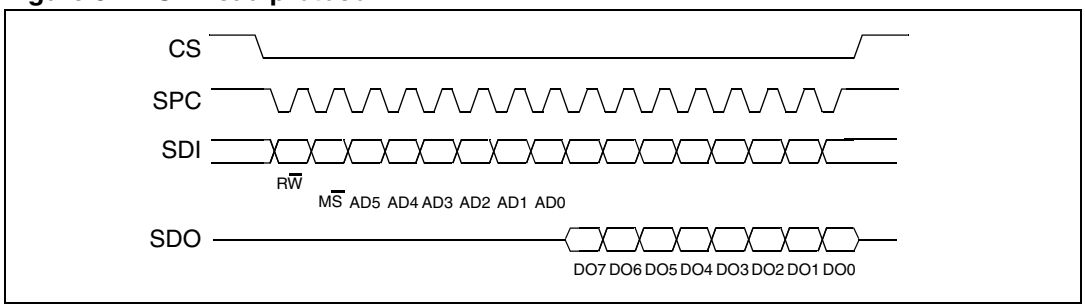
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is 0 the address used to read/write data remains the same for every block. When M$\overline{S}$ bit is 1 the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.3.1 SPI read

Figure 5. SPI read protocol



The SPI Read command is performed with 16 clock pulses. The multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

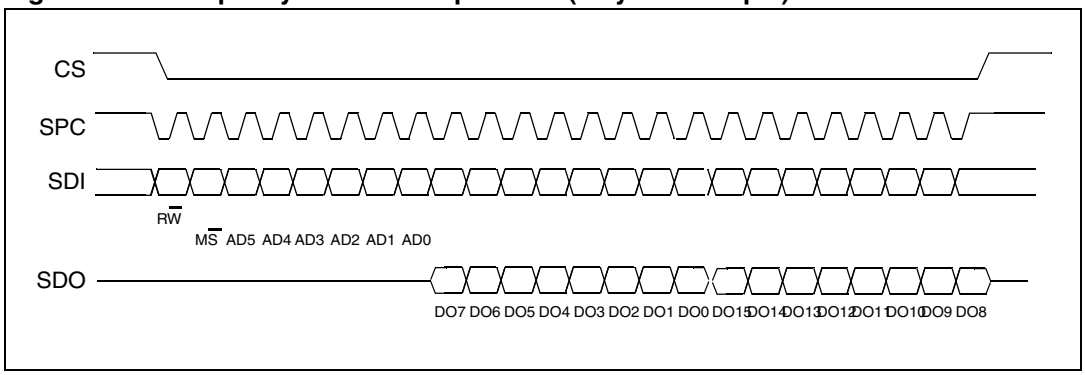
bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

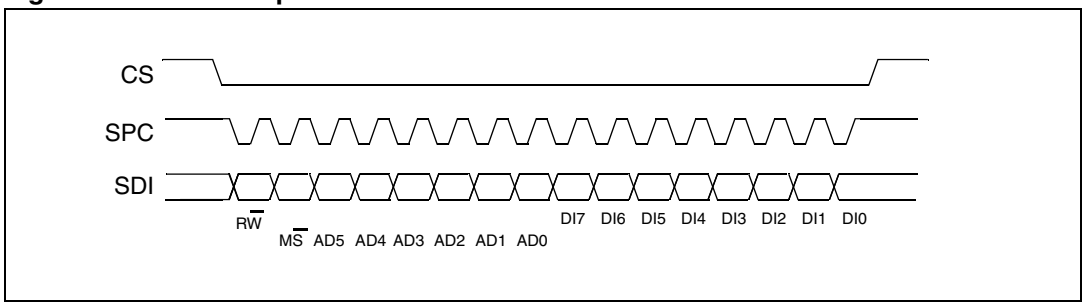
bit 16-... : data DO(...-8). Further data in multiple byte readings.

Figure 6. Multiple bytes SPI read protocol (2 bytes example)



5.3.2 SPI write

Figure 7. SPI write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

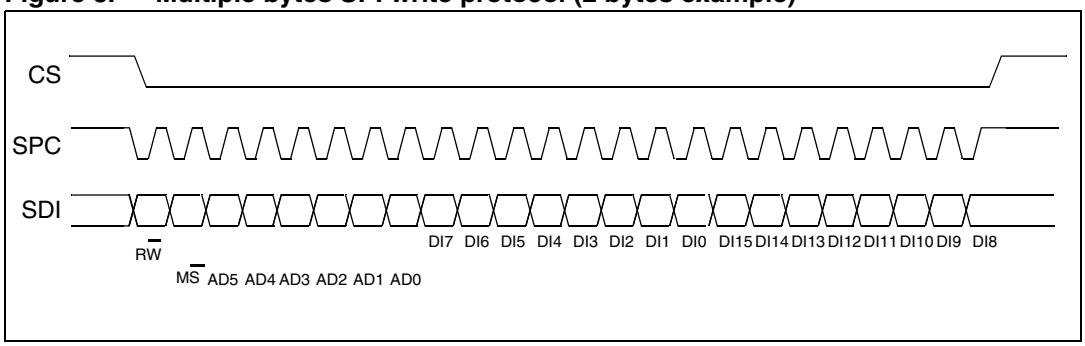
bit 1: MS bit. When 0 do not increment the address, when 1 increment the address in multiple writings.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writings.

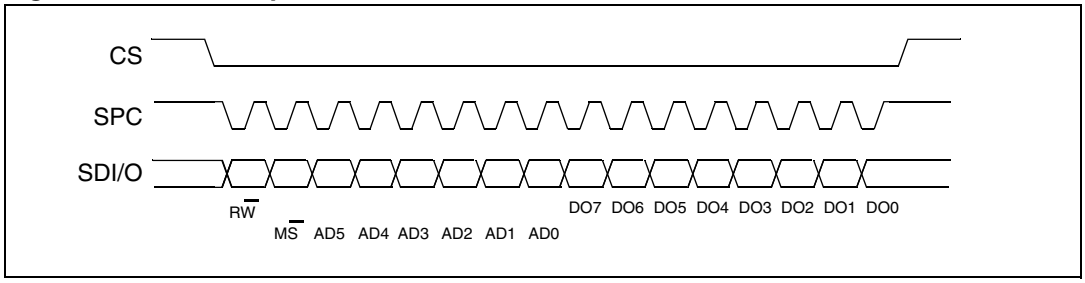
Figure 8. Multiple bytes SPI write protocol (2 bytes example)



5.3.3 SPI read in 3-wires mode

3-wires mode is entered by setting to '1' bit SIM (SPI serial interface mode selection) in CTRL_REG4.

Figure 9. SPI read protocol in 3-wires mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0, do not increment the address, when 1, increment the address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

6 Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses

Table 14. Registers address map

Name	Type	Register Address		Default	Comment
		Hex	Binary		
Reserved (Do not modify)		00-0E			Reserved
REF_P_XL	rw	08	00 1000	00000000	
REF_P_L	rw	09	0001001	00000000	
REF_P_H	rw	0A	0001010	00000000	
WHO_AM_I	r	0F	0001111	10111011	Dummy register
P_RES	rw	10	0010000	00000000	
Reserved (Do not modify)		11-1F			Reserved
CTRL_REG1	rw	20	010 0000	00000000	
CTRL_REG2	rw	21	010 0001	00000000	
CTRL_REG3	rw	22	010 0010	00000000	
INT_CFG_REG	rw	23	0100011	00000000	
INT_SOURCE_REG	rw	24	0100100	00000000	
THS_P_LOW_REG	rw	25	0100101	0000000	
THS_P_HIGH_REG	rw	26	0100110	0000000	
STATUS_REG	r	27	010 0111	00000000	
PRESS_POUT_XL_REH	r	28	010 1000	output	
PRESS_OUT_L	r	29	010 1001	output	
PRESS_OUT_H	r	2A	010 1010	output	
TEMP_OUT_L	r	2B	010 1011	output	
TEMP_OUT_H	r	2C	010 1100	output	
Reserved (Do not modify)		2D-2F			Reserved

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The registers address, made of 7 bits, is used to identify them and to read/write the data through serial interface.

7.1 REF_P_XL (08h)

REFL7	REFL6	REFL5	REFL4	REFL3	REFL2	REFL1	REFL0

REFL7 - REFL0	Reference pressure LSB data. Default value: 00h.

This register contains the lower part of the reference pressure for computing of delta pressure.
Full value is REF_P_XL & REF_P_H & REF_P_L and it is represented as unsigned number.

7.2 REF_P_L (09h)

REFL15	REFL14	REFL13	REFL12	REFL11	REFL10	REFL9	REFL8

REFL15 - REFL8	Default value: 00h.

This register contains the middle part of the reference pressure for computing of delta pressure.
Full value is REF_P_H & REF_P_L and it is represented as unsigned number.

7.3 REF_P_H (0Ah)

REFL23	REFL14	REFL13	REFL12	REFL11	REFL10	REFL9	REFL16

REFL23 - REFL16	Reference pressure MSB data. Default value: 00h.

This register contains the higher part of the reference pressure for computing of delta pressure.
Full value is REF_P_XL & REF_P_H & REF_P_L and it is represented as unsigned number.

7.4 RES_MODE_CONF(10h)

RFU	AVGT2	AVGT1	AVGT0	AVGP3	AVGP2	AVGP1	AVGP0

AVGP3-AVGP0 allow to select the pressure resolution mode. AVGT2-AVGT0 allow to select the temperature resolution mode

AVGP3-AVGP0 bits can be configured as described in *Table 15*

AVGT2-AVGT0 bits can be configured as described in *Table 16*

Table 15. Pressure resolution configuration

AVGP3	AVGP2	AVGP1	AVGP0	RMS noise	Unit
0	0	0	0	0.450	mbar
0	0	0	1	0.320	
0	0	1	0	0.230	
0	0	1	1	0.160	
0	1	0	0	0.110	
0	1	0	1	0.080	
0	1	1	0	0.060	
0	1	1	1	0.040	
1	0	0	0	0.030	
1	0	0	1	0.025	
1	0	1	0	0.020	

Table 16. Temperature resolution configuration

AVGT2	AVGT1	AVGT1	RMS noise(1)	Unit
0	0	0	TBC	degC
0	0	1	TBC	
0	1	0	TBC	
0	1	1	TBC	
1	0	0	TBC	
1	0	1	TBC	
1	1	0	TBC	
1	1	1	TBC	

1. Suggested value [AVGT2:AVGT0] = ‘011’

7.5 WHO_AM_I (0Fh)

1	0	1	1	1	0	1	1

Device identification register.

This read only register contains the device identifier that, for LPS331AP, is set to BBh.

7.6 CTRL_REG1 (20h)

PD	ODR2	ODR1	ODR0	DIFF_EN	DBDU	X	SIM

PD	Power Down Control. Default value: 0 (0: power-down mode; 1: active mode)
ODR2 ODR1 ODR0	Output Data Rate selection. Default value: 00 (see *Table 17*)
DIFF_EN	Interrupt circuit Enable. Default value: 0 (0: interrupt generation disabled; 1: interrupt circuit enabled)
BDU	Block Data Update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB reading)
X	Reserved
SIM	SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

PD bit allows to turn on the device. The device is in power-down mode when PD = '0' (default value after boot). The device is active when PD is set to '1'.

ODR2- ODR1 - ODR0 bits allow to change the output data rates of pressure and temperature samples. The default value is "000" which corresponds to "one shot configuration" for both pressure and temperature output. ODR2, ODR1 and ODR0 bits can be configured as described in *Table 17*.

Table 17. Output Data Rate bit configurations

ODR2	ODR1	ODR0	Pressure Output Data Rate	Temperature Output Data Rate
0	0	0	one shot	one shot
0	0	1	1Hz	1Hz
0	1	0	7Hz	1Hz
0	1	1	12.5Hz	1Hz
1	0	0	25Hz	1Hz
1	0	1	7Hz	7Hz
1	1	0	12.5Hz	12.5Hz
1	1	1	25Hz	25Hz

DIFF_EN bit is used to enable the circuitry for the computing of delta pressure output, DELTA_P. In default mode (DIFF_EN = '0') this circuitry is turned off.
It is suggested to turn on the circuitry only after the configuration of REF_P_XL, REF_P_L, REF_P_H, THS_P_L and THS_P_H registers used by the circuitry.

BDU bit is used to inhibit output registers update between the reading of upper and lower register parts. In default mode (BDU = '0') the lower and upper register parts are updated continuously. If it is not sure to read faster than output data rate, it is recommended to set BDU bit to '1'. In this way, after the reading of the lower (upper) register part, the content of that output registers is not updated until the upper (lower) part is read too.
This feature avoids reading LSB and MSB related to different samples.

SIM bit selects the SPI Serial Interface Mode. When SIM is '0' (default value) the 4-wire interface mode is selected and data coming from the device are sent to pin #4 (SDO).
In 3-wire interface mode, output data are sent to pin #5 (SDI/SDO).

7.7 CTRL_REG2 (21h)

BOOT	X	X	X	X	SWRESET	AUTO_ZERO	ONE_SHOT

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
SWRESET	Software reset. Default value: 0 (0: normal mode; 1: software reset)
AUTO_ZERO	Autozero enable. Default value: 0 (0: normal mode; 1: autozero enable)
ONE_SHOT	One shot enable. Default value: 0 (0: waiting for start of conversion; 1: start for a new dataset)

BOOT bit is used to refresh the content of internal registers stored in the flash memory block. At the device power-up the content of the flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason the content of trimming registers was changed, it is sufficient to use this bit to restore correct values. When BOOT bit is set to '1' the content of internal flash is copied inside corresponding internal registers and it is used to calibrate the device. These values are factory trimmed and they are different for every device. They permit a good behavior of the device and normally they have not to be changed. At the end of the boot process the BOOT bit is set again to '0'.
BOOT bit takes effect after one ODR clock cycle.

SWRESET is the software reset bit. The device is resetted to the power on configuration if the SWRESET bit is set to '1' and BOOT is set to '1'.

AUTO_ZERO when set to '1' the actual pressure output is copied in the REF_P_H & REF_P_L & REF_P_XL and keep as reference and the PRESS_OUT_H & PRESS_OUT_L & PRESS _OUT_XL is the difference between this reference and the pressure sensor value

ONE_SHOT bit is used to start a new conversion when ODR1-ODR0 bits in CTRL_REG1 are set to "000". In this situation a single acquisition of temperature and pressure is started when ONE_SHOT bit is set to '1'. At the end of conversion new data are available in output registers, INT1 signal goes high and ONE_SHOT bit comes back to '0' by hardware.

7.8 CTRL_REG3 [Interrupt CTRL register] (22h)

INT_H_L	PP_OD	IEN2	INT2_S2	INT_S1	IEN1	INT1_S2	INT1S1

INT_H_L	Interrupt active high, low. Default value: 0 (0: active high; 1: active low)
PP_OD	Push-pull/Open Drain selection on interrupt pads. Default value: 0 (0: push-pull; 1: open drain)

IEN2	INT2 interrupt enable. Default value: 0 (0: INT2 set to GND; 1: INT2 Tri-state
INT2_S2 INT2_S1	Data signal on INT2 pad control bits. Default value: 00 (see *Table 18*.)
IEN1	INT1 interrupt enable. Default value: 0 (0: INT1 set to GND; 1: INT1 Tri-state
INT1_S2 INT1_S1	Data signal on INT1 pad control bits. Default value: 00 (see *Table 18*.)

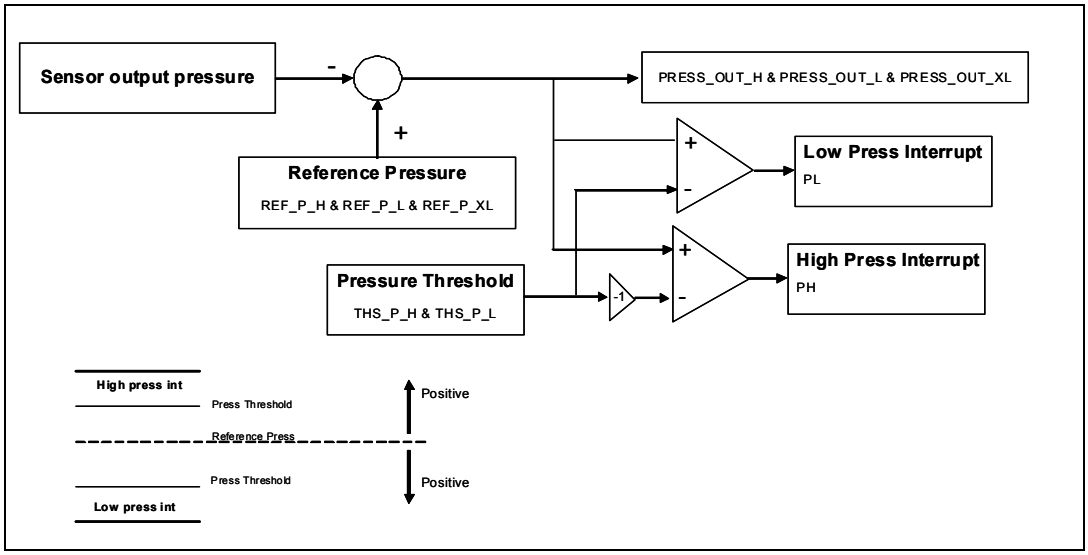
Table 18. Interrupt configurations

INT1(2)_S2	INT1(2)S1	INT1(2) Pin
0	0	Pressure Data Ready (Drdy)
0	1	Pressure High (P_high)
1	0	Pressure Low (P_low)
1	1	P_low OR P_high

The device features two fully-programmable interrupt sources (*INT1* and *INT2*) which may be configured to trigger different pressure events. *Figure 10* shows the block diagram of the interrupt generation block and output pressure data.

The device may also be configured to generate, through interrupt pins, a Data Ready signal (*Drdy*) which indicates when a new measured pressure data is available, thus simplifying data synchronization in digital systems.

Figure 10. Interrupt generation block and output pressure data.



7.9 INTERRUPT_CFG (23h)

X	X	X	X	X	LIR	PL_E	PH_E

LIR	Latch Interrupt request into INT_SOURCE register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
PL_E	Enable interrupt generation on delta pressure low event. Default value: 0. (0: disable interrupt request; 1: enable interrupt request on measured delta pressure value lower than preset threshold)
PH_E	Enable interrupt generation on delta pressure high event. Default value: 0 (0: disable interrupt request; 1:enable interrupt request on measured delta pressure value higher than preset threshold)

Interrupt configuration register.

7.10 INT_SOURCE (24h)

0	0	0	0	0	IA	PL	PH

IA	Interrupt Active. (0: no interrupt has been generated; 1: one or more interrupt event has been generated).
PL	Delta Pressure Low. (0: no interrupt has been generated; 1: Low delta pressure event has occurred).
PH	Delta Pressure High. (0: no interrupt has been generated; 1: High delta pressure event has occurred).

Interrupt source register. INT_SOURCE register is cleared by reading INT_ACK register.

7.11 THS_P_L (25h)

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

THS7 - THS0	Threshold pressure LSB. Default value: 00h.

This register contains the low part of threshold value for pressure Interrupt generation. The complete threshold value is given by THS_P_H & THS_P_L and it is expressed as unsigned number.

7.12 THS_P_H (26h)

THS15	THS14	THS13	THS12	THS11	THS10	THS9	THS8

THS15 - THS8	Threshold pressure MSB. Default value: 00h.

This register contains the high part of threshold value for pressure Interrupt generation. The complete threshold value is given by THS_P_H & THS_P_L and it is expressed as unsigned number.

7.13 STATUS_REG (27h)

0	0	P_OR	T_OR	0	0	P_DA	T_DA

P_OR	Pressure Data Overrun. Default value: 0 (0: no overrun has occurred; 1: new data for pressure has overwritten the previous one)
T_OR	Temperature Data Overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for temperature has overwritten the previous one)
P_DA	Pressure Data Available. Default value: 0 (0: new data for pressure is not yet available; 1: new data for pressure is available)
T_DA	Temperature Data Available. Default value: 0 (0: new data for temperature is not yet available; 1: new data for temperature is available)

The content of this register is updated every ODR cycle, regardless of BDU value in CTRL_REG1.

P_DA is set to 1 whenever a new pressure sample is available. P_DA is cleared anytime PRESS_OUT_H (29h) register is read.

T_DA is set to 1 whenever a new temperature sample is available. T_DA is cleared anytime TEMP_OUT_H (2Bh) register is read.

P_OR bit is set to '1' whenever new pressure data is available and P_DA was set in the previous ODR cycle and not cleared. P_OR is cleared anytime PRESS_OUT_H (29h) register is read.

T_OR is set to ‘1’ whenever new temperature data is available and T_DA was set in the previous ODR cycle and not cleared. T_OR is cleared anytime TEMP_OUT_H (2Bh) register is read.

7.14 PRESS_OUT_XL (28h)

POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0

POUT7 - POUT0	Pressure Data LSB

7.15 PRESS_OUT_L (29h)

POUT15	POUT14	POUT13	POUT12	POUT11	POUT10	POUT9	POUT8

POUT15 - POUT8	Pressure Data

7.16 PRESS_OUT_H (2Ah)

POUT23	POUT22	POUT21	POUT20	POUT19	POUT18	POUT17	POUT16

POUT23 - POUT16	Pressure Data MSB (when BLE bit in CTRL_REG1 is set to ‘0’)

Pressure data are expressed as PRESS_OUT_H & PRESS_OUT_L & PRESS_OUT_XL in 2’s complement. Values exceeding the Operating Pressure Range (see *Table 3*) are clipped.

Pressure output data:

Pout(mbar)=760 + (PRESS_OUT_H & PRESS_OUT_L & PRESS_OUT_XL)[dec]/4096

7.17 TEMP_OUT_L (2Bh)

TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

TOUT7 - TOUT0	Temperature Data LSB (when BLE bit in CTRL_REG1 register is set to ‘0’, Little Endian)

7.18 TEMP_OUT_H (2Ch)

TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

TOUT8 - TOUT15	Temperature Data MSB (when BLE bit in CTRL_REG1 register is set to '0')

Temperature data are expressed as TEMP_OUT_H & TEMP_OUT_L as 2's complement numbers.

Temperature output data:

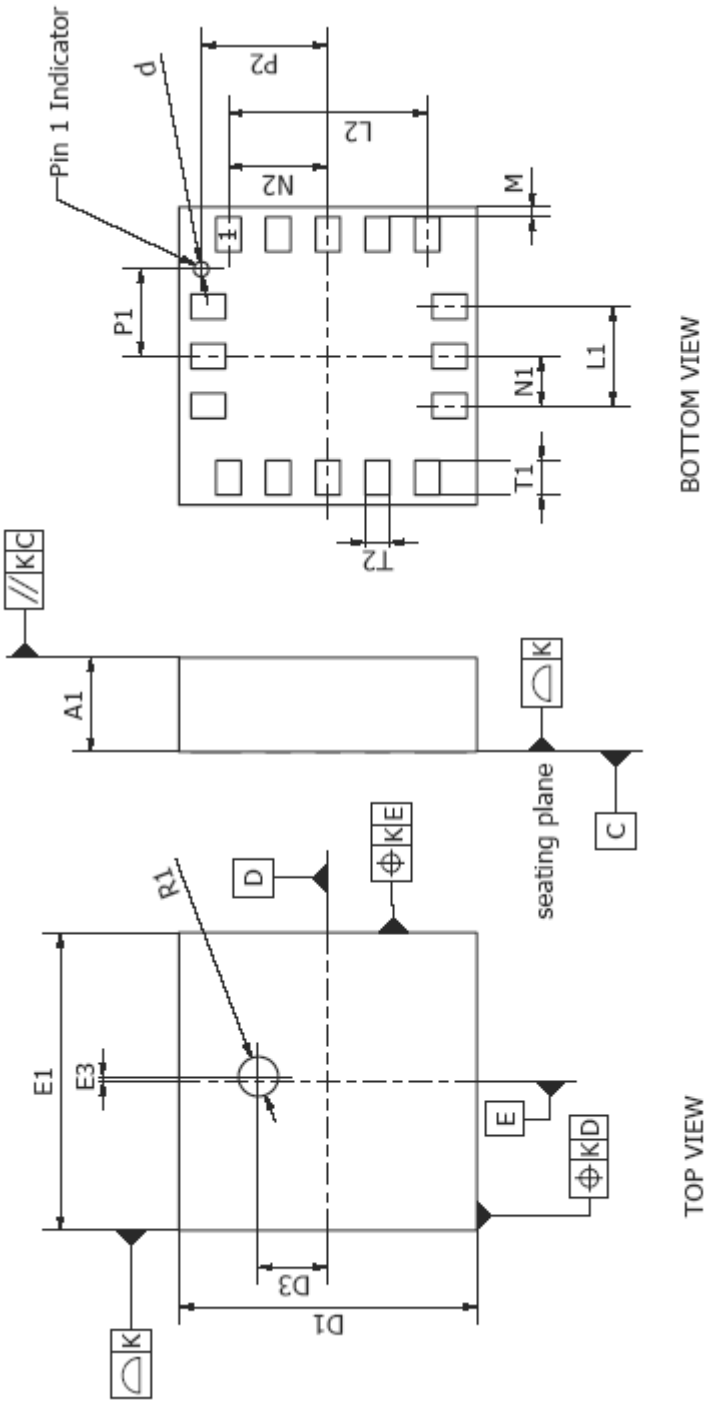
T(degC) = (Temp_OUTH & TEMP_OUT_L)[dec]/120

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 19. HCLGA 3 x 3 mm 16L mechanical data

DIMENSIONS									
	Databook (mm)			Drawing (mm)			Drawing (inches)		
Ref.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
E1	2.850	3.000	3.150	2.950	3.000	3.050	0.1161	0.1181	0.1201
E3		0			0.000	±0.10		0.0000	±0.0039
D1	2.850	3.000	3.150	2.950	3.000	3.050	0.1161	0.1181	0.1201
D3		0.700		0.660	0.7	0.740	0.0260	0.0276	0.0291
R1		0.400		0.300	0.400	0.500	0.0118	0.0157	0.0197
A1		1.200							
L1		1.000		0.960	1.000	1.040	0.0378	0.0394	0.0409
N1		0.500		0.460	0.500	0.540	0.0181	0.0197	0.0213
L2		2.000		1.960	2.000	2.040	0.0772	0.0787	0.0803
N2		1.000		0.960	1.000	1.040	0.0378	0.0394	0.0409
P1		0.875		0.835	0.875	0.915	0.0329	0.0344	0.0360
P2		1.275		1.235	1.275	1.315	0.0486	0.0502	0.0518
T1		0.350		0.310	0.350	0.390	0.0122	0.0138	0.0154
T2		0.250		0.210	0.250	0.290	0.0083	0.0098	0.0114
d		0.150		0.110	0.150	0.190	0.0043	0.0059	0.0075
K		0.050			0.050			0.0020	
M		0.100		0.060	0.100	0.140	0.0024	0.0039	0.0055


Pin 1 Indicator
d
P2
L2
N2
M
T1
P1
N1
L1
T2
BOTTOM VIEW
//KC
A1
K
seating plane
C
R1
D
KE
E1
E3
E
KD
D3
D1
K
TOP VIEW

9 Revision history

Table 20. Document revision history

Date	Revision	Changes
Dec-2010	1.0	Initial release
Dec-2010	1.1	Mistype fix
Dec-2010	1.2	ODR table update
Dec-2010	2.0	Table updating
Dec-2010	2.1	Interrupt figure update
Dec-2010	2.2	table update
Jan-2011	2.3	I2C address fixed

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