# Evaluation board with STM32H7B3LI MCU

## Introduction

The STM32H7B3I-EVAL Evaluation board is a complete demonstration and development platform for the Arm® Cortex®-M7-based STM32H7B3LIH6QU microcontroller. The STM32H7B3I-EVAL Evaluation board provides access to all the STM32 peripherals for user applications, and includes an embedded STLINK-V3E debugger/programmer.

The full range of the STM32H7B3I-EVAL hardware features helps to develop applications and evaluate all the peripherals, such as USB OTG_HS and FS, CAN FD, USART, ADC and DAC, digital microphones, SRAM, SDRAM, NOR Flash memory, Octo-SPI Flash memory with OTFDEC, microSD™ 3.0 card, 7" 800x480 WVGA TFT color RGB LCD with capacitive touch panel ($I^2C$), and DCMI camera.

The expansion connectors provide an easy way to add specialized features, while ETM trace is supported through external probes.

**Figure 1. STM32H7B3I-EVAL Evaluation board (top view)**


*Picture is not contractual.*

# 1 Features

- STM32H7B3LIH6QU Arm® Cortex® microcontroller with 2 Mbytes of Flash memory and 1.4 Mbytes of RAM in TFBGA225 package
- 7" 800x480 WVGA TFT color LCD module with RGB parallel interface and capacitive touch panel with $I^2C$ interface
- 1/4" color CMOS QSXGA (5 Mpixels) camera module with DCMI and $I^2C$ interface
- USB OTG_HS and USB OTG_FS
- On-board current measurement
- $I^2S$ / SAI audio codec
- 512-Mbit Octo-SPI NOR Flash, 8 Mx32bit SDRAM, 1 Mx16bit SRAM, and 8 Mx16bit NOR Flash
- 4 color user LEDs
- Reset, Wake Up and Tamper push-buttons
- 4-direction joystick with a selection button
- Potentiometer
- Coin-battery cell holder for power backup
- Power-metering and temperature-monitoring demonstration with 2 dual-channel, sigma-delta modulators
- Wi-Fi® module compliant with 802.11 b/g/n
- Board connectors:
  - 2 USB Micro-AB
  - 2 microSD™ cards
  - OCSPI NOR Flash module connector
  - Stereo Line OUT headset jack including analog microphone input
  - Stereo Line IN headset jack
  - 2xDB9 for external RS-232 port and CAN FD
  - JTAG and ETM trace debugger
  - Connectors for ADC and DAC
  - I/O expansion connectors
  - DFSDM microphones daughterboard expansion connector
  - Motor-control interface expansion connector
  - $I^2C$ expansion connector
- Flexible power-supply options: ST-LINK, USB $V_{BUS}$ or external sources
- On-board STLINK-V3E debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Comprehensive free software libraries and examples available with the STM32Cube MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and GCC-based IDEs

*Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.*

# 2 Ordering information

To order the STM32H7B3I-EVAL Evaluation board, refer to Table 1. For a detailed description, refer to its user manual on the product web page. Additional information is available from the datasheet and reference manual of the target STM32.

**Table 1. List of available products**

| Order code | Board references | Target STM32 |
|---|---|---|
| STM32H7B3I-EVAL | • MB1331<br>• MB1370(1)<br>• MB1379(2)<br>• MB1486(3) | STM32H7B3LIH6QU |

1. *LCD board*
2. *Camera module*
3. *Wi-Fi® module*

## 2.1 Product marking

Evaluation tools marked as “ES” or “E” are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference designs or in production.

“E” or “ES” marking examples of location:

- On the targeted STM32 that is soldered on the board (For an illustration of STM32 marking, refer to the STM32 datasheet “Package information” paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

This board features a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a "U" marking option at the end of the standard part number and is not available for sales.

In order to use the same commercial stack in his application, a developer may need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

## 2.2 Codification

The meaning of the codification is explained in Table 2. The order code is mentioned on a sticker placed on the top or bottom side of the board.

**Table 2. Codification explanation**

| STM32TTXXY-EVAL | Description | Example: STM32H7B3I-EVAL |
|---|---|---|
| STM32TT | MCU series in STM32 32-bit Arm Cortex MCUs | STM32H7 Series |
| XX | MCU product line in the series | STM32H7B3 |
| Y | STM32 Flash memory size:<br>• I for 2 Mbytes | 2 Mbytes |

# 3 Development environment

## 3.1 System requirements

- Windows® OS (7, 8 and 10), Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to Micro-B cable

*Note: macOS® is a trademark of Apple Inc. registered in the U.S. and other countries.*
*All other trademarks are the property of their respective owners.*

## 3.2 Development toolchains

- IAR Systems - IAR Embedded Workbench®(1)
- Keil® - MDK-ARM(1)
- GCC-based IDEs

1. *On Windows® only.*

## 3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 Flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

# 4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

**Table 3. ON/OFF convention**

| Convention | Definition |
|---|---|
| Jumper JPx ON | Jumper fitted |
| Jumper JPx OFF | Jumper not fitted |
| Jumper JPx [1-2] | Jumper fitted between Pin 1 and Pin 2 |
| Solder bridge SBx ON | SBx connections closed by 0 Ω resistor |
| Solder bridge SBx OFF | SBx connections left open |
| Resistor Rx ON | Resistor soldered |
| Resistor Rx OFF | Resistor not soldered |

# 5 Delivery recommendations

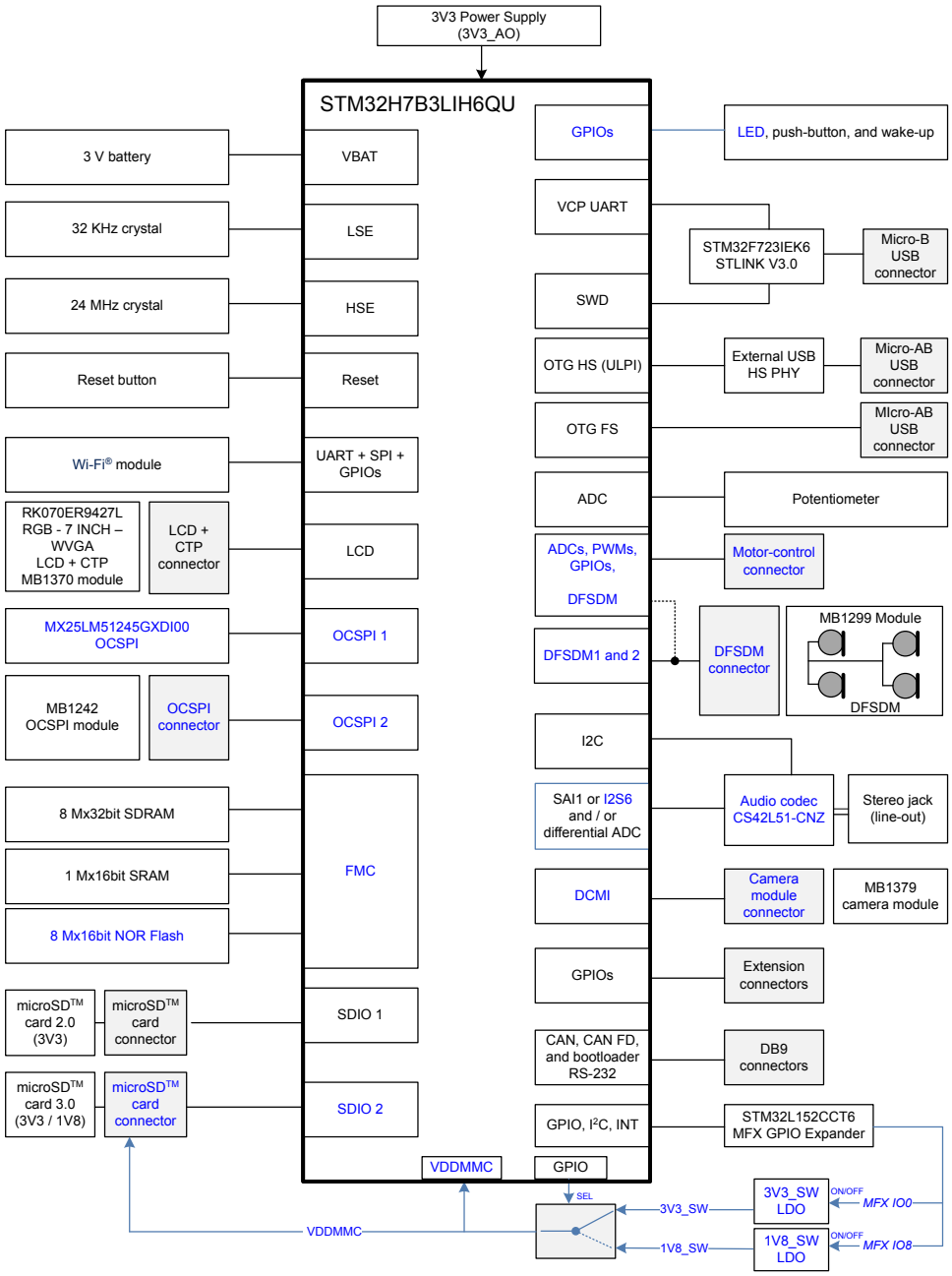
Some verifications are needed before using the board for the first time to make sure that nothing was damaged during shipment and that no components are unplugged or lost. When the board is extracted from its plastic bag, check that no component remains in the bag. Before starting the demo, take the microSD™ card from the separated ESD bag and plug it in the connector CN28, on the right side of the board.

**Warning:**
*There is an explosion risk if the battery is replaced by an incorrect one. Make sure to dispose of used batteries according to the instructions.*

# 6 Hardware layout and configuration

The STM32H7B3I-EVAL Evaluation board is designed around the STM32H7B3LIH6QU target microcontroller. Figure 2 illustrates STM32H7B3LIH6QU connections with peripheral components.

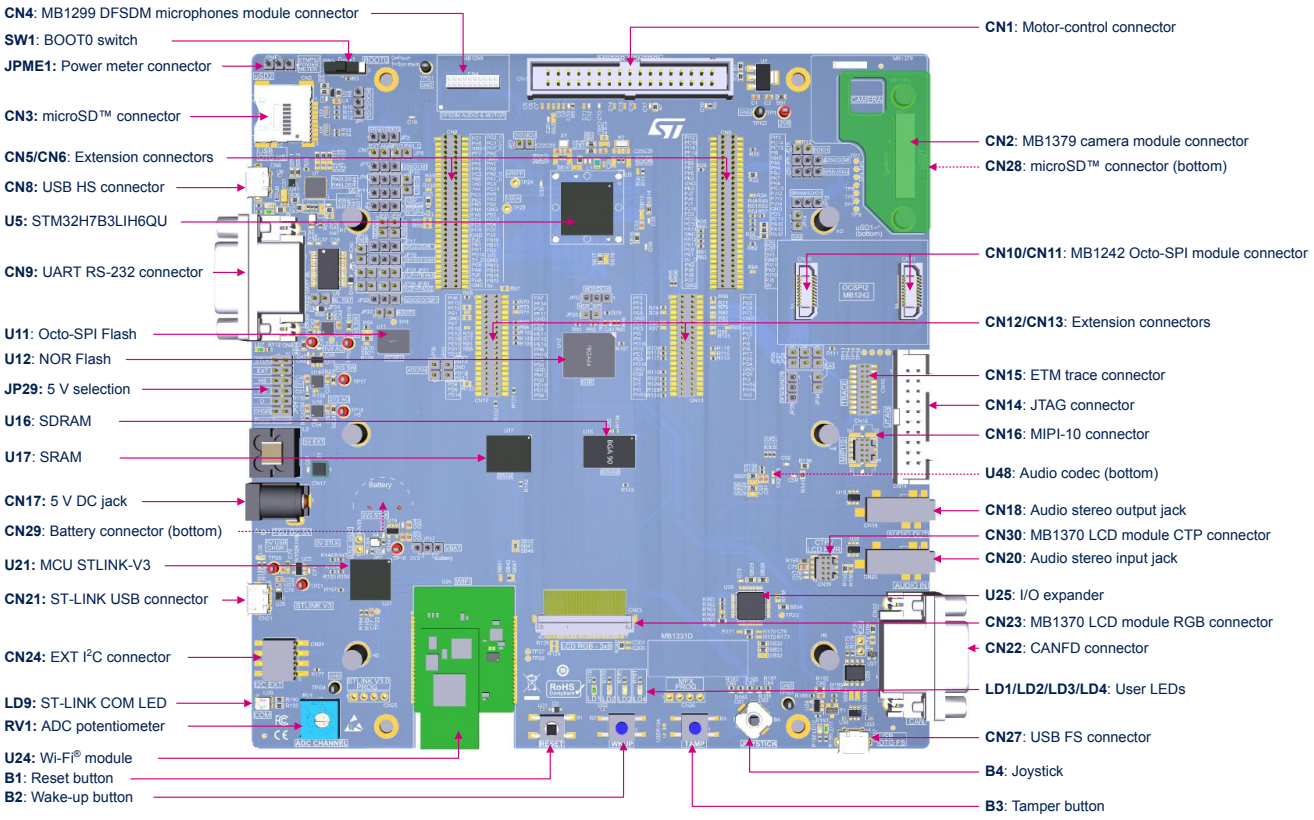
**Figure 2. Hardware block diagram**




*Note: Interfaces in blue are partially supplied by VDDMMC. Refer to Section 6.3.5 .*

Figure 3 shows the location of the main components on the top side of the Evaluation board.

**Figure 3. STM32H7B3I-EVAL Evaluation board layout**



There are two different ways to program and debug the onboard STM32 MCU:

- Using the embedded STLINK-V3E
- Using an external debug tool

## 6.1 Embedded STLINK-V3E

### 6.1.1 Description

The STLINK-V3E programming and debugging tool is integrated into the STM32H7B3I-EVAL Evaluation board.

The embedded STLINK-V3E supports:

- 5 V power supplied by the CN21 USB connector
- USB 2.0 high-speed-compatible interface
- JTAG and serial wire debugging (SWD) specific features:
  - 3 to 3.6 V application voltage on the JTAG/SWD interface and 5V tolerant inputs
  - JTAG
  - SWD and serial viewer (SWV) communication
- Direct firmware update feature (DFU) (CN25)
- MIPI10 compatible connector (CN16)
- Status COM LED (LD9) which blinks during communication with the PC
- Fault red LED (LD8) alerting on USB overcurrent request
- 5 V / 500 mA output power supply capability (U19) with current limitation
- 5 V enabled green LED (LD7)

### 6.1.2 How to use

It is very easy to use STLINK-V3E to program and debug the on-board STM32.

1. Verify that the jumper JP29 of Power Supply Sources is correctly set. Refer to Table 9.
2. Connect the board to a PC with a USB Type-A to Micro-B cable through the USB connector CN21.

*Note: For more details regarding the STLINK-V3E functionalities, refer to the STLINK-V3E user manual on the www.st.com website.*

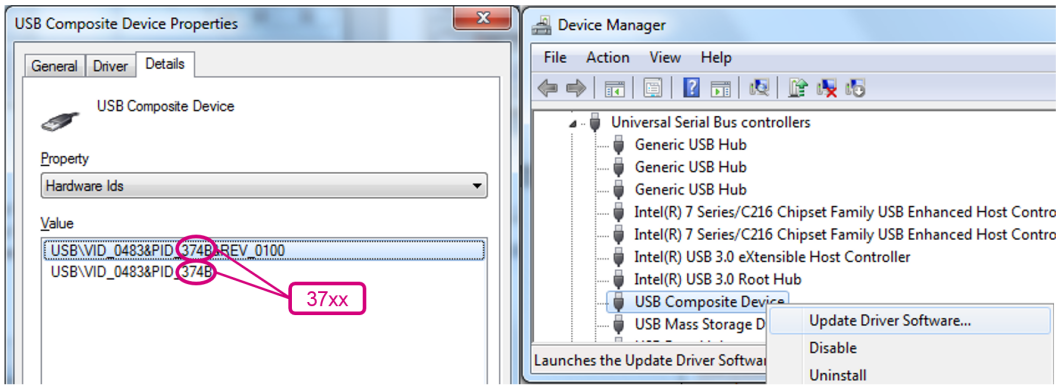
### 6.1.3 Drivers

Before connecting the STM32H7B3I-EVAL board to a Windows PC via USB, the user must install a driver for the STLINK-V3E (not required for Windows 10). It is available on the *www.st.com* website.

In case the STM32H7B3I-EVAL board is connected to the PC before the driver is installed, some STM32H7B3I-EVAL interfaces may be declared as “Unknown” in the PC device manager. In this case, the user must install the dedicated driver files, and update the driver of the connected device from the device manager as shown in Figure 4.

*Note: Prefer using the USB Composite Device handle for a full recovery.*

**Figure 4. USB composite device**




*Note: 37xx:*

- *374E for STLINK-V3E without bridges functions*
- *374F for STLINK-V3E with bridges functions*

### 6.1.4 STLINK-V3E firmware upgrade

The STLINK-V3E embeds a firmware upgrade mechanism for in-situ upgrades through the USB port. As the firmware may evolve during the lifetime of the STLINK-V3E product (For example new functionalities, bug fixes, support for new microcontroller families), it is recommended to visit the *www.st.com* website before starting to use the STM32H7B3I-EVAL Evaluation board and periodically, to stay up-to-date with the latest firmware version.

### 6.1.5 Interface

#### STLINK-V3E programming connector CN25

The connector CN21 is used only for embedded STLINK-V3E programming during board manufacturing. It is not populated by default and not for the end-user.

#### STLINK-V3E USB Type B connector CN21

The USB Micro-B connector CN21 is used to connect embedded STLINK-V3E to PC for debugging of the board.

## 6.2 External JTAG, SWD, and trace

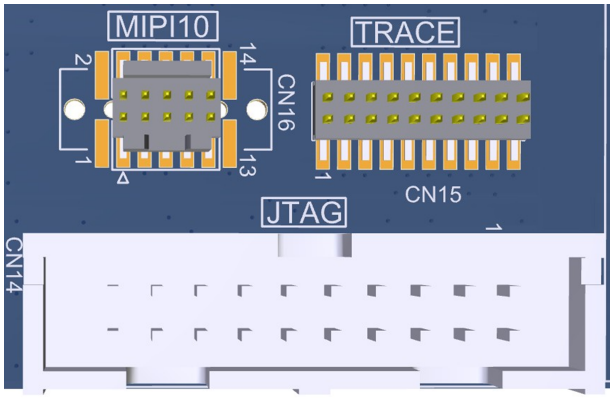
### 6.2.1 Description

There are two basics ways to support an external debug tool. If the user encounters any trouble with the first procedure, then the second one is mandatory.

1. Keep the embedded STLINK-V3E running. Power on the STLINK-V3E at first until the COM LED lights RED. Then connect the external Debug tool through connector CN14, CN15, or CN16.
2. Set the embedded STLINK-V3E in a high impedance state. When the Jumper CN19 (STLK NRST) is ON, the embedded STLINK-V3E is in RESET state and all GPIOs are in high impedance; then the user can connect his external Debug tool on the DEBUG connector CN14, CN15, or CN16 (Refer to Figure 5).

*Note: Depending on the design requirement, the embedded STLINK-V3E hardware may be completely disconnected if that is required early in the project.*

**Figure 5. External debug tools connectors**




Remarks:

- It is possible to power the board via CN21 (Embedded STLINK-V3E USB connector) even if an external tool is connected to CN15 (ETM trace connector) or CN14 (External JTAG and SWD connector).
- ETM can only work at 50 MHz clock frequency by default because ETM signals are shared with other peripherals.

### 6.2.2 Limitations and hardware configuration - ETM trace (CN15)

Limitations: Wi-Fi®, LCD, SAI, FMC A19-22 cannot be used at the same time as TRACE.
If the best performance of ETM is required (84 MHz/98 MHz), refer to Table 4. ETM trace hardware configuration.

**Table 4. ETM trace hardware configuration**

| Signal name | Pin name | Setting | JTAG / TRACE(1) |
|---|---|---|---|
| WIFI_SPI4_SCK | **PE2** | R343 | OFF(2) |
| FMC_A23 | | R342 | OFF(2) |
| TRACECLK | | R101 | **ON** |
| WIFI_SPI4_NSS | PE3 | R337 | OFF(2) |
| SAI1_SD_B | | JP34 | OFF(2) |
| FMC_A19 | | R97 | OFF(2) |
| JTAG_TDO (PB3) | | R390 | OFF(2) |
| TRACED0 | | R93 | **ON** |
| SAI1_FS_A | PE4 | JP26 | OFF(2) |
| FMC_A20 | | R88 | OFF(2) |
| JTAG_TRST (PB4) | | R372 | OFF(2) |
| DCMI_D4 | | R116 | OFF(2) |
| TRACED1 | | R340 | **ON** |
| WIFI_SPI4_MISO | PE5 | R69 | OFF(2) |
| SAI1_SCK_A | | JP28 | OFF(2) |
| FMC_A21 | | R324 | OFF(2) |
| TRACED2 | | R71 | **ON** |
| WIFI_SPI4_MOSI | PE6 | R334 | OFF(2) |
| SAI1_SD_A | | JP27 | OFF(2) |
| FMC_A22 | | R78 | OFF(2) |
| TRACED3 | | R80 | **ON** |
| RGB_LCD_G0 | PJ7 | R315 | OFF(2) |
| TRGIN | | R64 | **ON** |
| RGB_LCD_B0 | PJ12 | R259 | OFF(2) |
| TRGOUT | | R34 | **ON** |

1. *Trace configuration is in bold.*
2. *Remove to avoid stub if necessary.*

Remark:

- R69 must be removed to avoid conflict with the WIFI_SPI4_MISO output, but it is also recommended to remove R343, R337, R116, and R334 to have the best signal quality. With these changes, ETM trace 4-bits is successfully tested in DDR with the ULINK PRO up to 108MHz (CPU at 280 MHz) but the timing of the data [3:0] sampling must be adjusted on the ULINK pro: CLK: +0 ns (no change) / D [3:0]: ~ 2.5 ns.

### 6.2.3 Limitations and hardware configuration - JTAG (CN14) or MIPI10 (CN16)

Limitations: STM32H7B3LIH6QU JTAG cannot be connected at the same time to STLINK-V3E and to CN14 or CN16 connector. To be able to use JTAG on CN14 or CN16 connector, it is necessary to disconnect JTAG signals from STLINK-V3E (JTMS, JTCK, JTDO, and NRST).

- To do so, R409, R401, R399, and R398 must be removed.

### 6.2.4 Interface

**Figure 6. STDC14 / MIPI10 debugging connector CN16**

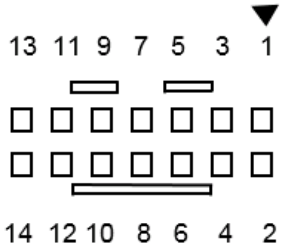



**Table 5. STDC14 / MIPI10 debugging connector CN16**

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1 (STDC14) | NC | 2 | NC (STDC14) |
| 3 (MIPI10) | +3.3V | 4 (MIPI10) | SWDIO-TMS / PA13 |
| 5 (MIPI10) | GND | 6 (MIPI10) | SWCLK-TCK / PA14 |
| 7 (MIPI10) | GND | 8 (MIPI10) | SWO-TDO / PB3 |
| 9 (MIPI10) | KEY (NC) | 10 (MIPI10) | TDI / PA15 |
| 11 (MIPI10) | GNDDetect | 12 (MIPI10) | RESET# |
| 13 (STDC14) | VCP_USART_RX / PB14 or PA2 | 14 (STDC14) | VCP_USART_TX / PB15 or PA3 |

**Table 6. STDC14 / MIPI10 debug connector CN16**

| MIPI10 pin | STDC14 pin | CN16 | Designation |
|---|---|---|---|
| - | 1 | NC | Reserved |
| - | 2 | NC | Reserved |
| 1 | 3 | T_VCC | Target VCC |
| 2 | 4 | T_SWDIO | Target SWDIO using SWD protocol or Target JTMS (T_JTMS) using JTAG protocol |
| 3 | 5 | GND | Ground |
| 4 | 6 | T_SWCLK | Target SWCLK using SWD protocol or Target JCLK (T_JCLK) using JTAG protocol |
| 5 | 7 | GND | Ground |
| 6 | 8 | T_SWO | Target SWO using SWD protocol or Target JTDO (T_JTMS) using JTAG protocol |
| 7 | 9 | KEY (NC) | KEY (NC) |
| 8 | 10 | T_JTDI | Not used by SWD protocol, Target JTDI (T_JTDI) using JTAG protocol, only for external tools |
| 9 | 11 | GNDDetect | GND detect for plug indicator, used on SWD and JTAG neither |
| 10 | 12 | T_NRST | Target NRST using SWD protocol or Target JTMS (T_JTMS) using JTAG protocol |

| MIPI10 pin | STDC14 pin | CN16 | Designation |
|---|---|---|---|
| - | 13 | T_VCP_RX | Target RX used for VCP (must be UART dedicated to Bootloader) |
| - | 14 | T_VCP_TX | Target TX used for VCP (must be UART dedicated to Bootloader) |

**Figure 7. ETM trace debugging connector CN15**

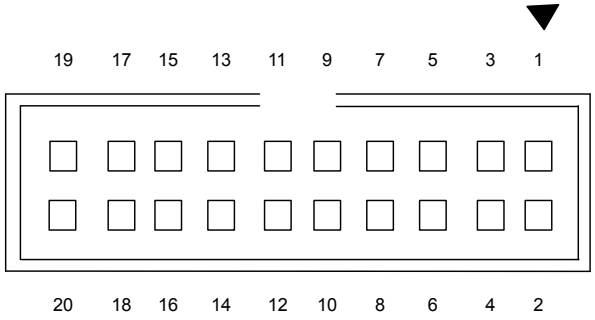



**Table 7. ETM trace debugging connector CN15**

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1 | +3.3V | 2 | TMS/PA13 |
| 3 | GND | 4 | TCK/PA14 |
| 5 | GND | 6 | TDO/PB3 |
| 7 | KEY (NC) | 8 | TDI/PA15 |
| 9 | GND | 10 | RESET# |
| 11 | GND | 12 | TraceCLK/PE2 |
| 13 | GND | 14 | TraceD0/PE3 or SWO / PB3 |
| 15 | GND | 16 | TraceD1/PE4 or nTRST / PB4 |
| 17 | GND | 18 | TraceD2 / PE5 |
| 19 | GND | 20 | TraceD3 / PE6 |

Figure 8. **JTAG debugging connector CN14**

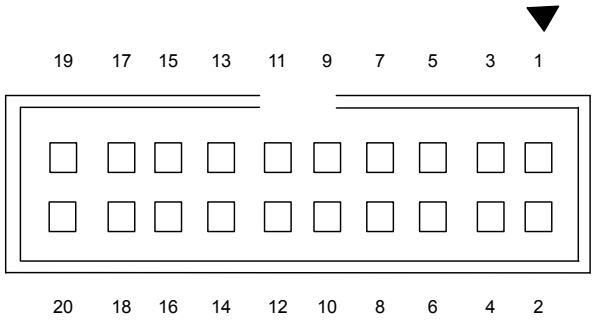



Table 8. **JTAG / SWD debugging connector CN14**

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1 | +3.3V | 2 | +3.3V |
| 3 | TRST(PB4) | 4 | GND |
| 5 | TDI(PA15) | 6 | GND |
| 7 | TMS/SWDIO(PA13) | 8 | GND |
| 9 | TCK/SWCLK(PA14) | 10 | GND |
| 11 | RTCK | 12 | GND |
| 13 | TDO/SWO(PB3) | 14 | GND |
| 15 | RESET# | 16 | GND |
| 17 | DBGRQ(PJ7) | 18 | GND |
| 19 | DBGACK(PJ12) | 20 | GND |

## 6.3 Power supply

### 6.3.1 Board power supply description

The STM32H7B3I-EVAL Evaluation board is designed to be powered from 5 V DC power source. It incorporates a precise polymer Zener diode (Poly-Zen) protecting the board from damage due to the wrong power supply. One of the following six 5 V DC power inputs can be used, upon an appropriate board configuration:

- **5V DC power adapter connected to CN17, the power jack on the board (EXT on the JP29 silkscreen). This is the default configuration.**
- 5V DC power with 500 mA limitation from CN21, the Micro-B USB connector of STLINK-V3E (STLK on the JP29 silkscreen). As explained below, if the USB enumeration succeeds, the ST-LINK U5V power is enabled, by asserting the PWR_EN pin. This pin is connected to a power switch U22, which powers the board. This power switch features also a current limitation to protect the PC in case of short-circuit on board. If overcurrent (More than 600 mA) happens onboard, the LED LD11 is lit.
- 5V DC power with 500 mA limitation from CN14, the USB OTG HS Micro-AB connector (HS on the HJP29 silkscreen)
- 5V DC power with 500 mA limitation from CN27, the USB OTG FS Micro-AB connector (FS on the JP29 silkscreen)
- 5V DC power from CN5 and CN6, the extension connectors for daughterboard (D on the JP29 silkscreen)
- 5V DC power without limitation from CN21, the Micro-B USB connector of STLINK-V3E (CHGR on the JP29 silkscreen)

The STM32H7B3I-EVAL Evaluation board can be powered from ST-LINK USB connector CN21 (“STLK”), but only the ST-LINK circuit has the power before USB enumeration, for the host PC only provides 100 mA to the boards at that time. During the USB enumeration, the STM32H7B3I-EVAL board asks for the 500 mA power to the Host PC.

- If the host is able to provide the required power, the enumeration succeeds, the power transistor U22 is switched ON, the green LED LD7 is turned ON, thus the STM32H7B3I-EVAL board is powered and can consume a maximum current of 500 mA current, but not more.
- If the host is not able to provide the requested current, the enumeration fails. Therefore, the power switch (U22) remains OFF, so consequently, 3.3 V domain of the board and MCU are not powered. As a consequence, the green LED LD7 remains turned OFF. In this case, it is mandatory to use an external power supply as an extra power supply.

“EXT” from PSU or “D” can be used as an external power supply in case current consumption of the STM32H7B3I-EVAL board exceeds the allowed current on USB. In this condition, it is still possible to use USB for communication for programming or debugging only, but it is mandatory to power the board first using E5V or D5V, and then connecting the USB cable to the PC. Proceeding this way ensures that the enumeration succeeds thanks to the external power source.

The following power sequence procedure must be respected:

1. Connect jumper JP29 to EXT or D side.
2. Connect the external power source to EXT or D (With mounted daughterboard).
3. Check green LED LD7 is turned ON.
4. Connect the PC to USB connector CN21.

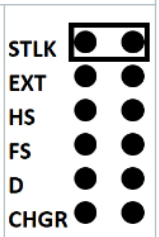
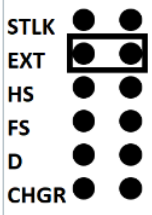
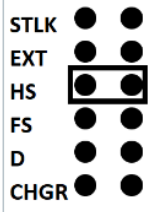
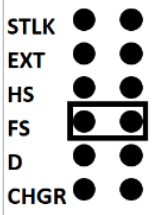
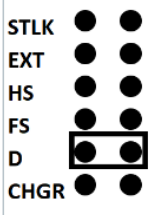
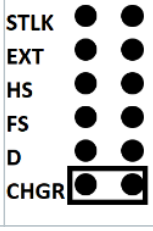
If this order is not respected, the board may be powered by VBUS first then “EXT” or “D”, and the following risks may be encountered:

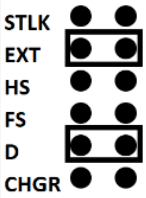
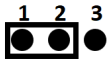
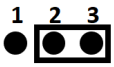
1. If more than 500 mA current is needed by the board, the PC may be damaged or current can be limited by PC. As a consequence, the board is not powered correctly.
2. 500 mA is requested at enumeration, so there is a risk that request is rejected and enumeration does not succeed if PC cannot provide such current. Consequently, the board is not powered and LED LD7 remains OFF.

### 6.3.2 Board power supply - Hardware configuration

The power supply is configured by setting the related jumpers JP3, JP29, and JP37 as described in Table 9.

**Table 9. Power related jumpers**

| Jumper | Description[1] | |
|---|---|---|
| JP3 | JP3 is used to measure current consumption manually with a multimeter.<br>**ON** | |
| JP29 | JP29 is used to select one of the six possible power supply resources:<br>For power supply from USB connector of STLINK-V3E (CN21) to STM32H7B3I-EVAL, JP29 is set as shown on the right. |  |
| | **For power supply jack(CN17) to the STM32H7B3I-EVAL, JP29 is set as shown on the right.** |  |
| | For power supply from USB OTG HS (CN14) to STM32H7B3I-EVAL, JP29 is set as shown on the right. |  |
| | For power supply from USB OTG FS (CN27) to STM32H7B3I-EVAL, JP29 is set as shown on the right. |  |
| | For power supply from the daughterboard connectors (CN5 and CN6) to STM32H7B3I-EVAL, JP29 is set as shown on the right. |  |
| | For power supply from a USB wall charger plugged to CN21 to STM32H7B3I-EVAL, JP29 is set as shown on the right. |  |

| Jumper | Description[1] | |
|---|---|---|
| (Continued) JP29 | For power supply from power supply jack (CN17) to both STM32H7B3I-EVAL and the daughterboard connected on CN5 and CN6, JP29 is set as shown on the right.<br>The daughterboard must not have its own power supply connected. |  |
| JP37 | **$V_{bat}$ is connected to +3.3V when JP37 is set as shown on the right.** |  |
| | $V_{bat}$ is connected to the battery when JP37 is set as shown on the right. |  |

1. *The default setting is in bold.*

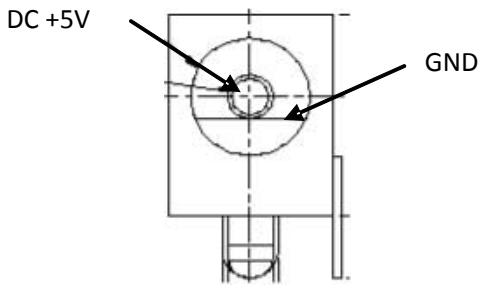
The LED LD7 is lit when the STM32H7B3I-EVAL Evaluation board is powered by the 5V correctly.

*Note: In order to avoid the impact of USB PHY and get precise results of current consumption on JP3, the following caution must be taken into account.*

1. *Configure USB HS PHY into Low Power Mode (Register Address=04, bit 6 in USB PHY).*

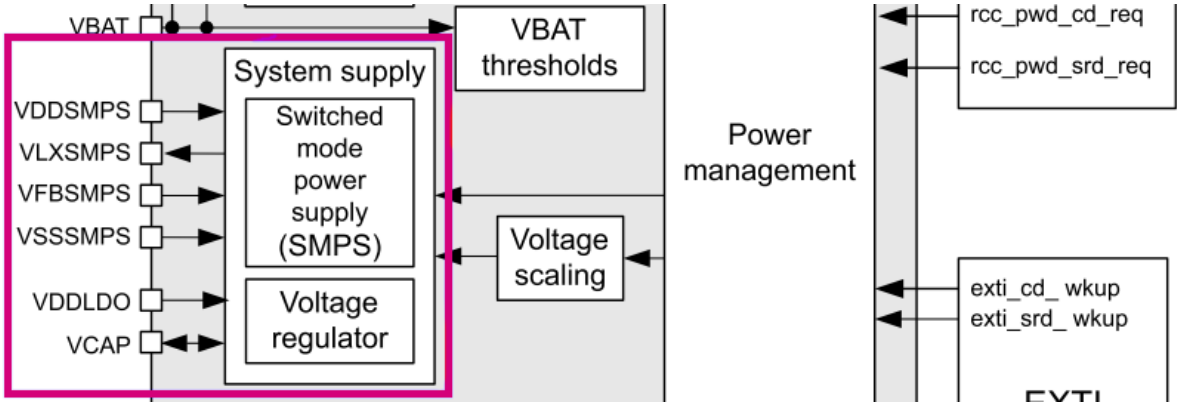
The STM32H7B3I-EVAL Evaluation board can be powered from a DC 5V power supply via the external power supply jack (CN17) shown in Figure 9. The central pin of CN17 must be positive.

**Figure 9. Power supply connector CN17**



### 6.3.3 Board power supply - SMPS / LDO configuration

**Figure 10. MCU Power : SMPS / LDO**




STM32H7B3I-EVAL supports four “SMPS / LDO” configurations of the STM32H7B3LIH6QU microcontroller described in Table 10:

1. LDO supply only
2. SMPS supply only (Default configuration)
3. SMPS and LDO supplies cascaded
4. SMPS and LDO supplies (SMPS supplies 1V8 to board as well)

Some PCB reworks are needed to change power configuration as shown in Table 10:

**Table 10. Internal SMPS / LDO and board configuration**

| Signal name | Setting | Supply config 1: LDO only | Supply config 2: SMPS only[1] | Supply config 3: SMPS and LDO cascaded | Supply config 4: external SMPS |
|---|---|---|---|---|---|
| - | | Figure 11 | **Figure 12** | Figure 13 | Figure 14 |
| SMPS | | OFF | **ON** | ON | ON |
| LDO | | ON | **OFF** | ON | ON |
| 3V3_MCU = VDD_LDO | SB37 | X | - | - | - |
| VFBSD = GND | R251 | X | - | - | - |
| 3V3_SMPS_IN = GND | SB10 | X | - | - | - |
| 3V3_MCU = 3V3_SMPS_IN | R22 | - | **X** | X | X |
| VDD_SMPS_IND_OUT = VDD_LDO | SB3 | - | **X** | X | X |
| VDD_SMPS_IND_OUT = VCAP | SB5 | - | **X** | - | - |
| VCAP capacitor | C121 | 2.2 uF | **100 nF** | 2.2 uF | 2.2 uF |
| VCAP capacitor | C126 | 2.2 uF | **100 nF** | 2.2 uF | 2.2 uF |
| VFBSD = VCAP | R263 | - | **X** | - | - |
| VFBSD = VDD_LDO | R262 | - | - | X | X |
| VDD_SMPS_IND_OUT = 1V8_AO | SB4 | - | - | - | X |
| 1V8_AO capacitor | C21 | - | - | - | X |

1. *The default setting is in bold.*

Figure 11. **Config1 - LDO only**

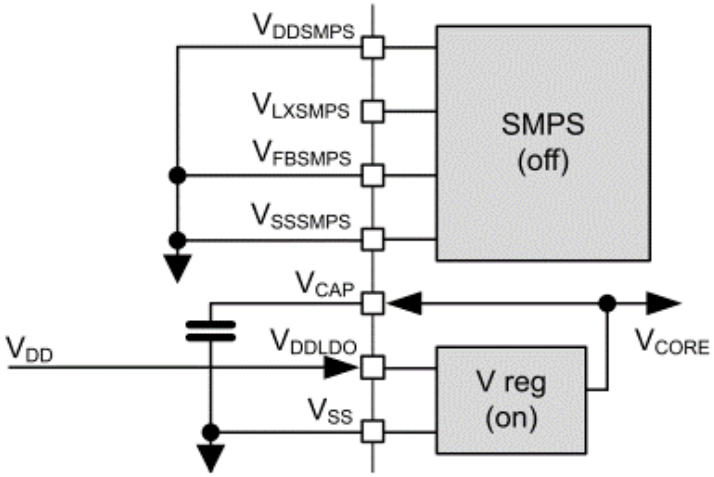



Figure 12. **Config2 - SMPS only (Default configuration)**

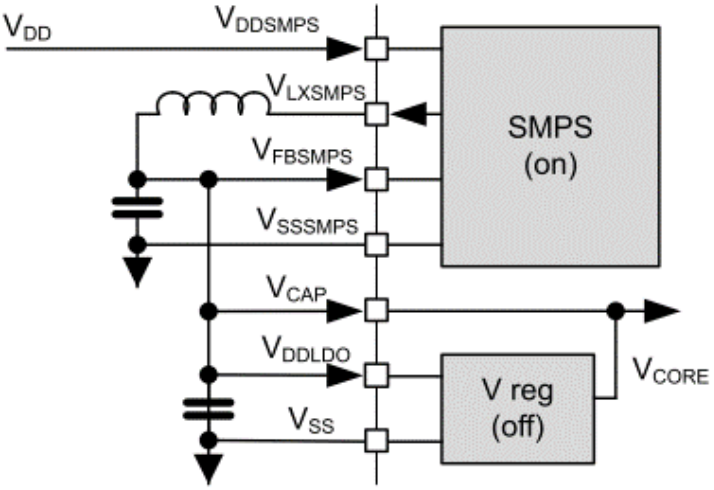


Figure 13. **Config3 - SMPS and LDO cascaded**

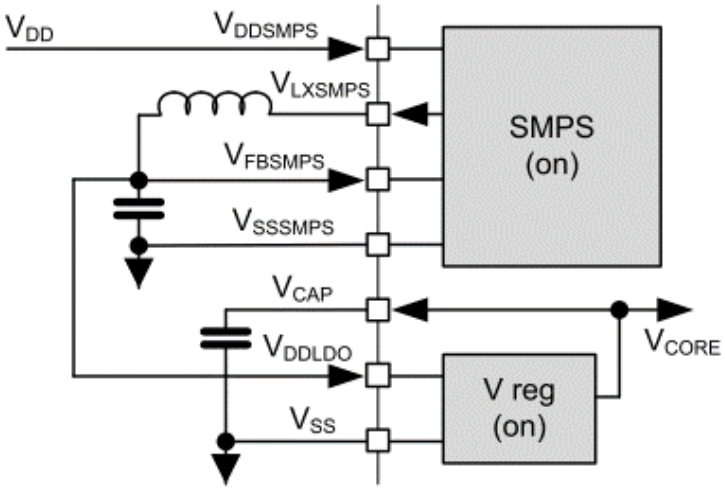
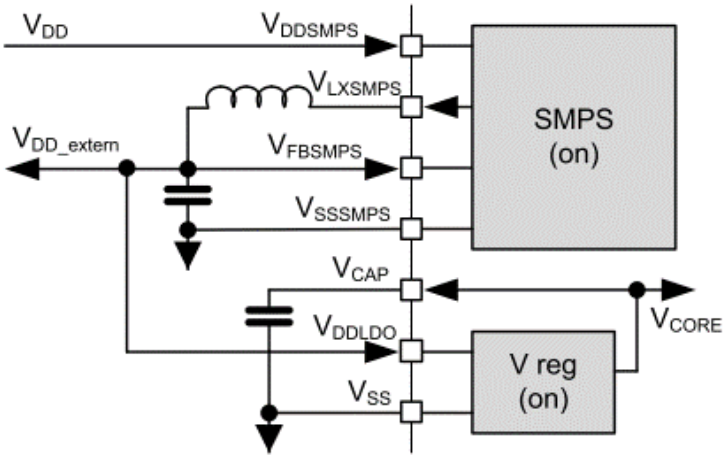



Figure 14. **Config4 - External SMPS**




**Caution:** A deadlock occurs if the board SMPS/LDO firmware PWR configuration does not match its hardware configuration: after the reset, the ST-LINK cannot connect the target anymore.

The firmware PWR configuration must be set as follows in function `SystemClock_Config` in file `main.c`:

- If the hardware configuration is *Direct SMPS* (Default configuration):
  `HAL_PWREx_ConfigSupply(PWR_DIRECT_SMPS_SUPPLY);`
- If the hardware configuration is *LDO*:
  `HAL_PWREx_ConfigSupply(PWR_LDO_SUPPLY);`

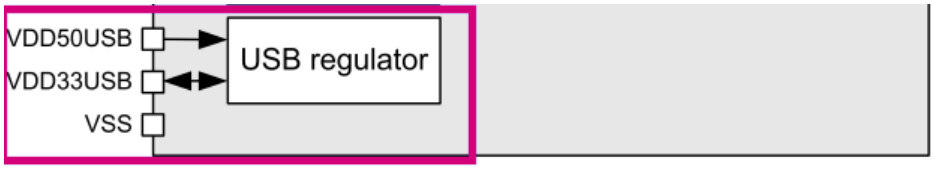
If a deadlock occurs because of a mismatch between hardware and firmware PWR settings (SMPS/LDO), the user can recover the board by applying the following procedure:

1. Power off the board.
2. Set SW1 (BOOT0) to 1 (system memory).
   This changes the BOOT0 pin to 1 instead of 0, thus changing the device boot address to boot address 1 and making the bootloader start in System memory. This avoids starting firmware in the user Flash with a wrong SMPS/LDO configuration versus the hardware board configuration.

3. Power on the board and connect using STM32CubeProgrammer (STM32CubeProg).
4. Erase the user Flash.
5. Power off the board and set SW1 to 0.
6. The board is recovered and can be used normally with matching firmware PWR.

### 6.3.4 Board power supply - VDD50_USB and VREGOUTV33V

**Figure 15. MCU Power: USB regulator**




The USB power sources to STM32H7B3LIH6QU microcontroller can be selected by setting solder bridges as shown in Table 11:

**Figure 16. VDD50_USB and VREGOUTV33V schematic (Page 21)**

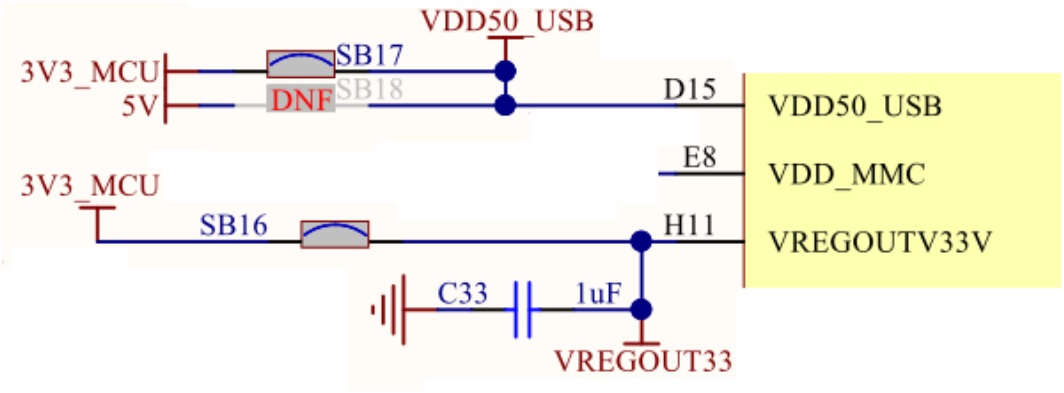



**Table 11. USB power sources**

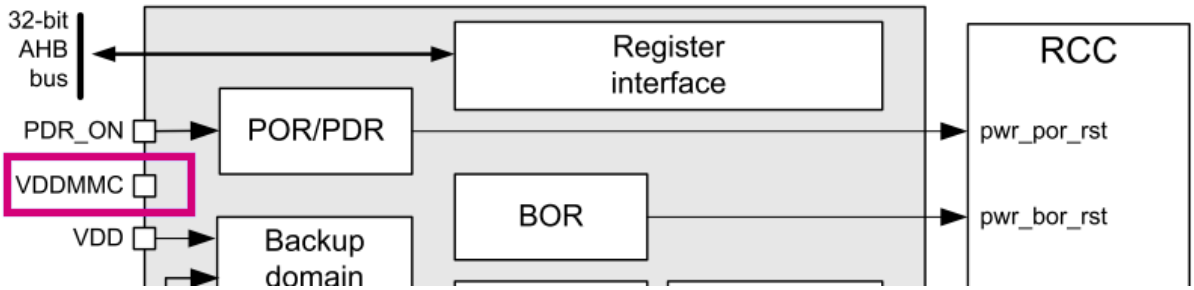
| Power mode[1] | Mount | Unmount |
|---|---|---|
| **External USB supply** | **SB16, SB17** | **SB18** |
| USB regulator supply | SB18 | SB16, SB17 |

1. *The default setting is in bold.*

### 6.3.5 Board power supply - VDDMMC

STM32H7B3I-EVAL can provide either 1.8 V or 3.3 V on VDDMMC power rail of the STM32H7B3LIH6QU microcontroller.

**Figure 17. MCU Power: VDDMMC**




This power rail can be used in different configurations:

- **Default configuration: VDDMMC is forced to 3.3V only.**
- SDIO2 configuration: VDDMMC is switched from 3.3 V to 1.8 V if necessary, and it can be powered off.

**Default configuration (VDDMMC = 3.3 V only)**

*Important:*
*Some pins from STM32H7B3LIH6QU are supplied by VDDMMC, but are '3.3V only' and not linked to SDIO2 (Refer to Table 12)*

**Table 12. Pins supplied by VDDMMC but '3.3V only'**

| Pin name | Pin function |
|---|---|
| PB8 | DCMI_D6 \|\| MEMS_LED \|\| MOTOR_DFSDM1_CKIN7 |
| PB9 | DCMI_D7 \|\| DFSDM1_DATIN7 |
| PD6 | OCSPI1_IO6 \|\| MOTOR_DFSDM1_CKIN4 |
| PG9 | DCMI_VSYNC/RDY |
| PG10 | DCMI_D2 \|\| FMC_NE3 \|\| OCSPI2_IO6 |
| PG11 | DCMI_D3 \|\| OCSPI2_IO7 |
| PG12 | OCSPI2_NCS |
| PG13 | LED1 |
| PG14 | OCSPI1_IO7 |

*Remember: The user must force VDDMMC at 3.3 V when using any of these functions:*

- *OCSPI1: Refer to Section 7.7 .*
- *LED1: Refer to Section 7.10 .*
- *Camera: Refer to Section 7.11 .*
- *MEMS LED and DFSDM: Refer to Section 7.2 .*
- *SRAM (FMC_NE3): Refer to Section 8.1 .*
- *OCSPI2: Refer to Section 8.6 .*
- *Motor control: Refer to Section 8.8 .*

**Table 13. VDDMMC default hardware configuration for '3.3V only' functions**

| Signal name | Setting | VDDMMC = '3.3 V only'(1) |
|---|---|---|
| OCSPI1_NCS (PG6) | JP23 | **[1-2]** |
| 3V3_SW_ENABLE (MFX IO0) | SB34 | **ON**(2) |
| 1V8_SW_ENABLE (MFX IO8) | SB29 | **ON**(2) |

1. *The default setting is in bold.*
2. *PB8 signal is supplied by VDDMMC. Make sure to supply 3.3V on VDDMMC (Refer to Section 6.3.5 ).*

Three possibilities to force VDDMMC to 3.3V:

1. **Default configuration: Software control** (Without hardware modification). In this case, the user must follow the hardware configuration described in Table 13:
   – Set 3V3_SW at 3.3 V by software: 3V3_SW_ENABLE (MFX IO0) = 1 (3V3_SW = ON).
2. Hardware modification to force 3V3_SW to be 'always ON'. If the user prefers 3V3_SW power supply to be always ON:
   – Remove SB34 or set MFX IO0 in high impedance mode (R130 pull-up resistor forces the enable of U14 LDO).

*Remember: In this configuration, the user cannot perform a “power OFF” of 3.3 V supply for SDIO2.*

3. Hardware modification to force VDDMMC to 3.3 V (3V3_AO). If the user wants VDDMMC MCU pin to remain always at 3.3 V without controlling MFX IO0:
   – Remove SB14 and fit SB15 in order to connect this pin to the 3V3_AO power supply.

*Remember: In this configuration, the user cannot use SDIO2 at 1.8 V.*

**SDIO2 configuration (VDDMMC = 1V8_SW or 3V3_SW)**

3V3_SW, 1V8_SW and VDDMMC are set up in order to allow controlling various use-cases with SDIO2 interface, including power OFF sequence, automatic detection of a UHS1 SD card, and switch from 3.3 V to 1.8 V (Refer to chapter 3.3).

**Table 14. SDIO2 pins supplied by VDDMMC (1.8V or 3.3V)**

| Pin name | Pin function |
|---|---|
| PD6 | SDIO2_CK |
| PD7 | SDIO2_CMD |
| PG9 | SDIO2_D0 |
| PG10 | SDIO2_D1 |
| PG11 | SDIO2_D2 |
| PG12 | SDIO2_D3 |

For SD card 2 (SDIO2) interface, in order to control independently 1V8_SW, 3V3_SW, and VDDMMC, it is necessary to control following GPIOs with software:

- SD_LDO_SEL (PG6)
- 3V3_SW_ENABLE (MFX IO0)
- 1V8_SW_ENABLE (MFX IO8)

And the user must follow the hardware configuration described in Table 15.

**Table 15. VDDMMC hardware configuration for '1.8V / 3.3V' function (SDIO2)**

| Signal name | Setting | VDDMMC configuration(1) |
|---|---|---|
| OCSPI1_NCS (PG6) | JP23 | [2-3] |
| 3V3_SW_ENABLE (MFX IO0) | SB34 | **ON**(2) |
| 1V8_SW_ENABLE (MFX IO8) | SB29 | **ON**(2) |

1. *The default setting is in bold.*
2. *PB8 signal is supplied by VDDMMC. Make sure to supply 3.3V on VDDMMC (Refer to Section 6.3.5 ).*

Make sure to take into account schematics below (Figure 18, Figure 19, Figure 20, and Figure 21).

- DNF means that the component is not fitted by default on the board.

**Schematics for 3V3_SW, 1V8_SW, and VDDMMC**

**Figure 18. 3V3_SW_SW_ENABLE and 1V8_SW_ENABLE MFX schematic (Page 2)**

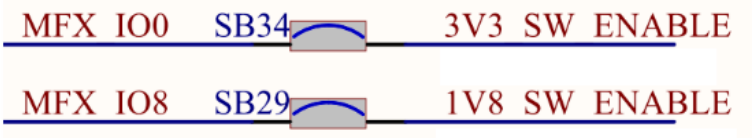


Figure 19. **3V3_SW and 1V8_SW LDOs schematic (page 20)**

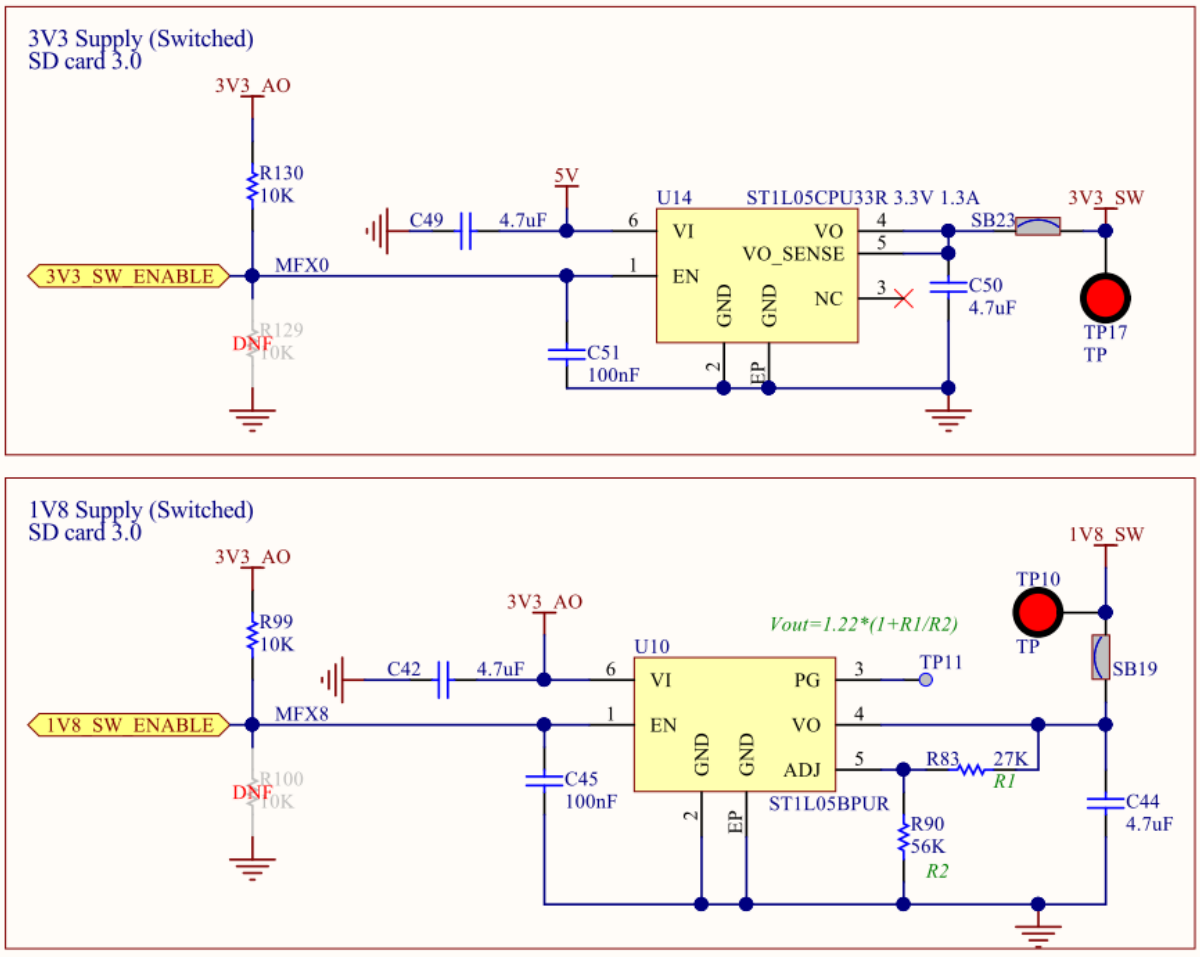



Figure 20. **VDDIO_MMC switch schematic (Page 21)**

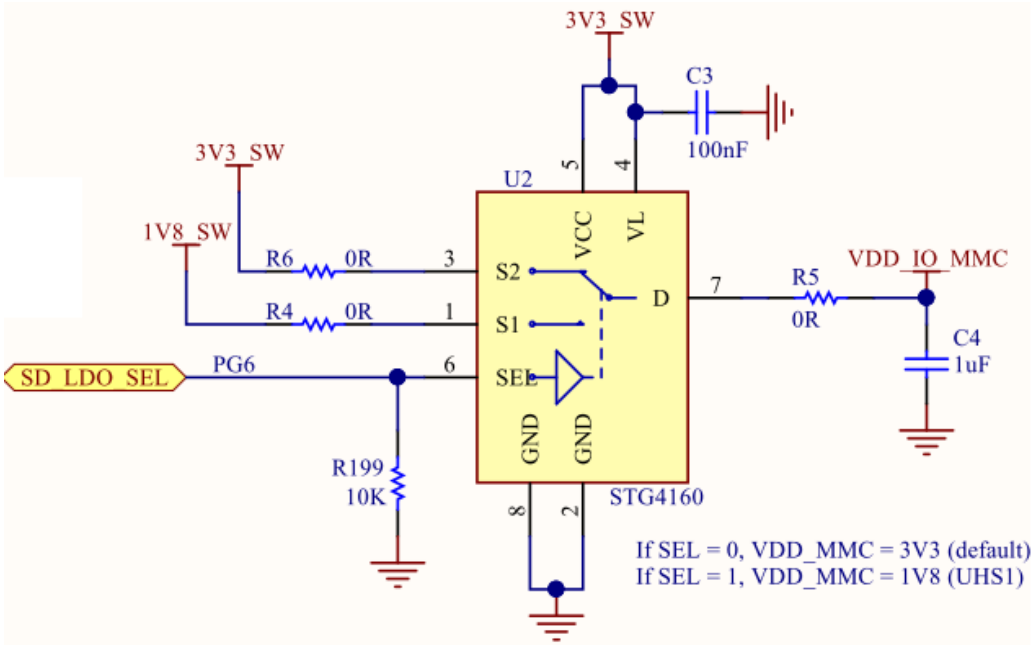
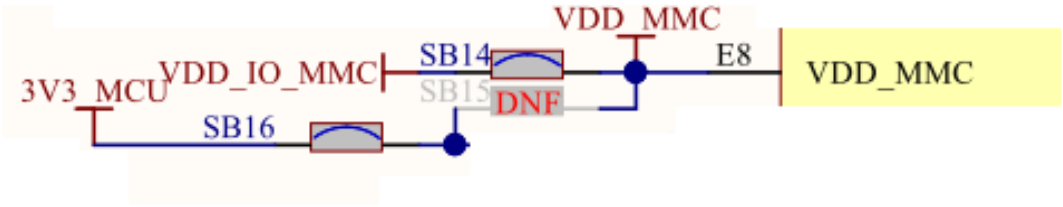


Figure 21. **VDDMMC schematic (Page 9)**




## 6.4 Clock, reset, and boot

### 6.4.1 Clock source

Two clock sources are available on the STM32H7B3I-EVAL Evaluation board for STM32H7B3LIH6QU and its embedded RTC, and other clock sources for their peripherals.

- 24 MHz crystal X1 for the STM32H7B3LIH6QU microcontroller. It can be disconnected by removing R20 and R21 when the internal RC clock is used.
- 32.768 kHz crystal X2 for embedded RTC
- 24 MHz oscillator X3 for USB OTG HS PHY

Table 16. **24 MHz crystal X1 related solder bridges**

| Solder bridge | Description(1) |
|---|---|
| SB7, R21 | **PH0 is connected to 24 MHz crystal when R21 is fitted and SB7 open.** |
| | PH0 is connected to extension connector CN6 when SB7 is closed. In such a case, R21 must be removed to avoid disturbance due to the 24 MHz quartz |
| SB6, R20 | **PH1 is connected to 24 MHz crystal when R20 is fitted and SB6 open.** |
| | PH1 is connected to extension connector CN6 when SB6 is closed. In such case, R20 must be removed to avoid disturbance due to the 24 MHz quartz |

1. *The default setting is in bold.*

Table 17. **32.768 kHz crystal X2 related solder bridges**

| Solder bridge | Description(1) |
|---|---|
| SB8, R23 | **PC14 is connected to 32.768 kHz crystal when R23 is fitted and SB8 is open.** |
| | PC14 is connected to extension connector CN5 when SB8 is closed. In such case R23 must be removed to avoid disturbance due to the 32 Khz quartz. |
| SB9, R24 | **PC15 is connected to 32.768 kHz crystal when R24 is fitted and SB9 is open.** |
| | PC15 is connected to extension connector CN5 when SB9 is closed. In such case R24 must be removed to avoid disturbance due to the 32 Khz quartz. |

1. *The default setting is in bold.*

### 6.4.2 Reset source

The reset signal of STM32H7B3I-EVAL Evaluation board is active low and the reset sources include:

- Reset button B1
- Debugging tools from JTAG/SWD connector CN14 and ETM trace connector CN15
- Daughterboard from CN6
- Embedded STLINK-V3E
- RS-232 connector CN9 for ISP

*Note: The jumper JP24 must be closed for RESET handling with pin8 of RS-232 connector CN9 (CTS signal).*

### 6.4.3 Boot option

The STM32H7B3I-EVAL Evaluation board can boot from:

- Embedded user Flash memory
- System memory with a bootloader for ISP
- Embedded SRAM for debugging

The boot option is configured by setting switch SW1 (BOOT) and the boot base address programmed in the BOOT_ADD0 and BOOT_ADD1 option bytes. The BOOT can be configured also via RS-232 connector CN9.

**Table 18. Boot related switch**

| Switch configuration | Boot address option bytes | Boot space[1] |
|---|---|---|
| 0<br>0<->1<br>  <br>SW1 | BOOT_ADD0[15:0] | **Boot address defined by user option byte BOOT_ADD0[15:0]**<br>**ST programmed value: Flash memory at 0x0800 0000** |
| 1<br>0<->1<br>  <br>SW1 | BOOT_ADD1[15:0] | Boot address defined by user option byte BOOT_ADD1[15:0]<br>ST programmed value: System bootloader at 0x1FF0 0000 |

1. *The default setting is in bold.*

**Table 19. Boot related jumpers**

| Jumper | Description[1] |
|---|---|
| JP22 | **OFF**<br>The Bootloader_BOOT0 is managed by pin 6 of connector CN9 (RS-232 DSR signal) when JP22 is ON. This configuration is used for bootloader application only. |

1. *The default setting is in bold.*

## 6.5 VCP ST-LINK UART

### 6.5.1 Description

Virtual COM port (VCP) UART can be connected to MCU pins **PB14/PB15 (Default configuration)** or PA2/PA3 (Compatible with bootloader).

UART to USB conversion is done by STLINK-V3E STM32F723IEK6 MCU U21 and routed to USB debug connector CN21.

### 6.5.2 Operating voltage

The STM32H7B3LIH6QU UART interface can only be at 3.3 V on this board.

### 6.5.3 Hardware configuration

#### VCP ST-LINK UART on PB14/PB15 (Default configuration)

**Table 20. STLINK-V3E VCP UART (PB14/P15: Default configuration)**

| Pin name | Setting | STLINK-V3E VCP[1] |
|---|---|---|
| PB14 (MCU TX) | **JP21 / SB42** | **ON** |
| | JP39 | OFF |
| PB15 (MCU RX) | **JP20 / SB41** | **ON** |
| | JP40 | OFF |

1. *The default setting is in bold.*

#### VCP ST-LINK RS-232 UART on PA2/PA3

*Important: Audio I2S6, USB HS, and motor control cannot be used with VCP UART PA2/PA3.*

**Table 21. STLINK-V3E VCP UART (PA2/PA3: Compatible with bootloader)**

| Pin name | Setting | STLINK-V3E VCP (Bootloader) |
|---|---|---|
| PA2 (MCU TX) | JP21 | OFF |
| | JP39 / SB42 | ON |
| PA3 (MCU RX) | JP20 | OFF |
| | JP40 / SB41 | ON |

## 6.6 RS-232 UART

### 6.6.1 Description

RS-232 communication is supported by D-type 9-pins RS-232 connector CN9, which is connected to PB14/PB15 (Default configuration) or PA2/PA3 (Compatible with bootloader) pins of STM32H7B3LIH6QU on the STM32H7B3I-EVAL Evaluation board through ST3241EBPR RS-232 transceiver U9.

The Bootloader_RESET and Bootloader_BOOT0 signals are added on RS-232 connector CN9 for ISP support.

### 6.6.2 Operating voltage

The STM32H7B3LIH6QU UART interface can only be at 3.3 V on this board.

### 6.6.3 Hardware configuration

#### RS-232 UART on PB14/PB15 (Default configuration)

Hardware modifications are listed in Table 22:

**Table 22. RS-232 UART (PB14/P15: Default configuration)**

| Pin name | Setting | STLINK-V3E VCP[1] |
|---|---|---|
| PB14 (MCU TX) | JP21 / SB50 | **ON** |
| | JP39 / SB42 | OFF |
| PB15 (MCU RX) | JP20 / SB49 | **ON** |
| | JP40 / SB41 | OFF |

1. *The default setting is in bold.*

**RS-232 UART on PA2/PA3**

*Important: Audio I2S6, USB HS, and motor control cannot be used with VCP UART PA2/PA3.*

Hardware modifications are listed in Table 23:

**Table 23. RS-232 UART related jumpers (PA2/PA3: Bootloader)**

| Pin name | Setting | STLINK-V3E VCP (Bootloader) |
|---|---|---|
| PA2 (MCU TX) | JP21 / SB42 | OFF |
| | JP39 / SB50 | ON |
| PA3 (MCU RX) | JP20 / SB41 | OFF |
| | JP40 / SB49 | ON |

### 6.6.4 Interface

**Figure 22. RS-232 connector CN9**

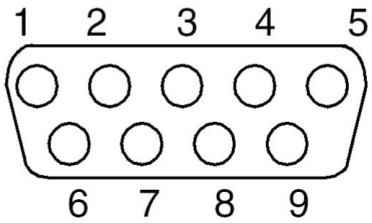



**Table 24. RS-232 connector CN9 with ISP support**

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1 | NC | 6 | Bootloader_BOOT0 |
| 2 | RS232_RX (PB15 or PA3) | 7 | NC |
| 3 | RS232_TX (PB14 or PA2) | 8 | Bootloader_RESET |
| 4 | NC | 9 | NC |
| 5 | GND | | |

# 7 Primary functions

The functions described in the chapter below do not have any usage limitations with each other, except Camera and Audio. For further details, refer to Section 7 Primary functions.

## 7.1 Audio

### 7.1.1 Description

An audio codec CS42L51-CNZ is connected to either I2S6 or SAI interface of STM32H7B3LIH6QU (Refer to Table 25 below for configurations) to support the TDM feature.

This feature implements audio recording on an analog microphone and audio playback of a different audio stream on headphones and lineout at the same time.

It communicates with STM32H7B3LIH6QU via the I2C2 bus.

The analog microphone on the headset is connected to the ADC of CS42L51-CNZ through audio jack CN20.

- External speakers can be connected to CS42L51-CNZ via audio jack CN18.

*Important: I2S6 interface is used by default.*

### 7.1.2 Operating voltage

STM32H7B3LIH6QU SAI and I2S6 interfaces can only be at 3.3 V on this board.

The audio codec CS42L51-CNZ has two power supply voltages:

- VL connected to 3V3_AO (Default configuration)
- VD, VA, and V_HP connected to 1V8_AO (Default configuration).

These pins can also be powered by 3V3_SW and 1V8_SW if necessary by fitting corresponding solder bridges.

### 7.1.3 Limitations and hardware configuration

I2S6 (Default configuration) limitations with primary functions: the camera cannot be used (Refer to the jumper config in Table 25)

I2S6 (Default configuration) limitations with secondary functions: USB HS and JTAG

SAI1 limitations: camera, Wi-Fi® SPI

I2C2 (PH4/PH5) is shared between EXT I²C module (CN24), MB1486 Wi-Fi® module (U24), MFX I/O expander (U25), audio codec (U48), MB1379 camera module (CN2), and MB1370 LCD touch panel (CN30).

Hardware modifications are listed in Table 25:

**Table 25. Hardware configuration for CS42L51-CNZ I2S-SAI communication bus**

| Configuration | Signal name | Pin name | Setting | I2S6 config EXT_SD = PB4 | I2S6 config EXT_SD = PA6 | SAI configuration |
|---|---|---|---|---|---|---|
| I2S6(1) | I2S6_MCK | PA3 | JP9 | **[1-2]** | [1-2] | OFF |
| | | | R139 | **ON** | ON | OFF(2) |
| | I2S6_CK | PA5 | JP11 | **[1-2]** | [1-2] | OFF |
| | | | R135 | **ON** | ON | OFF (2) |
| | I2S6_WS | PA4 | JP7 | **[1-2]** / DCMI_HSYNC cannot be used | [1-2] | OFF |
| | | | R137 | ON | ON | OFF (2) |
| | I2S6_SD | PB5 | JP18 | **[1-2]** | [1-2] | OFF |
| | | | R136 | **ON** | ON | OFF (2) |

| Configuration | Signal name | Pin name | Setting | I2S6 config EXT_SD = PB4 | I2S6 config EXT_SD = PA6 | SAI configuration |
|---|---|---|---|---|---|---|
| (Continued) I2S6[1] | ULPI_D7 | (Continued) PB5 | JP16 | OFF | OFF | OFF |
| | I2S6_EXT_SD | PA6 | JP6 | OFF | [1-2] | OFF |
| | | PB4 | JP8 | **[1-2]** | OFF | OFF |
| | | PA6 or PB4 | R140 | **ON** | ON | OFF [2] |
| SAI1 | SAI1_MCLK_A | PG7 | JP14 | OFF | OFF | ON |
| | | | R411 | OFF[2] | OFF [2] | ON |
| | SAI1_SCK_A | PE5 | JP28 | OFF | OFF | ON |
| | | | R405 | OFF [2] | OFF [2] | ON |
| | SAI1_FS_A | PE4 | JP26 | OFF | OFF | ON |
| | | | R116 | OFF [2] | OFF [2] | OFF [2] |
| | SAI1_SD_A | PE6 | JP27 | OFF | OFF | ON |
| | | | R404 | OFF [2] | OFF [2] | ON |
| | SAI1_SD_B | PE3 | JP34 | OFF | OFF | ON |
| | | | R413 | OFF [2] | OFF [2] | ON |
| | | | R337 | OFF [2] | OFF [2] | OFF [2] |

1. *The default configuration is in bold.*
2. *Remove to avoid stub if necessary.*

*Note: $I^2C$ address of CS42L51-CNZ is 0x94 (AD0=0).*

### 7.1.4 Interface

A 3.5 mm stereo audio jack CN20 is available on STM32H7B3I-EVAL Evaluation board to support headset (Headphone and microphone integrated).

A 3.5 mm stereo audio jack CN18 is available on STM32H7B3I-EVAL Evaluation board to support external speaker.

## 7.2 DFSDM microphones module (MB1299)

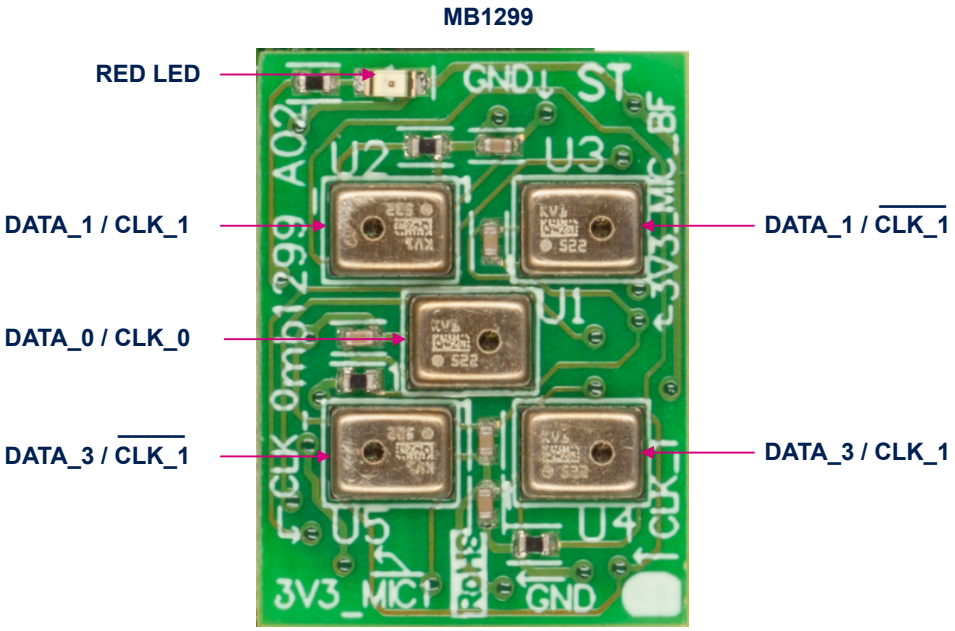
### 7.2.1 Description

A DFSDM Beam Forming microphone module (MB1299) can be connected to STM32H7B3LIH6QU DFSDM interface through CN4.

MB1299 module embeds five DFSDM MEMS microphones STMicroelectronics MP34DT01TR-M:

- One microphone for detection in the center (CLK_0, DATA_0)
- Four other microphones for beamforming (CLK_1, DATA_1, and DATA_3)

**Figure 23. MEMS beamforming microphone module (MB1299)**




CLK_0 and CLK_1 : data valid when the clock is HIGH

$\overline{CLK\_1}$ : data valid when the clock is LOW

**Table 26. DFSDM channel connection between MCU, MB1331, and MB1299**

| MB1299 function | MB1331 function | MCU pin |
|---|---|---|
| CLK_0 | DFSDM12_CKOUT | PB0 |
| DATA_0 | DFSDM12_DATIN1 | PB12 |
| CLK_1 | DFSDM12_CKOUT | PB0 |
| DATA_1 | DFSDM1_DATIN3 | PC7 |
| DATA_3 | DFSDM1_DATIN5 | PB6 |
| VCC_LED | GPIO OUTPUT | PB8 |
| DETECTn | GPIO INPUT | PC5 (2) |

1. *Not connected by default (Conflict with OCSPI1_DQS)*

### 7.2.2 Operating voltage

DFSDM microphone module supports only 3.3 V.

Make sure to supply 3.3 V on VDDMMC (Refer to Section 6.3.5 ).

### 7.2.3 Limitations and hardware configuration

Limitations with primary functions: camera (Refer to jumper configuration in Table 27)

Limitations with secondary functions: USB HS and NOR Flash

Hardware modifications are listed in Table 27:

**Table 27. Hardware configuration for DFSDM microphones module**

| Signal name | Pin name | Setting | DFSDM(1) |
|---|---|---|---|
| DFSDM1_2_DATIN1 | PB12 | JP19 | **[1-2]** |
| DFSDM1_DATIN3 | PC7 | JP35 | **[2-3]** |
| DCMI_D1 | - | R113 | OFF (2) |
| MEMS_LED | PB8(3) | R120 | ON |
| DCMI_D6 | | R110 | OFF (2) |
| DFSDM1_DATIN5 | PB6 | R33 | **OFF** |
| DFSDM1_CKOUT | PB0 | JP10 | **OFF** |

1. *The default setting is in bold.*
2. *Remove to avoid stub if necessary.*
3. *PB8 signal is supplied by VDDMMC. Make sure to supply 3.3V on VDDMMC (Refer to Section 6.3.5*

*Note: $I^2C$ address of CS42L51-CNZ is 0x94 (AD0=0).*

### 7.2.4 Interface

**Figure 24. MEMS microphone module and motor Control module connector CN4**

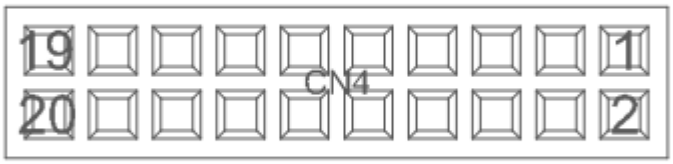



**Table 28. MEMS microphone module MB1299 and motor control module connector CN4**

| Pin number | Description | Pin connection | Pin number | Description | Pin connection |
|---|---|---|---|---|---|
| 1 | GND | GND | 2 | 3V3_AO | 3V3_AO |
| 3 | DFSDM1_2_CKOUT (1) | PB0 | 4 | DFSDM1_2_CKOUT (1) | PB0 |
| 5 | DFSDM1_DATIN3 (1) | PC7 | **6** | DFSDM1_2_DATIN1 (1) | PB12 |
| 7 | DFSDM1_DATIN5 | PB6 | 8 | DFSDM1_DATIN7 (1) | PB9 |

| Pin number | Description | Pin connection | Pin number | Description | Pin connection |
|---|---|---|---|---|---|
| 9 | MOTOR_DFSDM1_DATIN0 | PC1 | 10 | MOTOR_DFSDM1_DATIN2 | PC5 |
| 11 | MOTOR_DFSDM1_CKIN4 | PD6 | 12 | MEMS_LED (1) / MOTOR_DFSDM1_CKIN7 | PB8 |
| 13 | MOTOR_DFSDM1_CKIN3 | PD8 | 14 | MOTOR_DFSDM1_2_CKIN1 | PB13 |
| 15 | MOTOR_DFSDM1_DATIN4 | PE10 | 16 | MOTOR_DFSDM1_CKIN5 | PB7 |
| 17 | MOTOR_DFSDM1_CKIN0 | PC0 | 18 | MOTOR_DFSDM1_CKIN2 | PC4 |
| 19 | 3V3_AO | 3V3_AO | 20 | GND | GND |

1. *Pins used by MB1299. See the limitations in Section 7.2.3 .*

## 7.3 USB OTG FS

### 7.3.1 Description

The STM32H7B3I-EVAL Evaluation board supports USB OTG full speed communication via the USB Micro-AB connector CN27 and the USB power switch U29 connected to $V_{BUS}$. The STM32H7B3I-EVAL Evaluation board can be powered by this USB connection at 5 V DC with 500 mA current limitation.

A green LED LD11 is lit in one of these cases:

- Power switch (U29) is ON and STM32H7B3I-EVAL works as a USB host
- $V_{BUS}$ is powered by another USB host when STM32H7B3I-EVAL works as a USB device.

The red LED LD10 is lit when overcurrent occurs ($I_{VBUS}$ superior to 500 mA).

*Note: The STM32H7B3I-EVAL board must be powered by an external power supply when using the OTG function.*

### 7.3.2 Operating voltage

The STM32H7B3LIH6QU USB OTG FS interface can only be at 3.3 V on this board.

- In host mode, $V_{BUS}$ (5 V) is provided by the U29 power switch.
- In device mode, $V_{BUS}$ (5 V) is provided by an external source connected to CN27.

### 7.3.3 Limitations and hardware configuration

Limitation with secondary function FDCAN1:

- As USB FS DP/DM is shared with FDCAN1 RX/TX, SB36 and SB35 must be removed when using USB OTG FS in order to avoid any stub.

### 7.3.4 Interface

**Table 29. USB OTG FS Micro-AB connector CN27**

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1 | VBUS (PA9) (From STMPS2151STR or to STM32H7B3LIH6QU) | 4 | ID (PA10) |
| 2 | D- (PA11) | 5 | GND |
| 3 | D+ (PA12) | - | - |

## 7.4 microSD™ card 1

### 7.4.1 Description

An 8 GByte (Or more) Micro SD card connected to SDIO1 3.0 port of STM32H7B3LIH6QU is available on the board. The microSD™ card detection is managed by SD_DETECT1 (PF10).

### 7.4.2 Operating voltage

The STM32H7B3LIH6QU microSD™ card interface can only be at 3.3 V on this board.

### 7.4.3 Limitations and hardware configuration

Fit JP15 to connect SD_DETECT1 to the STM32H7B3LIH6QU PF10 pin, and fit JP12 [1-2] to connect SDIO1_D0 to STM32H7B3LIH6QU PC8 pin.

### 7.4.4 Interface

**Figure 25. microSD™ connector CN28**

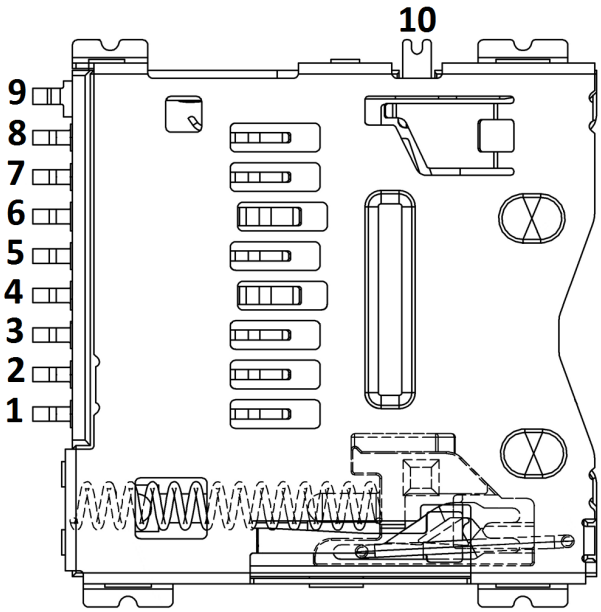



**Table 30. microSD™ connector CN28**

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1 | SD_DATA2 (PC10) | 6 | VSS / GND |
| 2 | SD_DATA3 (PC11) | 7 | SD_DATA0 (PC8) |
| 3 | SD_CMD (PD2) | 8 | SD_DATA1 (PC9) |
| 4 | 3V3_AO | 9 | GND |
| 5 | SD_CLK (PC12) | 10 | Micro SDcard_detect (PF10) |

## 7.5 EXT I²C connector

### 7.5.1 Description

I2C2 bus of STM32H7B3LIH6QU is connected to CN24 on STM32H7B3I-EVAL. The I²C functional daughterboard can be mounted on CN24 and accessed by the microcontroller via the I2C2 bus.

EXT_RESET is controlled by MFX_GPO6 signal.

### 7.5.2 Operating voltage

The STM32H7B3LIH6QU EXT I²C connector can only be at 3.3 V on this board.

### 7.5.3 Limitations and hardware configuration

I2C2 (PH4/PH5) is shared between EXT I²C module CN24, MB1486 Wi-Fi® module U24, MFX I/O expander U25, audio codec U48, MB1379 camera module CN2, and MB1370 LCD touch panel CN30.

### 7.5.4 Interface

**Figure 26. EXT I²C connector CN24**

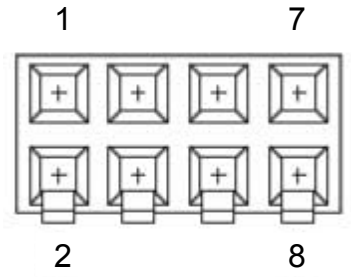



**Table 31. EXT I²C connector CN24**

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1 | I2C2_SDA (PH5) | 5 | +3V3 |
| 2 | NC | 6 | NC |
| 3 | I2C2_SCL (PH4) | 7 | GND |
| 4 | RESET (MFX_GPO6) | 8 | NC |

## 7.6 32-bit SDRAM

### 7.6.1 Description

8 Mx32bit SDRAM ISSI IS42S32800J-6BLI is connected to SDRAM bank1 of FMC interface of STM32H7B3LIH6QU.

### 7.6.2 Operating voltage

The STM32H7B3LIH6QU FMC interface (SDRAM, SRAM, and NOR) can only be at 3.3 V on this board.

### 7.6.3 Limitations and hardware configuration

Limitation with secondary function: OCSPI2.

Hardware modifications are listed in Table 32:

**Table 32. Hardware configuration for SDRAM**

| Pin name | Signal name | Setting | SDRAM(1) |
|---|---|---|---|
| PF0 | FMC_A0 | R339 | **ON** |
| | OCSPI2_IO0 | R98 | OFF (2) |
| PF1 | FMC_A1 | R335 | **ON** |
| | OCSPI2_IO1 | R89 | OFF (2) |
| PF2 | FMC_A2 | R331 | **ON** |

| Pin name | Signal name | Setting | SDRAM(1) |
|---|---|---|---|
| (Continued) PF2 | OCSPI2_IO2 | R82 | OFF (2) |
| PF3 | FMC_A3 | R74 | **ON** |
| | OCSPI2_IO3 | R75 | OFF (2) |
| PG0 | FMC_A10 | R73 | **ON** |
| | OCSPI2_IO4 | R76 | OFF (2) |
| PG1 | FMC_A11 | R333 | **ON** |
| | OCSPI2_IO5 | R77 | OFF (2) |
| PF4 | FMC_A4 | R66 | **ON** |
| | OCSPI2_CLK | R319 | OFF (2) |
| PF5 | FMC_A5 | R65 | **ON** |
| | OCSPI2_NCLK | R318 | OFF (2) |
| PG15 | FMC_SDNCAS | R352 | **ON** |
| | OCSPI2_DQS | R354 | OFF (2) |

1. *The default setting is in bold.*
2. *Remove to avoid stub if necessary.*

## 7.7 Octo-SPI NOR Flash 1

### 7.7.1 Description

One 512-Mbit Octo-SPI NOR Flash Macronix MX25LM51245GXDI00 is connected to OCSPI1 interface of STM32H7B3LIH6QU on the STM32H7B3I-EVAL Evaluation board.

### 7.7.2 Operating voltage

STM32H7B3LIH6QU OCSPI1 interface can only be at 3.3 V on this board. Make sure to supply 3.3 V on VDDMMC (Refer to Section 6.3.5 ).

### 7.7.3 Limitations and hardware configuration

Limitations with secondary function: SDIO2.

Hardware modifications are listed in Table 33:

**Table 33. OCSPI1 hardware configuration**

| Signal name | Pin name | Setting | OCSPI1(1) |
|---|---|---|---|
| OCSPI1_IO6 / SDIO2_CK | PD6(2) | JP4 | **[1-2]** |
| OCSPI1_NCS / SD_LDO_SEL | PG6 | JP23 | **[1-2]** |
| 3V3_SW_ENABLE | MFX IO0(2) | SB34 | **ON** |

1. *The default setting is in bold.*
2. *PD6 signal is supplied by VDDMMC. Make sure to set MFX_IO0 to 1 in order to supply 3.3V on VDDMMC (Refer to Section 6.3.5 )*

## 7.8 Analog input

### 7.8.1 Description

The two-pin header CN7 and 10 KΩ potentiometer RV1 are connected to PA0_C of STM32H7B3LIH6QU as an analog input. A low-pass filter can be implemented by replacing R221 and C96 with the right value of resistor and capacitor as requested by the end user's application.

### 7.8.2 Operating voltage

The STM32H7B3LIH6QU analog input interface can only be at 3.3 V on this board.

### 7.8.3 Interface

**Figure 27. Analog I/O connector CN7**


**Table 34. Analog I/O connector CN7 pinout**

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1 | Analog I/O (**PA0_C**) | 2 | GND |

## 7.9 LCD display module (MB1370)

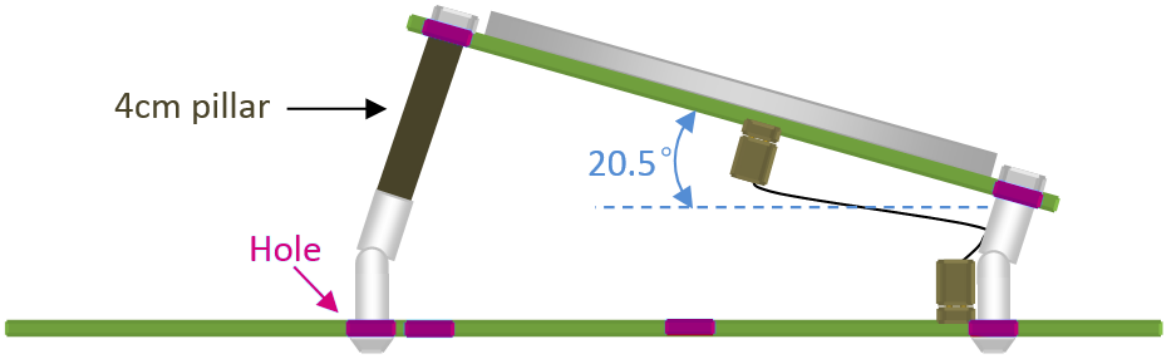
### 7.9.1 Description

The LCD module MB1370 features a 7-inch 800x480 WVGA TFT color LCD.

The ROCKTEK RK070ER9427-CT LCD is connected to STM32H7B3LIH6QU RGB (3x8 bits) interface.

The FOCALTECH FT5336GQQ capacitive touch panel is connected to the STM32H7B3LIH6QU I$^2$C interface. The orientation of the 7-inch LCD daughterboard can be changed by hinged standoffs and pillars. Refer to Figure 28 for details.

**Figure 28. Orientation setting of the 7-inch LCD daughterboard**




### 7.9.2 Operating voltage

The STM32H7B3LIH6QU RGB LCD interface can only be at 3.3 V on this board.

### 7.9.3 Limitations and hardware configuration

I2C2 (PH4/PH5) is shared between EXT I$^2$C module CN24, MB1486 Wi-Fi® module U24, MFX I/O expander U25, audio codec U48, MB1379 camera module CN2, and MB1370 LCD touch panel CN30.

### 7.9.4 Interface

A TFT color LCD with RGB interface module (MB1370) is connected to CN23 using an FFC/FPC flex cable and CN30 using a flat ribbon cable. Refer to Table 35 and Table 36 for details.

LCD RESET and CTP RESET can be connected to GPIOs or to NRST. Refer to Table 37 and Table 38 for details.

**Table 35. LCD module connector CN23**

| Pin number | Description | Pin connection |
|---|---|---|
| 1 | GND | GND |
| 2 | LCD CLK | PI14 |
| 3 | GND | GND |
| 4 | LCD R0 | PI15 |
| 5 | LCD R1 | PJ0 |
| 6 | LCD R2 | PJ1 |
| 7 | LCD R3 | PJ2 |
| 8 | LCD R4 | PJ3 |
| 9 | LCD R5 | PJ4 |
| 10 | LCD R6 | PJ5 |

| Pin number | Description | Pin connection |
|---|---|---|
| 11 | LCD R7 | PJ6 |
| 12 | GND | GND |
| 13 | LCD G0 | PJ7 |
| 14 | LCD G1 | PJ8 |
| 15 | LCD G2 | PJ9 |
| 16 | LCD G3 | PJ10 |
| 17 | LCD G4 | PJ11 |
| 18 | LCD G5 | PK0 |
| 19 | LCD G6 | PK1 |
| 20 | LCD G7 | PK2 |
| 21 | GND | GND |
| 22 | LCD B0 | PJ12 |
| 23 | LCD B1 | PJ13 |
| 24 | LCD B2 | PJ14 |
| 25 | LCD B3 | PJ15 |
| 26 | LCD B4 | PK3 |
| 27 | LCD B5 | PK4 |
| 28 | LCD B6 | PK5 |
| 29 | LCD B7 | PK6 |
| 30 | GND | GND |
| 31 | LCD HSYNC | PI12 |
| 32 | LCD VSYNC | PI13 |
| 33 | LCD DE | PK7 |
| 34 | LCD RESET | PK7 |
| 35 | GND | GND |
| 36 | GND | GND |
| 37 | GND | GND |
| 38 | GND | GND |
| 39 | LCD BL CTRL | PA1 (or PA3) |
| 40 | GND | GND |

**Table 36. CTP and LCD power connector CN30**

| Pin number | Description | Pin connection | Pin number | Description | Pin connection |
|---|---|---|---|---|---|
| 1 | GND | GND | 2 | 3V3_AO | 3.3V |
| 3 | CTP I2C2 SDA | PH5 | 4 | 5V | 5V |
| 5 | CTP I2C2 SCL | PH4 | 6 | 5V | 5V |
| 7 | GND | GND | 8 | GND | GND |
| 9 | CTP RST | PC4 (not used) | 10 | CTP INT | PH2 |

**Table 37. LCD RESET hardware configuration**

| Signal name | R125[1] | R126[1] |
|---|---|---|
| LCD_RESET = NC | **OFF** | **OFF** |
| LCD_RESET = NRST | ON | OFF |
| LCD_RESET = PA2 | OFF | ON |

1. *The default setting is in bold.*

**Table 38. CTP RESET hardware configuration**

| | R155[1] | R156[1] |
|---|---|---|
| CTP_RST = NRST | **ON** | **OFF** |
| CTP_RST = PC4 | OFF | ON |

1. *The default setting is in bold.*

## 7.10 LEDs and buttons

### 7.10.1 Description

Four general-purpose color LEDs (LD1, LD2, LD3, and LD4) are available as display devices.

**Table 39. LCD module connector CN23**

| Pin name | LED name |
|---|---|
| PG13[1] | LED1 |
| MFX IO11 | LED2 |
| MFX IO12 | LED3 |
| MFX IO13 | LED4 |

1. *PG13 pin is supplied by VDDMMC. Make sure to supply 3.3 V on VDDMMC (Refer to Section 6.3.5 ).*

The Wakeup B2 and Tamper/key B3 buttons3 are available as input devices.

**Table 40. B2 and B3 buttons**

| Pin name | Button name |
|---|---|
| PA0 | B2 (KEY_WKUP0) |
| PC13 | B3 (KEY_TAMP_1/WKUP2) |

### 7.10.2 Operating voltage

STM32H7B3LIH6QU LEDs and buttons interface can only be at 3.3 V on this board. For LED1, make sure to supply 3.3 V on VDDMMC (Refer to Section 6.3.5 ).

## 7.11 Camera module MB1379

### 7.11.1 Description

The MB1379 camera module is connected to STM32H7B3LIH6QU DCMI and $I^2C$ interface through CN2. This module embeds an HDF5640-AF-V2.0 module with an OmniVision OV5640 1/4" color CMOS QSXGA (5 megapixel) camera sensor.

### 7.11.2 Operating voltage

STM32H7B3LIH6QU DCMI camera interface can only be at 3.3 V on this board. I²C is at 2.8 V on the camera side and therefore requires the use of level shifters Q1 and Q2. Make sure to supply 3.3 V on VDDMMC (Refer to Section 6.3.5 )

### 7.11.3 Limitations and hardware configuration

Limitation with primary functions: audio I2S6 and DFSDM (Refer to the jumper configuration in Table 41).

Limitation with secondary functions: microSD™ card 2, SAI, USB HS, MEMS LED, NOR, and OCSPI2.

I2C2 (PH4/PH5) is shared between EXT I²C module CN24, MB1486 Wi-Fi® module U24, MFX I/O expander U25, audio codec U48, MB1379 camera module CN2, and MB1370 LCD touch panel CN30.

Hardware modifications are listed in Table 41:

**Table 41. Hardware modifications for camera**

| Pin name | Signal name | Setting | Camera(1) |
|---|---|---|---|
| PA4 | INT_USB_OTG_HS_OVRCR | R108 | **OFF** |
| | DCMI_HSYNC (I2S6_WS cannot be used) | JP7 | [2-3] |
| PC6 | DCMI_D0 | JP32 | **[1-2]** |
| PC7 | FMC_NOR_NE1 | JP35 | OFF(2) |
| | DFSDM1_DATIN3 (Remove MB1299) | JP35 / R120 | OFF / OFF(2) |
| | DCMI_D1 | R113 | **ON** |
| PG10 | FMC_NE3 | JP2 | OFF(2) |
| | SDIO2_D1 | JP2 | OFF(2) |
| | OCSPI2_IO6 | R115 | OFF(2) |
| | DCMI_D2 | R118 | **ON** |
| PG11(3) | OCSPI2_IO7 | R257 | OFF(2) |
| | DCMI_D3 | JP1 | **[1-2]** |
| PE4 | SAI1_FS_A | JP26 | **OFF** |
| | FMC_A20 | R88 | **OFF** |
| | TRACED1 | R340 | **OFF** |
| | DCMI_D4 | R116 | **ON** |
| PB8(3) | MEMS_LED\|\|MOTOR_DFSDM1_CKIN7 | R120 | OFF(2) |
| | DCMI_D6 | R110 | **ON** |
| PB9(3) | DFSDM1_DATIN7 | R233 | **OFF** |
| | DCMI_D7 | R104 | **ON** |
| PG9(3) | DCMI_VSYNC | JP17 | **[1-2]** |
| PA6 | DCMI_PIXCLK | JP6 | **[1-2]** |
| MFX IO0(3) | 3V3_SW_ENABLE | SB34 | **ON** |

1. *The default setting is in bold.*
2. *Remove to avoid stub if necessary.*
3. *PB8, PB9, PG9, PG10, and PG11 signals are using pins supplied by VDDMMC. Make sure to supply 3.3V on VDDMMC (Refer to Section 6.3.5 ).*

### 7.11.4 Interface

Figure 29. **Camera module connector CN2**

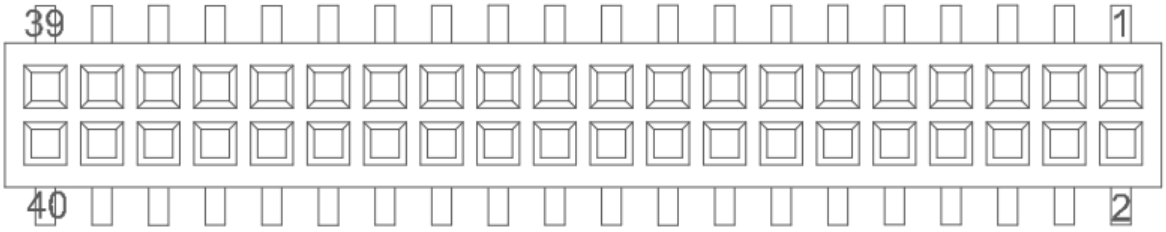



Table 42. **Camera module MB1379 connector CN2**

| Pin number | Description | Pin connection | Pin number | Description | Pin connection |
|---|---|---|---|---|---|
| 1 | TP2 | NC | 2 | TP3 | NC |
| 3 | GND | GND | 4 | GND | GND |
| 5 | NC | NC | 6 | D11 | PH15 |
| 7 | GND | GND | 8 | GND | GND |
| 9 | NC | NC | 10 | NC | NC |
| 11 | GND | GND | 12 | GND | GND |
| 13 | I2C SCL | PH4 | 14 | I2C SDA | PH5 |
| 15 | PLUG | MFX IO4 | 16 | GND | GND |
| 17 | RSTI | MFX IO5 | 18 | TP4 | NC |
| 19 | XSDN | MFX IO6 | 20 | TP5 | NC |
| 21 | GND | GND | 22 | GND | GND |
| 23 | D0 | PC6 | 24 | D1 | PC7 |
| 25 | D2 | PG10 | 26 | D3 | PG11 |
| 27 | D4 | PE4 | 28 | D5 | PD3 |
| 29 | D6 | PB8 | 30 | D7 | PB9 |
| 31 | HSYNC | PA4 | 32 | VSYNC | PG9 |
| 33 | PIXCLK | PA6 | 34 | TP6 | NC |
| 35 | TP7 | NC | 36 | TP8 | NC |
| 37 | GND | GND | 38 | GND | GND |
| 49 | 2V8 | 2V8 | 50 | 2V8 | 2V8 |

## 7.12 Wi-Fi® module MB1486

### 7.12.1 Description

An embedded serial to 802.11 a/b/g/n compliant Wi-Fi® module, MB1486 with INVENTEK ISM43340-M4G-L44-10CF, is connected to STM32H7B3LIH6QU SPI, I$^2$C, and GPIO interface through U24.

### 7.12.2 Operating voltage

STM32H7B3LIH6QU Wi-Fi® interface (SPI, GPIO, and I$^2$C) can only be at 3.3 V on this board. A 5 V power supply is required for the MB1486 Wi-Fi® module with INVENTEK ISM43340-M4G-L44-10CF.

### 7.12.3 Limitations and hardware configuration

Limitations with secondary functions: FMC A19, A21-23, trace, and SAI.

I2C2 (PH4/PH5) is shared between EXT I$^2$C module CN24, MB1486 Wi-Fi® module U24, MFX I/O expander U25, audio codec U48, MB1379 camera module CN2, and MB1370 LCD touch panel CN30.

Hardware modifications are listed in Table 43 below:

**Table 43. Hardware modifications for Wi-Fi®**

| Signal name | Pin name | Setting | Wi-Fi®(1) |
|---|---|---|---|
| WIFI_SPI4_SCK | PE2 | R343 | **ON** |
| FMC_A23 | | R342 | OFF(2) |
| TRACECLK | | R101 | OFF(2) |
| WIFI_SPI4_NSS | PE3 | R337 | **ON** |
| SAI1_SD_B | | JP34 | OFF |
| FMC_A19 | | R97 | OFF(2) |
| TRACED0 | | R93 | OFF(2) |
| WIFI_SPI4_MISO | PE5 | R69 | **ON** |
| SAI1_SCK_A | | JP28 | OFF |
| FMC_A21 | | R324 | OFF(2) |
| TRACED2 | | R71 | OFF(2) |
| WIFI_SPI4_MOSI | PE6 | R334 | **ON** |
| SAI1_SD_A | | JP27 | OFF |
| FMC_A22 | | R78 | OFF(2) |
| TRACED3 | | R80 | OFF(2) |

1. *The default setting is in bold.*
2. *Remove to avoid stub if necessary.*

### 7.12.4 Interface

Figure 30. **Wi-Fi® module interposer footprint (Top view)**

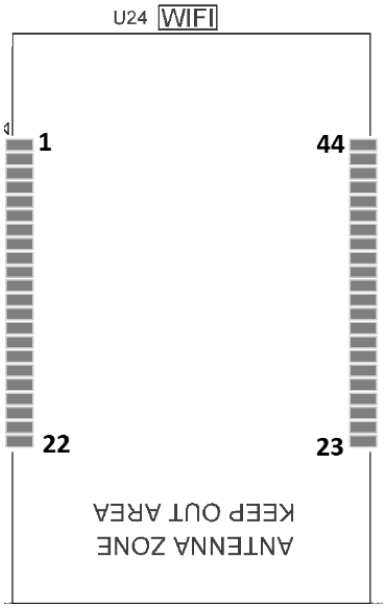



Table 44. **Wi-Fi® module interposer connector U24**

| Pin number | Description | Pin connection | Pin number | Description | Pin connection |
|---|---|---|---|---|---|
| 1 | GND | GND | 44 | NC | NC |
| 2 | NC | NC | 43 | GND | GND |
| 3 | GND | GND | 42 | VDD_5V | 5V |
| 4 | I2C SDA | PH5 | 41 | GND | GND |
| 5 | I2C SCL | PH4 | 40 | WIFI DATA RDY | MFX IO2 |
| 6 | NC | NC | 39 | WIFI BOOT | MFX IO14 |
| 7 | NC | NC | 38 | NC | NC |
| 8 | SPI MOSI | PE6 | 37 | NC | NC (TP26) |
| 9 | SPI NSS | PE3 | 36 | NC | NC (TP27) |
| 10 | SPI SCK | PE2 | 35 | WIFI UART RX | PB15 or PA3 (NC by default) |
| 11 | SPI MISO | PE5 | 34 | WIFI UART TX | PB14 or PA2 (NC by default) |
| 12 | NC | NC | 33 | GND | GND |
| 13 | WIFI GPIO | MFX IO1 | 32 | USB DM | NC |
| 14 | WIFI NRST | MFX IO15 (or NRST) | 31 | USB DP | NC |
| 15 | WIFI WAKEUP | MFX IO10 | 30 | GND | GND |
| 16 | NC | NC | 29 | T_SWDIO | PA13 (NC by default) |
| 17 | NC | NC | 28 | T_SWCLK | PA14 (NC by default) |
| 18 | NC | NC | 27 | NC | NC |
| 19 | NC | NC | 26 | NC | NC |

| Pin number | Description | Pin connection | Pin number | Description | Pin connection |
|---|---|---|---|---|---|
| 20 | NC | NC | 25 | NC | NC |
| 21 | NC | NC | 24 | NC | NC |
| 22 | NC | NC | 23 | GPIO4 | GND |

## 7.13 MFX (Multi-function expander)

### 7.13.1 Description

The MFX circuit on the STM32H7B3I-EVAL Evaluation board acts as an I/O expander. The communication interface between MFX and STM32H7B3LIH6QU is the I2C2 bus.

I2C2 (PH4/PH5) is shared between EXT $I^2C$ module CN24, MB1486 Wi-Fi® module U24, MFX I/O expander U25, audio codec U48, MB1379 camera module CN2, and MB1370 LCD touch panel CN30.

The signals connected to MFX are listed in Table 45.

**Table 45. MFX signals**

| Pin number of MFX | Pin name of MFX | MFX functions | Function of STM32H7B3I-EVAL | Direction (For MFX) | Terminal device |
|---|---|---|---|---|---|
| 18 | PB0 | MFX_GPIO0 | 3V3_SW_ENABLE | Output | PWR |
| 19 | PB1 | MFX_GPIO1 | WIFI_GPIO | Output | WIFI |
| 20 | PB2 | MFX_GPIO2 | WIFI_DATRDY | Output | WIFI |
| 39 | PB3 | MFX_GPIO3 | Audio_RST | Output | Codec |
| 40 | PB4 | MFX_GPIO4 | Camera_PLUG_IN | Input | Camera |
| 15 | PA5 | MFX_GPIO5 | Camera_RSTI | Input | Camera |
| 16 | PA6 | MFX_GPIO6 | Camera_XSDN | Input | Camera |
| 17 | PA7 | MFX_GPIO7 | USB_OTG_FS_PWR_EN | Output | USB FS |
| 29 | PA8 | MFX_GPIO8 | 1V8_SW_ENABLE | Output | PWR |
| 30 | PA9 | MFX_GPIO9 | FDCAN_STBY | Output | CAN FD |
| 31 | PA10 | MFX_GPIO10 | WIFI_WKUP | Output | WIFI |
| 32 | PA11 | MFX_GPIO11 | LED2 | Output | LED |
| 33 | PA12 | MFX_GPIO12 | LED3 | Output | LED |
| 26 | PB13 | MFX_GPIO13 | LED4 | Output | LED |
| 27 | PB14 | MFX_GPIO14 | WIFI_BOOT | Output | WIFI |
| 28 | PB15 | MFX_GPIO15 | WIFI_RST | Output | WIFI |
| 3 | PC14 | MFX_GPO4 | USB_OTG_HS_PWR_EN | Output | USB HS |
| 5 | PH0 | MFX_GPO5 | USB_HS_PHY_RESET | Output | USB HS |
| 6(1) | PH1 | MFX_GPO6 | EXT_RESET / MOTOR_GPIO1 | Output / Output | I2C EXT / MOTOR |
| 38 | PA15 | MFX_GPO7 | MOTOR_GPIO2 | Output | MOTOR |

1. *This pin is shared between different functions and requires a hardware configuration (Such as jumpers and solder bridges).*

### 7.13.2 Operating voltage

STM32H7B3LIH6QU MFX interface (GPIO, $I^2C$) can only be at 3.3 V on this board.

### 7.13.3 Limitations and hardware configuration

Limitations with a secondary function: When using motor control CN1, EXT_I2C CN24 cannot be used as MFX_GPO6 is used for both.

### 7.13.4 Interface

The connector CN26 is used only for MFX (Multi-Function eXpander) programming during board manufacturing. It is not populated by default and not for the end-user.

# 8 Secondary functions

Functions described in the chapter below have usage limitations with primary functions or with each other. Refer to Section 8 Secondary functions for further details.

## 8.1 SRAM

### 8.1.1 Description

1Mx16bit SRAM ISSI IS61WV102416BLL-10MLI is connected to bank1 NOR/PSRAM2 of FMC interface and both 8-bit and 16-bit access are allowed by BLN0 and BLN1 connected to BLE and BHE of SRAM respectively.

### 8.1.2 Operating voltage

STM32H7B3LIH6QU FMC interface (SDRAM, SRAM, and NOR) can only be at 3.3 V on this board. Make sure to supply 3.3 V on VDDMMC (Refer to Section 6.3.5 ).

### 8.1.3 Limitations and hardware configuration

Limitations with primary functions: camera (Refer to the jumper configuration in Table 46).

Limitations with secondary functions: OCSPI2.

Hardware modifications are listed in Table 46 below:

**Table 46. Configuration for SRAM A0-A5, A10-11 addresses, and command**

| Pin name | Signal name | Setting | SRAM(1) |
|---|---|---|---|
| PF0 | FMC_A0 | R339 | **ON** |
| | OCSPI2_IO0 | R98 | OFF(2) |
| PF1 | FMC_A1 | R335 | **ON** |
| | OCSPI2_IO1 | R89 | OFF(2) |
| PF2 | FMC_A2 | R331 | **ON** |
| | OCSPI2_IO2 | R82 | OFF(2) |
| PF3 | FMC_A3 | R74 | **ON** |
| | OCSPI2_IO3 | R75 | OFF(2) |
| PG0 | FMC_A10 | R73 | **ON** |
| | OCSPI2_IO4 | R76 | OFF(2) |
| PG1 | FMC_A11 | R333 | **ON** |
| | OCSPI2_IO5 | R77 | OFF(2) |
| PF4 | FMC_A4 | R66 | **ON** |
| | OCSPI2_CLK | R319 | OFF(2) |
| PF5 | FMC_A5 | R65 | **ON** |
| | OCSPI2_NCLK | R318 | OFF(2) |
| PG10 | FMC_NE3(3) | R280 / JP2 | ON / [1-2] |
| | SDIO2_D1 | R280 / JP2 | OFF(2) / OFF |
| | OCSPI2_IO6 | R115 | OFF(2) |
| | DCMI_D2(3) | R118 | OFF(2) |

1. *The default setting is in bold.*
2. *Remove to avoid stub if necessary.*

3. *PG10 signal is supplied by VDDMMC. Make sure to supply 3.3 V on VDDMMC (Refer to Section 6.3.5 )*

*Note: If using SD card 1 (Default configuration), use FMC_NE3 = PG10, then SD card 2 cannot be used). If using SD card 2, use FMC_NE3 = PC8 by fitting JP12 [2-3], then SD card 1 cannot be used.*

### 8.1.4 Limitations and hardware configuration for SRAM A19 (Just for the test)

Limitations with primary functions: Wi-Fi® SPI.

Limitations with secondary functions: SAI1 and TRACE cannot be used.

Hardware modifications are listed in Table 47 below:

**Table 47. Configuration for SRAM A19 (Just for the test)**

| Pin name | Signal name | Setting | SRAM |
|---|---|---|---|
| PE3 | SAI1_SD_B | JP34 | OFF |
| | WIFI_SPI4_NSS | R337 | OFF(1) |
| | TRACED0 | R93 | OFF(1) |
| | FMC_A19 | R97 | ON just for test |

1. *Remove to avoid stub if necessary.*

*Note: If using SD card 1 (Default configuration), use FMC_NE3 = PG10, then SD card 2 cannot be used). If using SD card 2, use FMC_NE3 = PC8 by fitting JP12 [2-3], then SD card 1 cannot be used.*

## 8.2 NOR

### 8.2.1 Description

128Mbit NOR Flash Micron MT28EW128ABA1LPC-0SIT is connected to bank1 NOR/PSRAM1 of the FMC interface. The 16-bit operation mode is selected by a pull-up resistor connected to the BYTE pin of the NOR Flash memory.

### 8.2.2 Operating voltage

STM32H7B3LIH6QU FMC interface (SDRAM, SRAM, and NOR) can only be at 3.3 V on this board.

### 8.2.3 Limitations and hardware configuration

The write protection can be enabled by fitting jumper JP25.

Limitations with primary functions: camera and DFSDM (Refer to jumper configuration Table 48 below)

Limitations with secondary functions: OCSPI2 FMC addresses

Hardware modifications are listed in Table 48 below.

**Table 48. Configuration for NOR A0-A5, A10-11 addresses, and command**

| Pin name | Signal name | Setting | NOR(1) |
|---|---|---|---|
| PF0 | FMC_A0 | R339 | **ON** |
| | OCSPI2_IO0 | R98 | OFF(2) |
| PF1 | FMC_A1 | R335 | **ON** |
| | OCSPI2_IO1 | R89 | OFF(2) |
| PF2 | FMC_A2 | R331 | **ON** |
| | OCSPI2_IO2 | R82 | OFF(2) |
| PF3 | FMC_A3 | R74 | **ON** |
| | OCSPI2_IO3 | R75 | OFF(2) |

| Pin name | Signal name | Setting | NOR[1] |
|---|---|---|---|
| PG0 | FMC_A10 | R73 | **ON** |
| | OCSPI2_IO4 | R76 | OFF[2] |
| PG1 | FMC_A11 | R333 | **ON** |
| | OCSPI2_IO5 | R77 | OFF[2] |
| PF4 | FMC_A4 | R66 | **ON** |
| | OCSPI2_CLK | R319 | OFF[2] |
| PF5 | FMC_A5 | R65 | **ON** |
| | OCSPI2_NCLK | R318 | OFF[2] |
| PC7 | FMC_NOR_NE1 / DFSDM_DATIN3<br>Remove MB1299 | JP35 | [1-2] |
| | DCMI_D1 | R113 | OFF[2] |

1. *The default configuration is in bold.*
2. *Remove to avoid stub if necessary.*

### 8.2.4 Limitations and hardware configuration for NOR A19-A22 (Just for the test)

Limitations with primary functions: camera, Wi-Fi® SPI.
Limitations with secondary functions: SAI1 and TRACE
Hardware modifications are listed in Table 49 below:

**Table 49. Configuration for SRAM A19-A22 (Just for the test)**

| Pin name | Signal name | Setting | NOR |
|---|---|---|---|
| PE3 | SAI1_SD_B | JP34 | OFF |
| | WIFI_SPI4_NSS | R337 | OFF[1] |
| | TRACED0 | R93 | OFF[1] |
| | FMC_A19 | R97 | ON just for test |
| PE4 | SAI1_FS_A | JP26 | N/A |
| | TRACED1 | R340 | N/A |
| | DCMI_D4 | R116 | N/A |
| | FMC_A20 | R88 | ON just for test |
| PE5 | WIFI_SPI4_MISO | R69 | N/A |
| | SAI1_SCK_A | JP28 | N/A |
| | TRACED2 | R71 | N/A |
| | FMC_A21 | R324 | ON just for test |

1. *Remove to avoid stub if necessary.*

*Note: If using SD card 1 (Default configuration), use FMC_NE3 = PG10, then SD card 2 cannot be used). If using SD card 2, use FMC_NE3 = PC8 by fitting JP12 [2-3], then SD card 1 cannot be used.*

## 8.3 microSD™ card 2

### 8.3.1 Description

A microSD™ card connector connected to the SDIO2 3.0 port of STM32H7B3LIH6QU is available on the board. The microSD™ card detection is managed by SD_DETECT2 (PI11).

It supports SD 3.0, SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 high-speed (50 MHz) and default speed (25 MHz) modes.

SDIO2 signals are all supplied by VDDMMC. Make sure to supply 3.3 V or 1.8 V on VDDMMC (Refer to Section 6.3.5 ).

### 8.3.2 Operating voltage

As SDIO2 is in the VDDMMC domain (VDDMMC = 3.3 V or 1.8 V), when going to UHS1 mode (1.8 V), the STG4160 switch U2 allows switching signals from 3.3 V to 1.8 V using the SD_LDO_SEL signal (PG6). 3V3_SW and 1V8_SW can also be switched OFF using MFX IO0 and MFX IO8 in case a power-off sequence is needed.

### 8.3.3 Limitations and hardware configuration

Limitations with primary functions: camera and OCSPI1 (Refer to jumper configuration below)

Limitations with secondary functions: SRAM and OCSPI2

Hardware modifications are listed in Table 50 below:

**Table 50. Configuration for NOR A0-A5, A10-11 addresses, and command**

| Signal name | Setting | SDIO2 configuration(1) |
|---|---|---|
| SDIO2_D0 (PG9) (DCMI_VSYNC) | JP17 | [2-3](2) |
| SDIO2_D1 (PG10) | R118 | OFF(3) |
| | R115 | OFF(3) |
| | R280 | ON(2) |
| | JP2 | [2-3](2) |
| SDIO2_D2 (PG11) (DCMI_D3) | R257 | OFF |
| | JP1 | [2-3](2) |
| SDIO2_D3 (PG12) | R122 | **ON(2)** |
| SD_LDO_SEL (PG6) (OCSPI1_NCS) | JP23 | [2-3](2) |
| SDIO2_CK (PD6) | JP4 | [2-3](2) |
| SD_DETECT2 (PI11) | JP13 | ON(2) |
| 3V3_SW_ENABLE (MFX IO0) | SB34 | **ON(2)** |
| 1V8_SW_ENABLE (MFX IO8) | SB29 | **ON(2)** |

1. *The default configuration is in bold.*
2. *SDIO2 signals are all supplied by VDDMMC. Make sure to supply 3.3 V or 1.8 V on VDDMMC (Refer to Section 6.3.5 ).*
3. *Remove to avoid stub if necessary.*

*Note: Remove the MB1242 OCSPI module when using the SD card 2 interface.*

### 8.3.4 Interface

Figure 31. microSD™ connector CN3

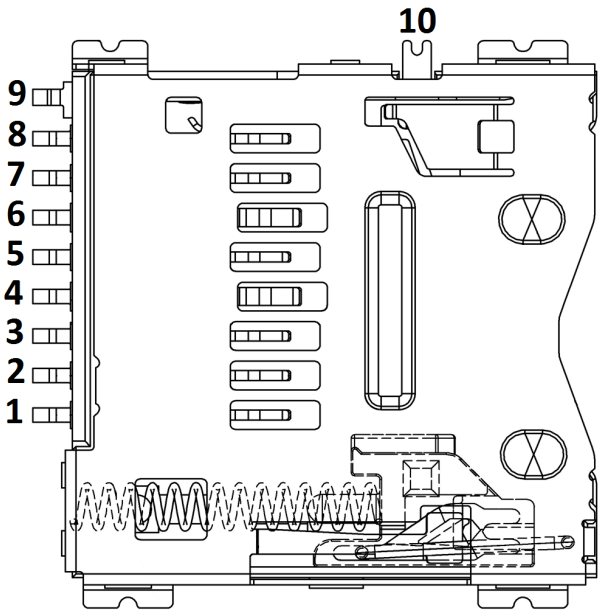



Table 51. microSD™ connector CN3

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1 | SD_DATA2 (PG11) | 6 | VSS/GND |
| 2 | SD_DATA3 (PG12) | 7 | SD_DATA0 (PG9) |
| 3 | SD_CMD (PD7) | 8 | SD_DATA1 (PG10) |
| 4 | 3V3_SW | 9 | GND |
| 5 | SD_CLK (PD6) | 10 | Micro SDcard_detect (PI11) |

## 8.4 USB OTG HS

### 8.4.1 Description

STM32H7B3I-EVAL Evaluation board supports USB OTG high-speed communication via a USB Micro-AB connector CN8, and a USB high-speed PHY U7, connected to STM32H7B3LIH6QU ULPI bus for high-speed function.

USB high-speed PHY (U7) RESETB pin is connected to MFX_GPO5 signal, and can also be connected to NRST if needed by removing SB31 and fitting SB13.

USB high-speed PHY (U7) REFCLK pin is connected to an external 24 MHz oscillator (X3).

The STM32H7B3I-EVAL Evaluation board can be powered by this USB connector (CN8) at 5V DC with 500mA current limitation.

A USB power switch (U39) is also connected to $V_{BUS}$ and provides power to CN8 (with SB11 closed). U39 can be enabled with CPEN from U7 with SB12 fitted. It can also be controlled by an MFX GPIO (MFX_GPO4).

Green LED LD6 for CN8 is lit when either:

- The power switch (U39) is ON and STM32H7B3I-EVAL works as a USB host.
- $V_{BUS}$ is powered by another USB host when STM32H7B3I-EVAL works as a USB device.

Red LED LD5 is lit when over-current occurs ($IV_{BUS}$ > 500 mA).

*Note: STM32H7B3I-EVAL Evaluation board must be powered by an external power supply when using the OTG function.*

### 8.4.2 Operating voltage

STM32H7B3LIH6QU ULPI interface can only be at 3.3 V on this board. USB OTG HS external PHY requires the following power supplies:

- 5 V for VBAT pin
- 3.3 V for VDDIO pin
- 1.8 V for VDD_1V8 pins

### 8.4.3 Limitations and hardware configuration

Limitations with primary functions: camera, I2S6, and DFSDM

Hardware modifications are listed in Table 52.

**Table 52. USB OTG HS function configuration**

| Signal name | Pin name | Setting | USB HS (CN8)(1) |
|---|---|---|---|
| ULPI_D0 / I2S6_MCK | PA3 | JP9 | [2-3] |
| ULPI_D1 / DFSDM12_CKOUT | PB0 | JP10 | ON |
| ULPI_D5 / DFSDM12_DATIN1 | PB12 | JP19 | [2-3] |
| ULPI_D7 | PB5 | JP16 | ON |
| I2S6_SD | | JP18 | OFF |
| ULPI_CK / I2S6_CK | PA5 | JP11 | [2-3] |
| USB_OTG_HS_OVCR | PA4 | R108 | ON |
| I26_WS / DCMI_HSYNC | | JP7 | OFF |
| USB_OTG_HS_PWR_EN | U7 CPEN | SB12 | **ON** |
| | MFX_GPO4 | SB32 | OFF |
| USB_HS_PHY_RESET | MFX_GPO5 | SB31 | **ON** |
| | NRST | SB13 | OFF |

1. *The default configuration is in bold.*

### 8.4.4 Interface

**Table 53. USB OTG HS Micro-AB connector CN8**

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1 | VBUS (From STMPS2151STR or to USB3320C-EZK) | 4 | ID (From USB3320C-EZK) |
| 2 | D- (From USB3320C-EZK) | 5 | GND |
| 3 | D+ (From USB3320C-EZK) | - | - |

## 8.5 DFSDM STMP2 and PT100 monitoring

### 8.5.1 Description

Two STMPS2 ICs are connected to STM32H7B3LIH6QU DFSDM1_2 interface:

- U36 is transmitting analog data from a power metering jumper (JP1) to DFDSM_DATIN1.
- U37 is transmitting temperature analog data from a PTS (R200) to DFDSM_DATIN5.

### 8.5.2 Operating voltage

STM32H7B3LIH6QU DFSDM STMPS2 and PT100 monitoring interfaces can only be at 3.3 V on this board. The power supply (VCC) of both STPMS2L-PUR (U36 and U37) is “3V3_SW”. Take care to control this power supply or use one of the hardware configurations to force it “always ON” (Refer to Section 8.5.2 )

### 8.5.3 Limitations and hardware configuration

Limitations: DFSDM Audio and USB HS

Hardware modifications:

- Fit R201, R202, R205, R208, and R33.
- Remove the MB1299 DFSDM audio module.

## 8.6 OCSPI NOR Flash 2 module (MB1242)

### 8.6.1 Description

CN11 (left) and CN10 (right) allow connecting MB1242 modules. Different versions of this module support ICs part numbers described in Table 54 and Table 55. These connectors are connected to OCSPI2 interface of STM32H7B3LIH6QU on the STM32H7B3I-EVAL Evaluation board.

WARNING: Due to board design, as OCSPI2 interface is “shared” with SDRAM and camera, it can only be tested at low speed (Maximum: 50 MHz).

**Table 54. OCSPI / HYPERBUS supported part numbers on MB1242**

| Manufacturer | Reference | Memory type | Voltage | Size |
|---|---|---|---|---|
| MACRONIX | MX25LM51245G | OCTAL Flash | 3 V | 512-Mbit |
| CYPRESS | S26KL512DPBHI02 | HYPERFLASH | 3 V | 512-Mbit |
| ISSI | IS66WVH8M8BLL-100B1LI | HYPERRAM | 3 V | 64-Mbit |
| JSC | JSC64SSU8AGDY-75M | OCTAL RAM | 3 V | 64-Mbit |
| MICRON | MT35XL512ABA1G12 | Xccela Flash | 3 V | 512-Mbit |
| CYPRESS | S71KL512SC0BHI00 | HYPER COMBO FLASH / RAM | 3 V | 512-Mbit Flash 64-Mbit RAM |
| CYPRESS | S27KL0641DABHI020 | HYPERRAM | 3 V | 64-Mbit |
| MACRONIX | MX65L12A64AAXDR00 | COMBO FLASH / RAM | 3 V | 512-Mbit Flash 64-Mbit RAM |
| AP Memory | APS6408L-3OB-BA | | 3 V | 64-Mbit |
| MACRONIX | MX25LW51245G | OCTAL Flash RWW | 3 V | 512-Mbit |
| MACRONIX | MX46LP6408AXDR00 | OCTAL RAM | 3 V | 64-Mbit |

**Table 55. QSPI / Dual QSPI supported part numbers on MB1242**

| Manufacturer | Reference | Memory type | Voltage | I/O | Size |
|---|---|---|---|---|---|
| MACRONIX | MX66L1G85GXDI | Dual QSPI | 3 V | Fixed | 1-Gbit |
| CYPRESS | S79FL01GSDSBHVC1 | Dual QSPI | 3 V | Fixed | 1-Gbit |

### 8.6.2 Operating voltage

STM32H7B3LIH6QU OCSPI2 interface can only be at 3.3 V on this board.

### 8.6.3 Limitations and hardware configuration

Limitations with primary functions: camera, SDRAM (Refer to jumper configuration below)

Limitations with secondary functions: NOR, SRAM, and SDIO2

Hardware modifications are listed in Table 56 below:

**Table 56. OCSPI2 hardware configuration**

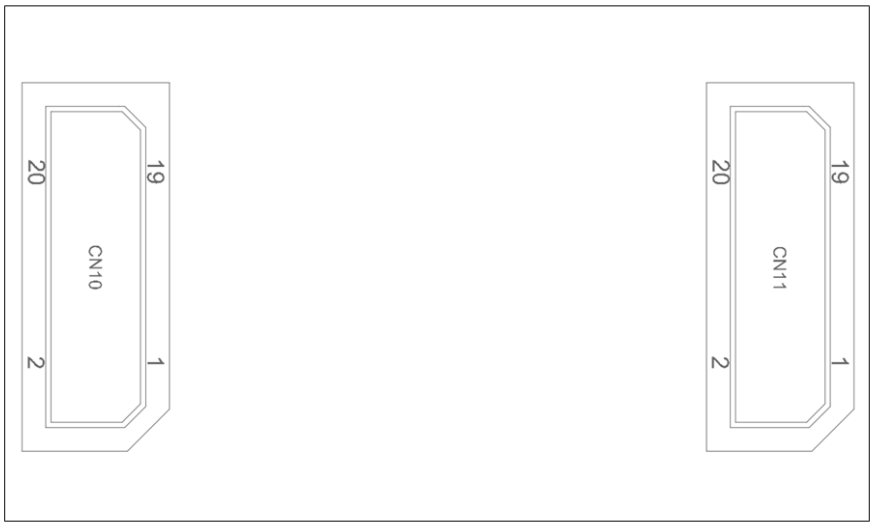
| Signal name | Pin name | Setting | OCSPI2[1] |
|---|---|---|---|
| FMC_A0 | PF0 | R339 | OFF[2] |
| OCSPI2_IO0 | | R98 | **ON** |
| FMC_A1 | PF1 | R335 | OFF[2] |

| Signal name | Pin name | Setting | OCSPI2[1] |
|---|---|---|---|
| OCSPI2_IO1 | (Continued) PF1 | R89 | **ON** |
| FMC_A2 | PF2 | R331 | OFF[2] |
| OCSPI2_IO2 | | R82 | **ON** |
| FMC_A3 | PF3 | R74 | OFF[2] |
| OCSPI2_IO3 | | R75 | **ON** |
| FMC_A10 | PG0 | R73 | OFF[2] |
| OCSPI2_IO4 | | R76 | **ON** |
| FMC_A11 | PG1 | R333 | OFF[2] |
| OCSPI2_IO5 | | R77 | **ON** |
| FMC_A4 | PF4 | R66 | OFF[2] |
| OCSPI2_CLK | | R319 | **ON** |
| FMC_A5 | PF5 | R65 | OFF[2] |
| OCSPI2_NCLK | | R318 | **ON** |
| FMC_NE3 | PG10[3] | JP2 | OFF |
| SDIO2_D1 | | | |
| DCMI_D2 | | R118 | OFF[2] |
| OCSPI2_IO6 | | R115 | **ON** |
| SDIO2_D2 | PG11[3] | JP1 | OFF |
| DCMI_D3 | | JP1 | OFF |
| OCSPI2_IO7[2] | | R257 | **ON** |
| SDIO2_D3 | PG12[3] | JP13 | OFF |
| OCSPI2_NCS[2] | | R287 | **ON** |
| FMC_SDNCAS | PG15 | R352 | OFF[2] |
| OCSPI2_DQS | | R354 | **ON** |
| 3V3_SW_ENABLE | **MFX IO0**[3] | SB34 | **ON** |

1. *The default configuration is in bold.*
2. *Remove to avoid stub if necessary.*
3. *PG10, PG11, PG12 signals are using pins supplied by VDDMMC. Make sure to supply 3.3 V on VDDMMC (Refer to Section 6.3.5 )*

### 8.6.4 Interface

Figure 32. **MB1242 OCSPI module connectors CN10 and CN11**




Find CN10 (Left) pin-out in Table 57.

Table 57. **CN10 (Left) MB1242 pin-out**

| Pin number | Description | Pin connection | Pin number | Description | Pin connection |
|---|---|---|---|---|---|
| 1 | OCSPI2_NCS | PG12 | 2 | 3V3_AO | 3V3_AO |
| 3 | OCSPI2_IO0 | PF0 | 4 | 3V3_AO | 3V3_AO |
| 5 | OCSPI2_IO1 | PF1 | 6 | OCSPI1_NCS | PG6 |
| 7 | OCSPI2_IO2 | PF2 | 8 | OCSPI2_IO4 | PG0 |
| 9 | OCSPI2_IO3 | PF3 | 10 | OCSPI2_IO5 | PG1 |
| 11 | OCSPI2_DQS | PG15 | 12 | OCSPI2_IO6 | PG10 |
| 13 | GND | GND | 14 | OCSPI2_IO7 | PG11 |
| 15 | OCSPI2_CLK_N | PF5 | 16 | OCSPI2_RESET | NRST |
| 17 | OCSPI2_CLK_P | PF4 | 18 | GND | GND |
| 19 | GND | GND | 20 | GND | GND |

Find CN11 (Right) pin-out in Table 58.

Table 58. **CN11 (Right) MB1242 pin-out**

| Pin number | Description | Pin connection | Pin number | Description | Pin connection |
|---|---|---|---|---|---|
| 1 | 3V3_AO | 3V3_AO | 2 | 3V3_AO | 3V3_AO |
| 3 | 3V3_AO | 3V3_AO | 4 | 3V3_AO | 3V3_AO |
| 5 | NC | NC | 6 | NC | NC |
| 7 | NC | NC | 8 | NC | NC |

| Pin number | Description | Pin connection | Pin number | Description | Pin connection |
|---|---|---|---|---|---|
| 9 | NC | NC | 10 | NC | NC |
| 11 | NC | NC | 12 | NC | NC |
| 13 | RFU2 test point | NC | 14 | RFU1 test point | NC |
| 15 | RSTOUTn test point | NC | 16 | INTn test point | NC |
| 17 | GND | GND | 18 | GND | GND |
| 19 | GND | GND | 20 | GND | GND |

## 8.7 CAN FD

### 8.7.1 Description

The STM32H7B3I-EVAL Evaluation board supports one channel of flexible data rate CAN, CAN-FD-compliant bus communication based on 3.3 V CAN transceiver.

To use CAN FD, fit SB36 and SB35 solder bridges (And remove these solder bridges when using USB OTG FS, to avoid stubs).

Standby signal on CAN-FD transceiver is controlled by MFX IO9.

### 8.7.2 Operating voltage

STM32H7B3LIH6QU CAN-FD interface can only be at 3.3 V on this board. The CAN-FD MCP2562FDT-H/SN transceiver (U28) requires 5 V on the VDD pin.

### 8.7.3 Limitations and hardware configuration

Limitation with primary function USB OTG FS

### 8.7.4 Interface

**Figure 33. CAN D-type 9-pin male connector CN22**

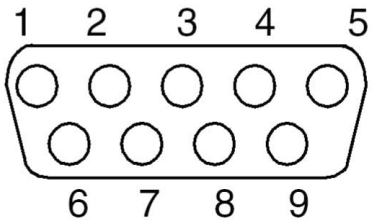



**Table 59. CN10 (Left) MB1242 pin-out**

| Pin number | Description | Pin number | Description |
|---|---|---|---|
| 1,4,8,9 | NC | 7 | CANH |
| 2 | CANL | 3,5,6 | GND |

## 8.8 Motor control

### 8.8.1 Description

Motor-control functions can be accessed:

- Either through the 17x2 legacy connector CN1,
- or through the 10x2 DFSDM connector CN4.

### 8.8.2 Operating voltage

The STM32H7B3LIH6QU motor-control interfaces (Such as GPIO, PWM, and ADC) can only be at 3.3 V on this board.

### 8.8.3 Limitations and hardware configuration

Limitations with primary functions: USB FS, Wi-Fi®, SD card 1, camera, audio I2S6, SDRAM, OCSPI1

Limitations with secondary functions: audio SAI, USB HS, NOR, SRAM, TRACE, KEY WKUP, MCO1, 3V3_SW_ENABLE and 1V8_SW_ENABLE

### 8.8.4 Interface

**Figure 34. Motor-control legacy connector CN1**

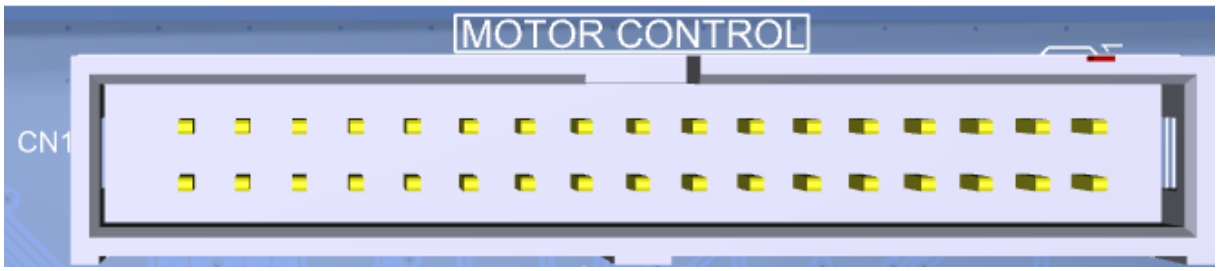



**Table 60. Motor-control legacy connector CN1 (17x2)**

| Pin name | Fitted | Not fitted | MCU function | Motor-control function |
|---|---|---|---|---|
| PF12 | R72 | R326 | ADC1_INP6 | BUS VOLTAGE |
| PC0 | R253 | R255 | ADC12_INP10 | PHASE A CURRENT |
| PC1 | R210 | R216 | ADC12_INP11 | PHASE B CURRENT |
| PC4 | R277 | R281 | ADC12_INP4 | PFC INDUCTOR CURRENT |
| PA7 | R67 | R322 | ADC12_INP7 | PHASE C CURRENT |
| PC5 | R282 | R286 | ADC12_INP8 | PFC VAC |
| PC3_C | R219 | | ADC2_INP1 | HEATSINK TEMPERATURE |
| MFX_GPO6 | SB33 / R130 | R129 | GPIO1 | ICL SHUT OUT |
| MFX_GPO7 | SB30 / R99 | R100 | GPIO2 | DISSIPATIVE BREAK |
| PD4 | R367 | R368 | INT_JOY_DOWN | JOYSTICK DOWN |
| PA4 | - | JP7 | | |
| PD5 | R363 | R364 | INT_JOY_LEFT | JOYSTICK LEFT |
| PI0 | R386 | R128 | INT_JOY_RIGHT | JOYSTICK RIGHT |
| PI9 | R360 | R351 | INT_JOY_SEL | JOYSTICK SEL |
| PH13 | R389 | R131 | INT_JOY_UP | JOYSTICK UP |
| PA8 | R301 | R308 | TIM1_CH1 | PWM_1H |

| Pin name | Fitted | Not fitted | MCU function | Motor-control function |
|---|---|---|---|---|
| PE8 | R81 | R96 | TIM1_CH1N | PWM_1L |
| PA9 | R294 | R60 | TIM1_CH2 | PWM_2H |
| PB14 | R304 | R307 | TIM1_CH2N | PWM_2L |
| PA10 | R288 | R58 | TIM1_CH3 | PWM_3H |
| PB15 | R309 | R311 | TIM1_CH3N | PWM_3L |
| PD2 | R278 | R49 | TIM15_BKIN | PFC SHUTDOWN |
| PE6 | R330 | JP27 / R78 / R334 | TIM15_CH2 | PFC PWM |
| PA0 | R213 | R229 / C30 | TIM2_CH1 | ENCODER A |
| PA1 | R235 | R236 | TIM2_CH2 | ENCODER B |
| PA2 | R239 | R240 | TIM2_CH3 | ENCODER C |
| PA6 | R349 | JP6 | TIM1_BKIN | EMERGENCY STOP |
| PE5 | R323 | R69 / R71 / JP28 | TIM15_CH1 | PFC SYNC |
| PA3 | R258 | R236 | LCD_BL_CTRL BACK-UP | LCD_BL_CTRL BACK-UP |

**Figure 35. Motor-control legacy connector CN4**

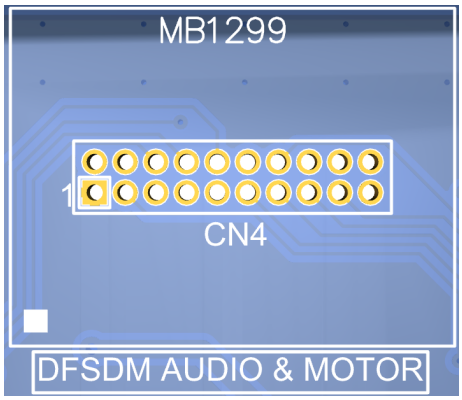



**Table 61. Motor-control DFSDM connector CN4 (10x2)**

| Pin name | Fitted | Not fitted | MCU function | Motor-control function |
|---|---|---|---|---|
| PC0 | R253 | R255 | DFSDM_1_CKIN0 | MOTOR_DFSDM_1_CKIN0 |
| PC1 | R210 | R216 | DFSDM_1_DATIN0 | MOTOR_DFSDM_1_DATIN0 |
| PC4 | R277 | R281 | DFSDM1_CKIN2 | MOTOR_DFSDM1_CKIN2 |
| PC5 | R282 | R286 | DFSDM_1_DATIN2 | MOTOR_DFSDM_1_DATIN2 |
| PB13 | R314 | R316 | DFSDM1_CKIN1_DFSDM2_CKIN1 | MOTOR_DFSDM1_CKIN1_DFSDM2_CKIN1 |
| PD8 | R123 | R384 | DFSDM1_CKIN3 | MOTOR_DFSDM1_CKIN3 |
| PD6 | R284 | R285 | DFSDM1_CKIN4 | MOTOR_DFSDM1_CKIN4 |

| Pin name | Fitted | Not fitted | MCU function | Motor-control function |
|---|---|---|---|---|
| PB7 | R238 | R29 | DFSDM1_CKIN5 | MOTOR_DFSDM1_CKIN5 |
| PB8(1) | - | - | DFSDM1_CKIN7 | MOTOR_DFSDM1_CKIN7 |
| PB12 | JP19 [1-2] | - | DFSDM1_DATIN1 | MOTOR_DFSDM1_DATIN1 |
| PC7 | JP35 [2-3] | - | DFSDM1_DATIN3 | MOTOR_DFSDM1_DATIN3 |
| PE10 | R95 | R341 | DFSDM1_DATIN4 | MOTOR_DFSDM1_DATIN4 |
| PB6 | - | - | DFSDM1_DATIN5 | MOTOR_DFSDM1_DATIN5 |
| PB9(1) | R233 | - | DFSDM1_DATIN7 | MOTOR_DFSDM1_DATIN7 |
| PD4 | R367 | R368 | INT_JOY_DOWN | JOYSTICK DOWN |
| PA4 | | JP7 | | |
| PD5 | R363 | R364 | INT_JOY_LEFT | JOYSTICK LEFT |
| PI0 | R386 | R128 | INT_JOY_RIGHT | JOYSTICK RIGHT |
| PI9 | R360 | R351 | INT_JOY_SEL | JOYSTICK SEL |
| PH13 | R389 | R131 | INT_JOY_UP | JOYSTICK UP |
| PA3 | R258 | R236 | LCD_BL_CTRL BACK-UP | LCD_BL_CTRL BACK-UP |

1. *PB8 and PB9 signals are supplied by VDDMMC. Make sure to supply 3.3V on VDDMMC (Refer to Section 6.3.5 )*

## 8.9 FMC memory extension connectors CN12 and CN13

All signals for memory are also connected to memory connectors CN12 and CN13 for memory daughterboards.

Two 40-pin male headers CN12 and CN13 are used to connect with the memory daughterboard. GPIOs which work as FMC memory signals and don't on CN5 and CN6 are available on these two connectors.

The space between these two connectors is defined as a standard that allows developing common daughterboards. The standard width between CN13 pin1 and CN12 pin1 is 1914 mils (48.62 mm). For signal-assignment details, refer to Table 62, Table 63, Table 64, and Table 65.

**Table 62. Memory connector CN12 left odd pins**

| Pin number | Pin name | STM32H7B3I-EVAL pin name | How to disconnect with function block on STM32H7B3I-EVAL board |
|---|---|---|---|
| 1 | PH6 | FMC_SDR_SDNE1 | R68 |
| 3 | PF13 | FMC_A7 | R325 |
| 5 | PF12(1) | FMC_A6 \|\| MOTOR_ADC1_INP6 | R326 |
| 7 | PG1(1) | FMC_A11 \|\| OCSPI2_IO5 | R333 |
| 11 | PE7 | FMC_D4 | R338 |
| 13 | PE10(1) | FMC_D7 \|\| MOTOR_DFSDM1_DATIN4 | R341 |
| 15 | PE12 | FMC_D9 | R345 |
| 17 | PE15 | FMC_D12 | R348 |
| 19 | PE13 | FMC_D10 | R353 |
| 21 | PD11 | FMC_A16 | R359 |
| 23 | PD12 | FMC_A17 | R362 |
| 25 | PG5 | FMC_A15 | R366 |
| 27 | PH11 | FMC_D19 | R370 |
| 31 | PD13 | FMC_A18 | R375 |
| 33 | PG2 | FMC_A12 | R380 |
| 35 | PD8(1) | FMC_D13 \|\| MOTOR_DFSDM1_CKIN3 | R384 |
| 37 | PD9 | FMC_D14 | R385 |
| 39 | PD14 | FMC_D0 | R391 |

1. *Pins shared between different functions and requiring hardware configuration (Such as jumper and soldered bridges)*

**Table 63. Memory connector CN12 left even pins**

| Pin number | Pin name | STM32H7B3I-EVAL pin name | How to disconnect with function block on STM32H7B3I-EVAL board |
|---|---|---|---|
| 2 | PA7(1) | FMC_SDR_SDNWE \|\| MOTOR_ADC12_INP7 | R322 |
| 4 | PF14 | FMC_A8 | R70 |
| 6 | PG0(1) | FMC_A10 \|\| OCSPI2_IO4 | R73 |

| Pin number | Pin name | STM32H7B3I-EVAL pin name | How to disconnect with function block on STM32H7B3I-EVAL board |
|---|---|---|---|
| 8 | PF11 | FMC_SDR_SDNRAS | R332 |
| 12 | PE9 | FMC_D6 | R87 |
| 14 | PE8(1) | FMC_D5 \|\| MOTOR_TIM1_CH1N | R96 |
| 16 | PE11 | FMC_D8 | R102 |
| 18 | PF15 | FMC_A9 | R103 |
| 20 | PE14 | FMC_D11 | R105 |
| 22 | PH8 | FMC_D16 | R358 |
| 24 | PH10 | FMC_D18 | R361 |
| 26 | PH9 | FMC_D17 | R365 |
| 28 | PG4 | FMC_A14 | R369 |
| 32 | PH12 | FMC_D20 | R371 |
| 34 | PG3 | FMC_A13 | R374 |
| 36 | PD10 | FMC_D15 | R381 |
| 38 | PD15 | FMC_D1 | R127 |
| 40 | PG8 | FMC_SDR_SDCLK | R132 |

1. *Pins shared between different functions and requiring hardware configuration (Such as jumper and soldered bridges)*

**Table 64. Memory connector CN13 right odd pins**

| Pin number | Pin name | STM32H7B3I-EVAL pin name | How to disconnect with function block on STM32H7B3I-EVAL board |
|---|---|---|---|
| 1 | PF5(1) | FMC_A5 \|\| OCSPI2_NCLK | R65 |
| 3 | PF4(1) | FMC_A4 \|\| OCSPI2_CLK | R66 |
| 5 | PF3(1) | FMC_A3 \|\| OCSPI2_IO3 | R74 |
| 7 | PE6(1) | WIFI_SPI4_MOSI \|\| SAI1_SD_A \|\| FMC_A22 \|\| TRACED3 \|\| MOTOR_TIM15_CH2 | R334 |
| 11 | PE4(1) | DCMI_D4 \|\| SAI1_FS_A \|\| FMC_A20 \|\| TRACED1 | R116 |
| 13 | PE3(1) | WIFI_SPI4_NSS \|\| SAI1_SD_B \|\| FMC_A19 \|\| TRACED0 | R337 |
| 15 | PI5 | FMC_NBL3 | R344 |
| 17 | PI4 | FMC_NBL2 | R350 |
| 19 | PG15(1) | FMC_SDNCAS \|\| OCSPI2_DQS | R352 |
| 21 | PI10 | FMC_D31 | R357 |
| 23 | PE1 | FMC_NBL1 | R114 |
| 25 | PE0 | FMC_NBL0 | R117 |
| 27 | PG10(1) | DCMI_D2 \|\| FMC_NE3 \|\| SDIO2_D1 \|\| OCSPI2_IO6 | R280 |
| 31 | PD0 | FMC_D2 | R119 |

| Pin number | Pin name | STM32H7B3I-EVAL pin name | How to disconnect with function block on STM32H7B3I-EVAL board |
|---|---|---|---|
| 33 | PI2 | FMC_D26 | R121 |
| 35 | PI1 | FMC_D25 | R124 |
| 37 | PI0(1) | FMC_D24 \|\| MOTOR_INT_JOY_RIGHT | R128 |
| 39 | PH13(1) | FMC_D21 \|\| MOTOR_INT_JOY_UP | R131 |

1. *Pins shared between different functions and requiring hardware configuration (Such as jumper and soldered bridges)*

**Table 65. Memory connector CN13 right even pins**

| Pin number | Pin name | STM32H7B3I-EVAL pin name | How to disconnect with function block on STM32H7B3I-EVAL board |
|---|---|---|---|
| 2 | PH7 | FMC_SDR_SDCKE1 | R320 |
| 4 | PE5(1) | WIFI_SPI4_MISO \|\| SAI1_SCK_A \|\| FMC_A21 \|\| TRACED2 \|\| MOTOR_TIM15_CH1 | R69 |
| 6 | PC6(1) | DCMI_D0 \|\| FMC_NOR_NWAIT | JP32 |
| 8 | PF2(1) | FMC_A2 \|\| OCSPI2_IO2 | R331 |
| 12 | PF1(1) | FMC_A1 \|\| OCSPI2_IO1 | R335 |
| 14 | PF0(1) | FMC_A0 \|\| OCSPI2_IO0 | R339 |
| 16 | PE2(1) | WIFI_SPI4_SCK \|\| FMC_A23 \|\| TRACECLK | R343 |
| 18 | PI7 | FMC_D29 | R347 |
| 20 | PI9(1) | FMC_D30 \|\| MOTOR_INT_JOY_SEL | R351 |
| 22 | PI6 | FMC_D28 | R356 |
| 24 | PC7(1) | DCMI_D1 \|\| FMC_NOR_NE1 \|\| DFSDM1_DATIN3 | JP35 |
| 26 | PD5(1) | FMC_NWE \|\| MOTOR_INT_JOY_LEFT | R364 |
| 28 | PD4(1) | FMC_NOE \|\| MOTOR_INT_JOY_DOWN | R368 |
| 32 | PD1 | FMC_D3 | R373 |
| 34 | PI3 | FMC_D27 | R378 |
| 36 | PH15 | FMC_D23 | R382 |
| 38 | PH14 | FMC_D22 | R387 |

1. *Pins shared between different functions and requiring hardware configuration (Such as jumper and soldered bridges)*

## 8.10 Daughterboard extension connectors CN5 and CN6

Two 60-pin male headers CN5 and CN6 can be used to connect with a daughterboard or a standard wrapping board to the STM32H7B3I-EVAL Evaluation board. All GPIOs are available on them and memory connectors (CN12 and CN13).

The space between these two connectors is defined as a standard, which allows developing common daughterboards for several ST evaluation boards. The standard width between CN6 pin1 and CN5 pin1 is 2700 mils (68.58 mm). Each pin on CN5 and CN6 can be used by a daughterboard after disconnecting it from the corresponding function block on the STM32H7B3I-EVAL Evaluation board. Refer to Table 66, Table 67, Table 68, and Table 69 for details.

**Table 66. Daughterboard extension connector CN6 left odd pins**

| Pin number | Pin name | Pin function | How to disconnect |
|---|---|---|---|
| 1 | PC1 | OCSPI1_IO4 \|\| MOTOR_ADC12_INP11 \|\| MOTOR_DFSDM_1_DATIN0 | R216 |
| 3 | PH0 | OSC_IN | R21 / SB7 |
| 5 | NRST | NRST | SB13 / SB21 / SB38 / SB45 / R225 / R218 / JP24 |
| 7 | PF7 | OCSPI1_IO2 | R230 |
| 9 | PF6 | OCSPI1_IO3 | R234 |
| 11 | PF8 | OCSPI1_IO0 | R237 |
| 13 | PF9 | OCSPI1_IO1 | R241 |
| 15 | PC2 | ULPI_DIR | R245 |
| 17 | PB6 | DFSDM1_DATIN5 | R33 |
| 21 | PA4 | DCMI_HSYNC \|\| I2S6_WS \|\| INT_BKUP_USB_OTG_HS_OVRCR | JP7 |
| 23 | PC3 | ULPI_NXT | R261 |
| 25 | PH2 | CTP_INT | |
| 27 | PH3 | OCSPI1_IO5 | R272 |
| 29 | PH4 | I2C_SCL | R275 |
| 31 | PA5 | I2S6_CK \|\| ULPI_CK | JP11 |
| 33 | PC4 | CTP_RST \|\| MOTOR_ADC12_INP4 \|\| MOTOR_DFSDM1_CKIN2 | R281 |
| 35 | PC5 | OCSPI1_DQS \|\| MOTOR_ADC12_INP8 \|\| MOTOR_DFSDM_1_DATIN2 | R286 |
| 37 | PI15 | RGB_LCD_R0 | R290 |
| 41 | PJ0 | RGB_LCD_R1 | R293 |
| 43 | PB1 | ULPI_D2 | R296 |
| 45 | PI11 | INT_uSDCard_Detect2 | R297 |
| 47 | PG14 | OCSPI1_IO7 | R300 |
| 51 | PG9 | DCMI_VSYNC/RDY \|\| SDIO2_D0 | JP17 |
| 53 | PA8 | MCO1 \|\| USB_OTG_HS_CLK_BKUP \|\| MOTOR_TIM1_CH1 | R308 |
| 55 | PJ5 | RGB_LCD_R6 | R313 |
| 57 | PG6 | OCSPI1_NCS \|\| SD_LDO_SEL | JP23 |

**Table 67. Daughterboard extension connector CN6 left even pins**

| Pin number | Pin name | Pin function | How to disconnect |
|---|---|---|---|
| 2 | PC2_C | FREE ADC | |
| 4 | PC3_C | MOTOR_ADC2_INP1 | R219 |
| 6 | PH1 | OSC_OUT | R20 / SB6 |
| 8 | PA0 | KEY_WKUP0 \|\| MOTOR_TIM2_CH1 | R229 |
| 12 | PA1 | LCD_BL_CTRL \|\| MOTOR_TIM2_CH2 | R236 |
| 14 | PA2 | LCD_RESET \|\| MOTOR_TIM2_CH3 \|\| BOOTLOADER_VCP_TX | JP40 |
| 16 | PA0_C | Potentiometer \|\| ADC_IN_P | R244 |
| 18 | PA1_C | ADC_IN_N | R250 |
| 20 | PC0 | ULPI_STP \|\| MOTOR_ADC12_INP10 \|\| MOTOR_DFSDM_1_CKIN0 | R255 |
| 22 | PG11 | DCMI_D3 \|\| SDIO2_D2 \|\| OCSPI2_IO7 | JP1 |
| 24 | PH5 | I2C_SDA | R35 |
| 26 | PA3 | I2S6_MCK \|\| ULPI_D0 \|\| MOTOR_LCD_BL_CTRL_BKUP \|\| BOOTLOADER_VCP_RX | JP39 |
| 28 | PB0 | DFSDM1_CKOUT \|\| DFSDM2_CKOUT \|\| ULPI_D1 | R271 |
| 32 | PB2 | OCSPI1_CLK | R283 |
| 34 | PG12 | SDIO2_D3 \|\| OCSPI2_NCS | R122 |
| 36 | PD6 | OCSPI1_IO6 \|\| SDIO2_CK \|\| MOTOR_DFSDM1_CKIN4 | JP4 |
| 38 | PD7 | SDIO2_CMD | R289 |
| 40 | PJ3 | RGB_LCD_R4 | R291 |
| 42 | PB10 | ULPI_D3 | R292 |
| 44 | PB11 | ULPI_D4 | R295 |
| 46 | PB5 | I2S6_SD \|\| ULPI_D7 | JP18 / JP16 |
| 52 | PB12 | DFSDM1_DATIN1 \|\| DFSDM2_DATIN1 \|\| ULPI_D5 | JP19 |
| 54 | PB14 | VCP+WIFI_USART1_TX \|\| BL_USART1_TX \|\| MOTOR_TIM1_CH2N | JP21 |
| 56 | PB15 | VCP+WIFI_USART1_RX \|\| BL_USART1_RX \|\| MOTOR_TIM1_CH3N | JP20 |
| 58 | PB13 | ULPI_D6 \|\| MOTOR_DFSDM1_CKIN1_DFSDM2_CKIN1 | R316 |

**Table 68. Daughterboard extension connector CN5 right odd pins**

| Pin number | Pin name | Pin function | How to disconnect |
|---|---|---|---|
| 1 | PI12 | RGB_LCD_HSYNC | R215 |
| 3 | PC15 | OSC32_OUT | R24 |
| 5 | PI14 | RGB_LCD_CLK | R226 |
| 7 | PF10 | INT_uSDCard_Detect1 | JP4 |
| 9 | PB9(1) | DCMI_D7 \|\| DFSDM1_DATIN7 | R104 |
| 11 | PB8(1) | DCMI_D6 \|\| MEMS_LED \|\| MOTOR_DFSDM1_CKIN7 | R110 |
| 13 | PB7(1) | INT_USB_OTG_FS_OVRCR \|\| MOTOR_DFSDM1_CKIN5 | R29 |
| 15 | PK6 | RGB_LCD_B7 | R243 |
| 17 | PK5 | RGB_LCD_B6 | R249 |

| Pin number | Pin name | Pin function | How to disconnect |
|---|---|---|---|
| 21 | PK3 | RGB_LCD_B4 | R256 |
| 23 | PJ2 | RGB_LCD_R3 | R260 |
| 25 | PJ4 | RGB_LCD_R5 | R265 |
| 27 | PJ1 | RGB_LCD_R2 | R270 |
| 29 | PJ15 | RGB_LCD_B3 | R276 |
| 31 | PD2(1) | SDIO1_CMD \|\| MOTOR_TIM15_BKIN | R49 |
| 33 | PC12 | SDIO1_CK | R54 |
| 35 | PC10 | SDIO1_D2 | R56 |
| 37 | PA14 | JTCK-SWCLK | R59 |
| 41 | PA12(1) | USB_FS1_DP \|\| FDCAN1_TX | R61 |
| 43 | PA11(1) | USB_FS1_DM \|\| FDCAN1_RX | R63 |
| 45 | PC9 | SDIO1_D1 | R62 |
| 47 | PK1 | RGB_LCD_G6 | R299 |
| 51 | PK2 | RGB_LCD_G7 | R303 |
| 53 | PJ8 | RGB_LCD_G1 | R306 |
| 55 | PJ9 | RGB_LCD_G2 | R310 |
| 57 | PJ7(1) | RGB_LCD_G0 \|\| TRGIN | R315 |

1. *Pins shared between different functions and requiring hardware configuration (Such as jumper and soldered bridges)*

**Table 69. Daughterboard extension connector CN5 right even pins**

| Pin number | Pin name | Pin function | How to disconnect |
|---|---|---|---|
| 2 | PI13 | RGB_LCD_VSYNC | R214 |
| 4 | PC14 | OSC32_IN | R23 |
| 6 | PC13(1) | KEY_TAMP_1/WKUP2 | R16 |
| 8 | PI8 | INT_MFX_IRQ_OUT | R168 |
| 12 | PA6(1) | DCMI_PIXCLK \|\| I2S6_EXT_SD_BKUP \|\| MOTOR_TIM1_BKIN | JP6 |
| 14 | PB4(1) | I2S6_EXT_SD \|\| NJTRST | JP8 |
| 16 | PB3 | JTDO/TRACESWO | R32 |
| 18 | PK7 | RGB_LCD_DE | R248 |
| 20 | PK4 | RGB_LCD_B5 | R254 |
| 22 | PG13 | LED1 | R178 |
| 24 | PJ12(1) | RGB_LCD_B0 \|\| TRGOUT | R259 |
| 26 | PJ13 | RGB_LCD_B1 | R264 |
| 28 | PJ14 | RGB_LCD_B2 | R269 |
| 32 | PD3 | DCMI_D5 | R48 |
| 34 | PC11 | SDIO1_D3 | R51 |
| 36 | PA15 | JTDI | R53 |
| 38 | PA13 | JTMS-SWDIO | R57 |
| 40 | PA10(1) | USB_FS_ID \|\| MOTOR_TIM1_CH3 | R58 |

| Pin number | Pin name | Pin function | How to disconnect |
|---|---|---|---|
| 42 | PA9(1) | USB_FS_VBUS \|\| MOTOR_TIM1_CH2 | R60 |
| 44 | PC8(1) | SDIO1_D0 \|\| SRAM_BKUP_NE3 | JP12 |
| 46 | PG7 | SAI1_MCLK_A | JP14 |
| 52 | PJ11 | RGB_LCD_G4 | R302 |
| 54 | PK0 | RGB_LCD_G5 | R305 |
| 56 | PJ10 | RGB_LCD_G3 | R312 |
| 58 | PJ6 | RGB_LCD_R7 | R317 |

1. *Pins shared between different functions and requiring hardware configuration (Such as jumper and soldered bridges)*

# Appendix A STM32H7B3I-EVAL I/O Assignment

**Table 70. STM32H7B3I-EVAL I/O Assignment**

| LQFP144 pinout | Pin name | Main function pinout assignment | Optional function pinout assignment | Motor-control connector |
|---|---|---|---|---|
| 1 | PE2 | TRACE_CLK | - | - |
| 2 | PE3 | SRAM-FMC_A19 | - | - |
| 3 | PE4 | SRAM-FMC_A20 | - | - |
| 4 | PE5 | TRACE_D2 | - | - |
| 5 | PE6 | LCD_RS_FMC_A22 | TRACE_D3 | - |
| 6 | VBAT | POWER | - | - |
| 7 | PC13 | User Button WKUP2 | TAMPER KEY | - |
| 8 | PC14 | OSC32_IN | - | - |
| 9 | PC15 | OSC32_OUT | - | - |
| 10 | PF0 | SRAM-FMC_A0 | - | - |
| 11 | PF1 | SRAM-FMC_A1 | - | - |
| 12 | PF2 | SRAM-FMC_A2 | - | - |
| 13 | PF3 | SRAM-FMC_A3 | - | - |
| 14 | PF4 | SRAM-FMC_A4 | - | - |
| 15 | PF5 | SRAM-FMC_A5 | - | - |
| 16 | VSS | POWER | - | - |
| 17 | VDD | POWER | - | - |
| 18 | PF6 | Audio SAI1_SD_B | - | - |
| 19 | PF7 | Audio SAI1_MCLK_B | - | - |
| 20 | PF8 | Audio SAI1_SCK_B | - | - |
| 21 | PF9 | Audio SAI1_FS_B | - | TIM15_CH1 |
| 22 | PF10 | DFSDM1_CKOUT | STMOD+ DFSDM | TIM15_CH2 |
| 23 | PH0 | OSC_IN | - | - |
| 24 | PH1 | OSC_OUT | - | - |
| 25 | NRST | NRST | - | - |
| 26 | PC0 | OCTOSPI_IO7 | - | ADC12_IN1 |
| 27 | PC1 | OCTOSPI_IO4 | - | ADC12_IN2 |
| 28 | PC2 | OCTOSPI_IO5 | - | ADC12_IN3 |
| 29 | PC3 | OCTOSPI_IO6 | - | ADC12_IN4 |
| 30 | VSSA | POWER | - | - |
| 31 | VREFP | POWER | - | - |
| 32 | VDDA | POWER | - | - |
| 33 | PA0 | MFX_IRQ_OUT | OPAMP1_VINP, STMOD+_ADC12_IN5 | ADC12_IN5<br>TIM2_CH1 |
| 34 | PA1 | TAMPER KEY | OPAMP1_VINM<br>STMOD+_PMOD_INT | ADC12_IN6<br>TIM2_CH2 |

| LQFP144 pinout | Pin name | Main function pinout assignment | Optional function pinout assignment | Motor-control connector |
|---|---|---|---|---|
| 35 | PA2 | OCTOSPI_NCS | - | ADC12_IN7<br>TIM2_CH3 |
| 36 | PA3 | OCTOSPI_CLK | OPAMP1_VOUT | ADC12_IN8 |
| 37 | VSS | POWER | - | - |
| 38 | VDD | POWER | - | - |
| 39 | PA4 | UCPD_ADC12_IN9 | ADC12_IN9/DAC1_OUT1<br>STMOD+_SPI3_NSS<br>PMOD_SPI3_NSS | ADC12_IN9 |
| 40 | PA5 | LCD_BL_CTRL TIM2_CH1 | STMOD+_TIM2_CH1 | - |
| 41 | PA6 | OCTOSPI_IO3 | - | ADC12_IN11 |
| 42 | PA7 | OCTOSPI_IO2 | - | TIM8_CH1N |
| 43 | PB0 | OCTOSPI_IO1 | - | TIM8_CH2N |
| 44 | PB1 | OCTOSPI_IO0 | - | TIM8_CH3N |
| 45 | PB2 | OCTOSPI_DQS | - | I/O |
| 46 | PF11 | OCTOSPI_NCLK | - | - |
| 47 | PF12 | SRAM-FMC_A6 | - | - |
| 48 | VSS | POWER | - | - |
| 49 | VDD | POWER | - | - |
| 50 | PF13 | SRAM-FMC_A7 | - | - |
| 51 | PF14 | SRAM-FMC_A8 | - | - |
| 52 | PF15 | SRAM-FMC_A9 | - | - |
| 53 | PG0 | SRAM-FMC_A10 | - | - |
| 54 | PG1 | SRAM-FMC_A11 | - | - |
| 55 | PE7 | LCD-SRAM-FMC_D4 | - | - |
| 56 | PE8 | LCD-SRAM-FMC_D5 | - | - |
| 57 | PE9 | LCD-SRAM-FMC_D6 | - | - |
| 58 | VSS | POWER | - | - |
| 59 | VDD | POWER | - | - |
| 60 | PE10 | LCD-SRAM-FMC_D7 | - | - |
| 61 | PE11 | LCD-SRAM-FMC_D8 | - | - |
| 62 | PE12 | LCD-SRAM-FMC_D9 | - | - |
| 63 | PE13 | LCD-SRAM-FMC_D10 | - | - |
| 64 | PE14 | LCD-SRAM-FMC_D11 | - | - |
| 65 | PE15 | LCD-SRAM-FMC_D12 | - | - |
| 66 | PB10 | VCP_USART3_TX | RS-232_UART_TX<br>STMOD+ UART_TX<br>PMOD_UART_TX | - |
| 67 | PB11 | VCP_USART3_RX | RS-232_UART_RX<br>STMOD+ UART_RX<br>PMOD_UART_RX | - |

| LQFP144 pinout | Pin name | Main function pinout assignment | Optional function pinout assignment | Motor-control connector |
|---|---|---|---|---|
| 68 | VDD_SMPS | POWER | - | - |
| 69 | VLX | POWER | - | - |
| 70 | VSS_SMPS | POWER | - | - |
| 71 | VSS | POWER | - | - |
| 72 | V15 | POWER | - | - |
| 73 | VDD | POWER | - | - |
| 74 | PB13 | RS-232 LPUART1_CTS | STMOD+_LPUART1_CTS<br>PMOD_LPUART1_CTS | - |
| 75 | PB14 | UCPD_DB2 | - | - |
| 76 | PB15 | UCPD_CC2 | - | - |
| 77 | PD8 | LCD-SRAM-FMC_D13 | - | - |
| 78 | PD9 | LCD-SRAM-FMC_D14 | - | - |
| 79 | PD10 | LCD-SRAM-FMC_D15 | - | - |
| 80 | PD11 | SRAM-FMC_A16 | - | - |
| 81 | PD12 | SRAM-FMC_A17 | - | - |
| 82 | PD13 | SRAM-FMC_A18 | - | - |
| 83 | VSS | POWER | - | - |
| 84 | VDD | POWER | - | - |
| 85 | PD14 | LCD-SRAM-FMC_D0 | - | - |
| 86 | PD15 | LCD-SRAM-FMC_D1 | - | - |
| 87 | PG2 | SRAM-FMC_A12 | - | - |
| 88 | PG3 | SRAM-FMC_A13 | - | - |
| 89 | PG4 | SRAM-FMC_A14 | - | - |
| 90 | PG5 | SRAM-FMC_A15 | - | - |
| 91 | PG6 | RS-232 LPUART1_RTS | STMOD+_LPUART1_RTS<br>PMOD_LPUART1_RTS | - |
| 92 | PG7 | RS-232 LPUART1_TX | STMOD+_LPUART1_TX<br>PMOD_LPUART1_TX<br>VCP_LPUART1_TX | - |
| 93 | PG8 | RS-232 LPUART1_RX | STMOD+_LPUART1_RX<br>PMOD_LPUART1_RX<br>VCP_LPUART1_RX | - |
| 94 | VSS | POWER | - | - |
| 95 | VDD | POWER | - | - |
| 96 | PC6 | - | Touch key | TIM8_CH1 |
| 97 | PC7 | DFSDM1_DATIN3 | Touch key | TIM8_CH2 |
| 98 | PC8 | SDIO1_D0 | - | TIM8_CH3 |
| 99 | PC9 | SDIO1_D1 | TRACE_D0 | - |
| 100 | PA8 | Smartcard USART1_CK | - | - |
| 101 | PA9 | Smartcard USART1_TX | - | TIM1_CH2 |

| LQFP144 pinout | Pin name | Main function pinout assignment | Optional function pinout assignment | Motor-control connector |
|---|---|---|---|---|
| 102 | PA10 | Audio SAI1_SD_A | - | - |
| 103 | PA11 | USB_DM | - | - |
| 104 | PA12 | USB_DP | - | - |
| 105 | PA13 | SWDIO | JTAG_JTMS | - |
| 106 | VDDUSB | POWER | - | - |
| 107 | VSS | POWER | - | - |
| 108 | VDD | POWER | - | - |
| 109 | PA14 | SWCLK | JTAG_JTCK | - |
| 110 | PA15 | UCPD_CC | JTAG_JTDI | - |
| 111 | PC10 | SDIO_D2 | TRACE_D1 | - |
| 112 | PC11 | SDIO_D3 | - | - |
| 113 | PC12 | SDIO1_CK | STMOD+_SPI3_MOSI PMOD_SPI3_MOSI | - |
| 114 | PD0 | LCD-SRAM-FMC_D2 | - | - |
| 115 | PD1 | LCD-SRAM-FMC_D3 | - | - |
| 116 | PD2 | SDIO1_CMD | - | - |
| 117 | PD3 | LED_RED | - | - |
| 118 | PD4 | LCD-SRAM-FMC_NOE | - | - |
| 119 | PD5 | LCD-SRAM-FMC_NWE | - | - |
| 120 | VSS | POWER | - | - |
| 121 | VDD | POWER | - | - |
| 122 | PD6 | DFSDM1_DATIN1 | STMOD +_DFSDM1_DATIN1 | - |
| 123 | PD7 | SRAM-FMC_NE1 | - | - |
| 124 | PG9 | MFX_WAKE-UP | STMOD+_SPI3_SCK PMOD_SPI3_SCK | I/O |
| 125 | PG10 | SDCARD_DETECT | STMOD+_SPI3_MISO PMOD_SPI3_MISO | - |
| 126 | PG12 | LCD_CSn_FMC_NE4 | - | - |
| 127 | PG13 | I2C1_SDA | - | - |
| 128 | PG14 | I2C1_SCL | - | - |
| 129 | VSS | POWER | - | - |
| 130 | VDD | POWER | - | - |
| 131 | PG15 | LCD_CTP_INT | - | - |
| 132 | PB3 | LED_GREEN | JTAG_JTDO_SWO | - |
| 133 | PB4 | - | JTAG_NJTRST COMP2_INP STMOD+_SPI3_MISO2 | - |
| 134 | PB5 | UCPD_DB1 | COMP2_OUT STMOD+_SPI3_MOSI2 | - |
| 135 | PB6 | - | Touch key | TIM8_BKIN2 |

| LQFP144 pinout | Pin name | Main function pinout assignment | Optional function pinout assignment | Motor-control connector |
|---|---|---|---|---|
| 136 | PB7 | - | Touch key | - |
| 137 | PH3 | BOOT0 | - | - |
| 138 | PB8 | FDCAN1_RX | - | - |
| 139 | PB9 | FDCAN1_TX | - | - |
| 140 | PE0 | SRAM_FMC_NBL0 | - | - |
| 141 | PE1 | SRAM_FMC_NBL1 | - | - |
| 142 | VSS | POWER | - | - |
| 143 | V15 | POWER | - | - |
| 144 | VDD | POWER | - | - |

# Appendix B MFX I/O Assignment

Table 71. **MFX I/O Assignment**

| Signal name | Pin name |
|---|---|
| WIFI_SPI4_SCK | PE2 |
| MFX IO0 | MFX_3V3_SW_ENABLE |
| MFX IO1 | MFX_WIFI_GPIO |
| MFX IO2 | MFX_WIFI_DATRDY |
| MFX IO3 | MFX_Audio_RST |
| MFX IO4 | MFX_Camera_PLUG_IN |
| MFX IO5 | MFX_Camera_RSTI |
| MFX IO6 | MFX_Camera_XSDN |
| MFX IO7 | MFX_USB_OTG_FS_PWR_EN |
| MFX IO8 | MFX_1V8_SW_ENABLE |
| MFX IO9 | MFX_FDCAN_STBY |
| MFX IO10 | MFX_WIFI_WKUP |
| MFX IO11 | MFX_LED2 |
| MFX IO12 | MFX_LED3 |
| MFX IO13 | MFX_LED4 |
| MFX IO14 | MFX_WIFI_BOOT |
| MFX IO15 | MFX_WIFI_RST |
| MFX_GPO4 | MFXGPO_USB_OTG_HS_PWR_EN |
| MFX_GPO5 | MFXGPO_USB_HS_PHY_RESET |
| MFX_GPO6(1) | MFXGPO_EXT_RESET / MOTOR_GPIO1 |
| MFX_GPO7 | MFXGPO_MOTOR_GPIO2 |

1. *Pins shared between different functions and requiring hardware configuration (Such as jumper and soldered bridges)*

# Appendix C STM32H7B3I-EVAL mechanical drawing

MB1331 with 7’’ LCD daughterboard (RGB)

**Figure 36. Mechanical dimensions (in millimeters)**

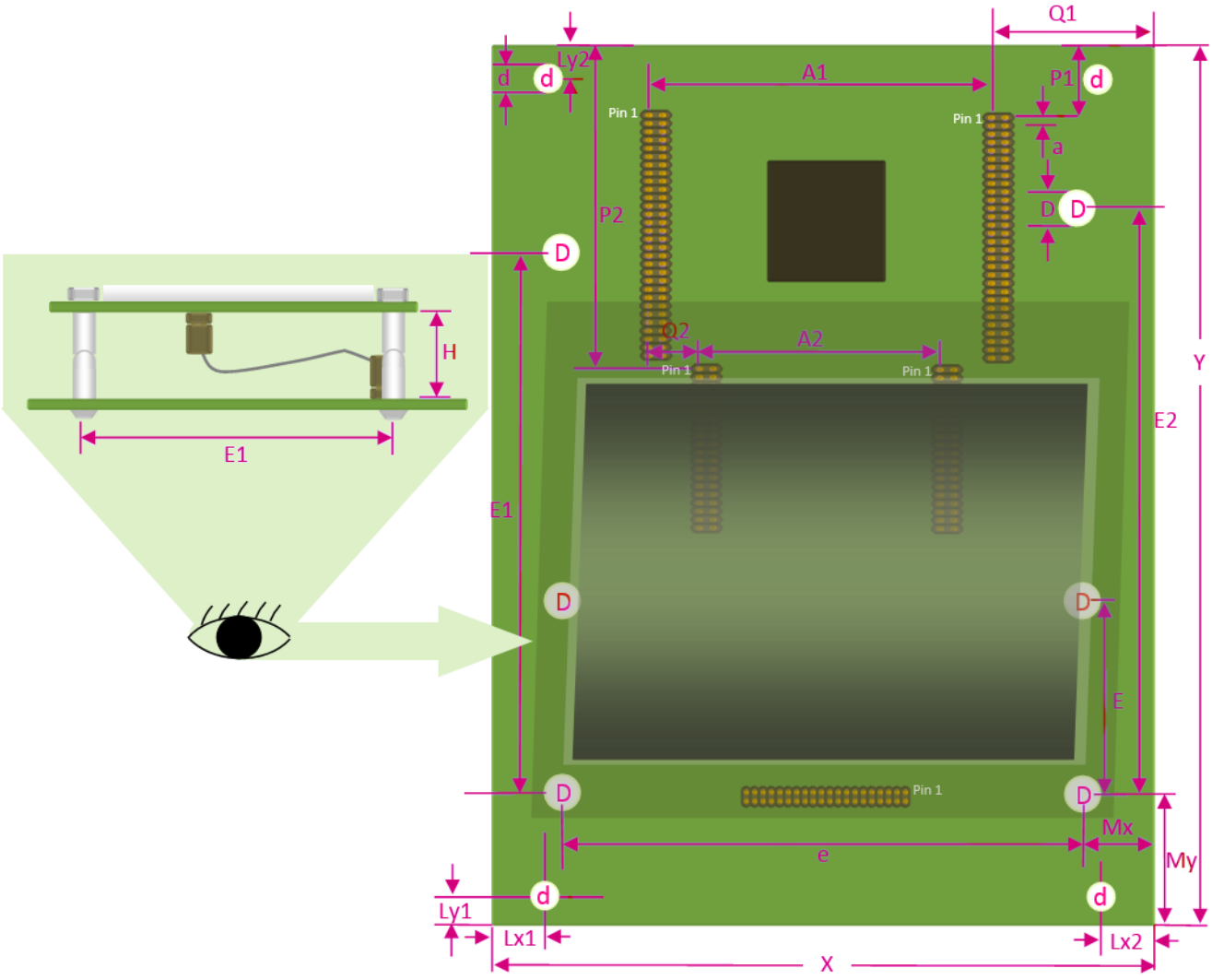



**Table 72. Mechanical dimensions (In millimeters)**

| Symbol | Size | Symbol | Size | Symbol | Size |
|---|---|---|---|---|---|
| A1 | 68.6 | e | 116.5 | My | 32.7 |
| A2 | 48.6 | H | 8 | P1 | 21.4 |
| a | 1.27 | Lx1 | 33.5 | P2 | 60.7 |
| D | 3.5 | Lx2 | 32.7 | Q1 | 50.6 |
| d | 3.5 | Ly1 | 5.4 | Q2 | 10 |
| E1 | 108 | Ly2 | 5.4 | X | 173 |
| E2 | 108 | Mx | 26.3 | Y | 169 |

# Appendix D Primary functions supported by default

Two main use case combinations are supported by default on the board with no limitations between these “primary” functions, and no hardware rework needed:

**Use case 1 (Audio)**

Following functions can be used at the same time without any limitations from each other:

- LCD
- 32-bit SDRAM
- OCSPI1
- SD card 1
- USB FS host
- Wi-Fi® SPI
- Audio I2S6
- VCP UART (PB14/PB15)
- DFSDM (4+1 microphones)

**Use case 2 (Camera)**

Following functions can be used at the same time without any limitations from each other:

- LCD
- 32-bit SDRAM
- OCSPI1
- SD card 1
- USB FS host
- Wi-Fi® SPI
- Camera
- VCP UART (PB14/PB15)
- DFSDM (1 microphone)

Figure 37. **Primary features - Use case compatibility matrix**

| | LCD | WIFI SPI | USB FS | VCP | SYS JTAG | DFSDMx4 | AUDIO I2S6 | CAMERA | ADC 16 BITS | OCSPI1 | SDRAM 32 bits | EXT I2C | SD CARD 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LCD | | - | - | - | - | - | - | - | - | - | - | - | - |
| WIFI SPI | - | | - | - | - | - | - | - | - | - | - | J (1) | - |
| USB FS | - | - | | - | - | - | - | - | - | - | - | - | - |
| VCP | - | - | - | | - | - | - | - | - | - | - | - | - |
| SYS JTAG | - | - | - | - | | - | J (1) | - | - | - | - | - | - |
| DFSDMx4 | - | - | - | - | - | | - | J (1) | - | - | - | - | - |
| AUDIO I2S6 | - | - | - | - | J (1) | - | | J (1) | - | - | - | - | - |
| CAMERA | - | - | - | - | - | J (1) | J (1) | | - | - | - | - | - |
| ADC 16 BITS | - | - | - | - | - | - | - | - | | - | - | - | - |
| OCSPI1 | - | - | - | - | - | - | - | - | - | | - | - | - |
| SDRAM 32 bits | - | - | - | - | - | - | - | - | - | - | | - | - |
| EXT I2C | - | J (1) | - | - | - | - | - | - | - | - | - | | - |
| SD CARD 1 | - | - | - | - | - | - | - | - | - | - | - | - | |

(1) Functions cannot be used together. A jumper is needed to select one of the two.

# Appendix E Secondary functions supported with limitations

Following secondary functions have limitations and cannot be used together with at least one of the primary functions supported by default on the board:

- NOR
- SRAM
- OCSPI2
- SD card 2
- USB HS (ULPI)
- Audio SAI
- DFSDM (5 microphones and LED)
- STMPS2 DFSDM
- CAN FD
- Bootloader VCP UART (PA2/PA3)
- RS-232 UART
- Motor control

**Figure 38. Secondary features - Use case compatibility matrix**

| | LCD | WIFI SPI | USB FS | VCP | SYS JTAG | DFSDMx4 | AUDIO I2S6 | CAMERA | ADC 16 BITS | OCSPI1 | SDRAM 32 bits | EXT I2 C | SD CARD 1 | AUDIO SAI | SD CARD 2 | USB HS | DFSDMx8 | NOR | SRAM | CAN | MOTOR JOYSTICK | MOTOR LEGACY | MOTOR DFSDM | OCSPI2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **AUDIO SAI** | - | J (1) | - | - | - | - | J (1) | J (1) | - | - | - | - | - | | - | - | - | - | - | - | - | SB (2) | - | - |
| **SD CARD 2** | - | - | - | J (1) | - | - | - | J (1) | - | J (1) | - | - | - | - | | - | - | - | J (1) | - | - | - | SB (2) | M (3) |
| **USB HS** | - | - | - | - | - | J (1) | J (1) | J (1) | J (1) | - | - | - | - | - | - | | J (1) | - | - | - | SB (2) | SB (2) | SB (2) | - |
| **DFSDMx8** | - | - | - | - | - | - | - | J (1) | - | - | - | - | - | - | - | J (1) | | J (1) | - | - | - | - | SB (2) | - |
| **NOR** | - | - | - | - | - | - | - | J (1) | - | - | - | - | - | - | - | - | J (1) | | - | - | SB (2) | SB (2) | SB (2) | M (3) |
| **SRAM** | - | - | - | - | - | J (1) | - | J (1) | - | - | - | - | J (1) | - | J (1) | - | - | - | | - | - | SB (2) | SB (2) | M (3) |
| **CAN** | - | - | SB (2) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | - | SB (2) | SB (2) | - |
| **MOTOR JOYSTICK** | - | - | - | - | - | - | - | SB (2) | - | - | SB (2) | - | - | - | - | SB (2) | - | SB (2) | - | - | | - | - | - |
| **MOTOR LEGACY** | J (1) | SB (2) | SB (2) | SB (2) | - | - | SB (2) | SB (2) | - | SB (2) | SB (2) | - | SB (2) | SB (2) | - | SB (2) | - | SB (2) | SB (2) | SB (2) | - | | SB (2) | - |
| **MOTOR DFSDM** | - | - | SB (2) | - | - | SB (2) | - | SB (2) | - | SB (2) | SB (2) | - | - | - | SB (2) | SB (2) | SB (2) | SB (2) | SB (2) | SB (2) | - | SB (2) | | - |
| **OCSPI2** | - | - | - | - | - | - | - | M (3) | - | - | M (3) | - | - | - | M (3) | - | - | M (3) | M (3) | - | - | - | - | |

(1) Functions cannot be used together. A jumper is needed to select one of the two.
(2) Functions cannot be used together. A solder bridge is needed to select one of the two.
(3) Functions cannot be used together. A module must be fitted or removed.

# Appendix F Federal Communications Commission (FCC) and Industry Canada (IC) Compliance Statements

Applicable for STM32H7B3I-EVAL Evaluation kit products with order code STM32H7B3I-EVAL (containing ISM43340-M4G-L44-10CF module).

## F.1 FCC Compliance Statement

Contains FCC ID: O7P-341

### Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

### Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

### Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

### Responsible party (in the USA)

Terry Blanchard
Americas Region Legal | Group Vice President and Regional Legal Counsel, The Americas
STMicroelectronics, Inc.
750 Canyon Drive | Suite 300 | Coppell, Texas 75019
USA
Telephone: +1 972-466-7845

## F.2 IC Compliance Statement

Contains/Contient IC: 10147A-341

This device complies with FCC and Industry Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

### Compliance Statement

Notice: This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Industry Canada ICES-003 Compliance Label: CAN ICES-3 (A) / NMB-3 (A).

### Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Étiquette de conformité à la NMB-003 d'Industrie Canada: CAN ICES-3 (A) / NMB-3 (A).

## F.3 CE conformity

### F.3.1 Warning

**EN 55032 / CISPR32 (2012) Class A product**

Warning: this device is compliant with Class A of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe A de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

### F.3.2 Simplified declaration of conformity

Hereby, STMicroelectronics declares that the radio equipment types STM32H7B3I-EVAL is in compliance with Directive 2014/53/EU.

# Appendix G Known limitations of demonstration firmware

- Embedded Wizard and Clock&weather: Moving background (moving wave ) behind the main background when the LCD dithering feature is enabled
- Touch GFX: Blinds Control - the kitchen and desk icons cannot be unselected once they are already selected
- Clock&Weather: Latency when gathering weather data from a remote server
- Clock&Weather: API keys are used in each weather API call, so sometimes the user may face a problem when collecting forecast data from the server due to the limited key number used by the application. When facing this problem, ST recommends trying connecting again in order to get forecast data. To use a private key, refer to the user manual *STM32CubeH7 demonstration platform* (UM2222), section 10.3.4, which explains how to integrate a custom key in the application source code.
- Clock&Weather: Display the weather only for a single city instead of three
- Clock&Weather: The Forecast weather service provider (OpenWeather map) modifies the data format by introducing new fields. This impacts data collection: city names and temperature values may sometimes be wrong. This issue must be fixed in the next release of the demo.

  ST recommends downloading the new binary available on the ST website for users who want to upgrade the demonstration binary.
- General: No “Return to Menu Launcher” icon for Touch GFX, STemWin and Embedded Wizard demos

# Revision history

Table 73. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 18-Feb-2020 | 1 | Initial release. |
| 25-Mar-2020 | 2 | Corrected supply config 1 title and R22 setting in Table 10 |
| 07-Jul-2020 | 3 | Added: Section  Appendix G  Known limitations of demonstration firmware |

# Contents

# List of tables

# List of figures

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved