Battery Input Board (BIB)
Lower Half Electronics (LHE) Primary Battery Board
Initial Board Bring-Up and Testing
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Battery Input Board (BIB) Testing

Before powering up the LHE I tested out the also new Battery Input Board (BIB). The BIB is used to interface the eight primary batteries to the LHE board. There are eight input connectors, one per battery, and one output connector which supplies battery power to the LHE. The BIB is laid out to provide a quad 2S4P battery connection. Simply put, there are four cells per battery; two in series provides the necessary bus voltage of 25.6Vdc. Four of these packs in parallel provide 104 amp-hours of energy to the CPF. The BIB has blocking diodes and fuses for each of the four packs.

Testing of the BIB entailed verifying the board was laid out and populated correctly. Ohm checks confirmed that the electrical connections were correct. I then applied power to each of the inputs and verified the correct outputs. The BIB was used on all subsequent LHE testing.

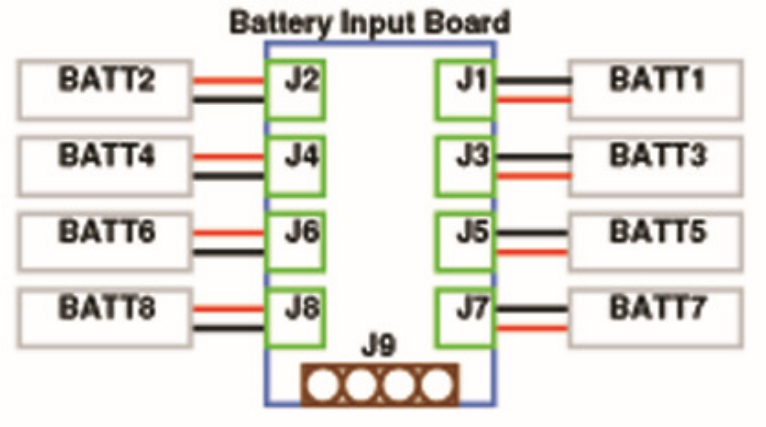

Figure One: Block diagram of the BIB connections.

Referring to Figure One, the eight individual 12.8Vdc batteries are connected to the BIB. The traces on the BIB combine 2&4, 6&8, 1&3, and 5&7 into four packs delivering 25.6Vdc (nominal) at 26Ah each.

Issues

No serious issues were found; the board operates as expected. I did notice that the spring activation mechanism is a little wonky on the Phoenix connectors which interface the batteries. When using a small flathead screwdriver to open the wire slot, the orange tab can move sideways a little bit. When installed in the CPF, care should be taken to apply the opening force in the down direction only.

Equipment Used

Extech 382260 Low Voltage Power Supply

Fluke 87 Multimeter

Relevant Battery Input Board (BIB) Files
\\CPF\Electrical Engr\Orcad Projects\Chads Stuff\Pri_Batt_Input_Board

Lower Half Electronics (LHE) Primary Battery Board Testing
There were five boards fabricated with two being populated onsite. The two boards were labeled as SN#01 and SN#02. A bulk of the testing required the rest of the CPF circuit boards to be connected to the LHE. These included the Motherboard, the Power Switch Board, and the Internal Sensor Interface Board. Tera Term on my computer was used to send and receive data.

Installed	JP1	Hotel LED
Installed	JP2	Pump LED
open	JP3	Sleep Disable
Used to turn on	JP4	Reed Switch On/Off
2-2	JP5	Power Override
2-2	JP6	Power Override

Table One: Initial jumper settings

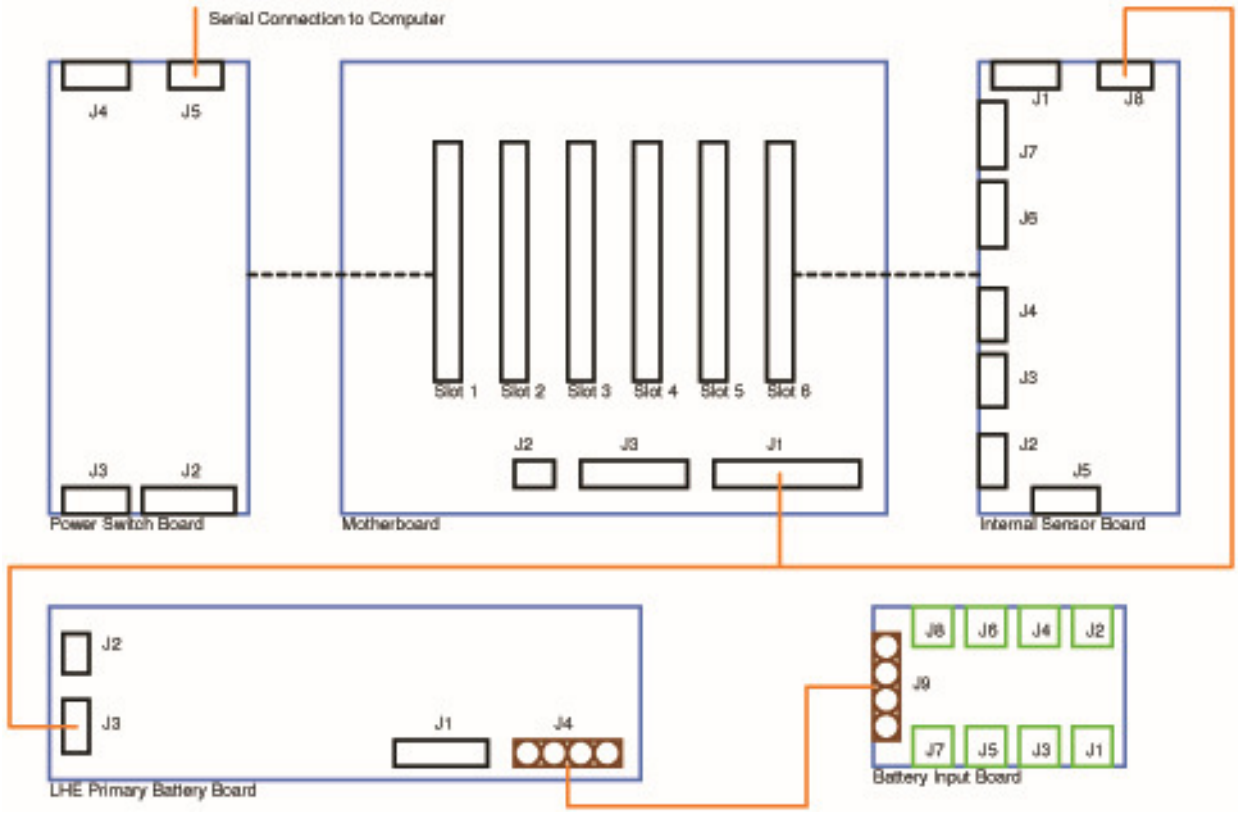

Figure Two: Block diagram of the CPF circuit boards

Equipment Used
Extech 382260 Low Voltage Power Supply (x4)
Fluke 87 Multimeter
Tektronix TDS 2014 Four Channel Digital Oscilloscope
BK Precision 8500 Programmable DC Electronic Load
Prolific PL2303GS USB-Serial Converter

Relevant LHE Primary Battery Board Files
\\CPF\Electrical Engr\Orcad Projects\Chads Stuff\LHE_Pri_Batt_Board

Board Power
For the initial powering of the LHE I used a single Extech power supply and ran the wires through the Battery Input Board. Straight away I noticed the board was not being powered correctly. I eventually discovered the shorting blocks for the i2c addresses were all shorted during population (see Issues below). Upon remedying the problem, the board powered up correctly. All voltages were within specifications, with the exception of pump power due to not having i2c up and running yet.

Good	TP1	Hotel Volts (Batt)
	TP2	Hotel Return
no i2c yet	TP3	Pump Volts (Batt)
	TP4	Pump Return
Good	TP5	Batt5V Spy
Good	TP6	Batt5V Spy
	TP7	Signal Common
Good	TP8	Mobo 5V Spy
Good	TP9	Mobo 5V Spy
	TP10	Signal Common

Table Two: Test point locations for initial power testing

Issues
During initial population, SB1-SB8 were all shorted. This caused Batt5V+ to be shorted to ground and damaged U7. Setting the SB's to their proper states and replacing U7 brought the Batt5V+ voltage back in compliance. This issue was present on both populated boards, so SN#02 was able to be fixed prior to powering up.

Communication via i2c

To test the i2c communication, the entire CPF board stack needs to be interconnected. See Figure Two above for the connection details. Eric Martin had already written a software interface to the Motherboard and had also written an initial piece of code for the LHE Primary Board.

Initial attempts at i2c communication were unsuccessful. My first troubleshooting step was to verify all of the i2c addresses across all of the interconnected boards. I did have to change the default address on the LHE board as that address was already in use on the Motherboard.

ADR0	ADR1	Hex Addr	Dec Addr	Device
H	L	CE	206	
NC	H	D0	208	
H	H	D2	210	Switch U6
NC	NC	D4	212	LHE U1
NC	L	D6	214	LHE U5
L	H	D8	216	Switch U12
H	NC	DA	218	
L	NC	DC	220	
L	L	DE	222	Mobo U1

Table Three: i2c Communication Addresses

At this point, I was able to communicate with the Motherboard via address DE. However, the LHE board was unable to communicate. Using an oscilloscope, I saw no activity on the clock or data lines on the output of U11 (PCA9512). The PCA9512 is an i2c buffer chip which allows hot swapping of daughter boards and provides voltage translation. After subsequent troubleshooting, I found that an incorrect version of the energy monitor IC (LTC2946) had been ordered and installed onto the two LHE boards (see Issues below). Replacing the part fixed the issue and i2c comms worked fine after that.

During my troubleshooting I also noticed that the ADIN pin (pin 13) on U1 was left floating. According to the datasheet, it needs to be tied to some sort of reference voltage in order to make an accurate measurement. I had a voltage divider added to the board in the same way that U5 has. After this mod was installed, I lost i2c comms to the energy monitor chips. After eliminating other possibilities, I had the mod removed and U1 and U5 replaced. Once again, i2c comms returned to normal. Subsequent Hotel Load testing (below) resulted in believable numbers. As of now, the pin is still floating, but the part appears to be working correctly.

Issues

The LTC2946 is an energy monitoring chip; it samples the input voltage and uses a current sense resistor to measure the load current. This part separates the serial data line (SDA) into individual input and output pins (SDAI and SDAO). This allows the user to add in optional external opto transistors for electrical isolation, if desired. A version of the LTC2946 exists which inverts the SDAO line (LTC2946-1). It is pin compatible with the non-inverting version (LTC2946). The inverting part was ordered and installed; the inverted output line locked up all i2c communication to the LHE board. Replacing it with the non-inverting version fixed the issue and all i2c comms started working.

Hotel Load

To test the hotel load, I clipped leads onto TP1 and TP2 and connected those to an electronic dummy load (BK Precision 8500). I varied the load resistance and measured both the analog voltage and current, and also used the i2c bus to read back the energy monitor readings. These values were then plotted and a conversion factor found.

Hotel Path

ILoad (nom)	RLoad (omhs)	VLoad (volts)	ILoad (amps)	Volt (Cts)	Amps (Cts)
0			0	954	5
0.01	2400	23.86	0.008	954	7
0.025	960	23.84	0.023	953	10
0.05	480	23.83	0.048	953	15
0.1	240	23.81	0.097	952	25
0.25	96	23.77	0.246	951	54
0.5	48	23.72	0.492	950	104
1	24	23.65	0.983	948	201
2	12	23.50	1.956	946	396
3	8	23.37	2.918	944	588
4	6	23.25	3.872	942	778

Table Four: SN#01 Hotel load values

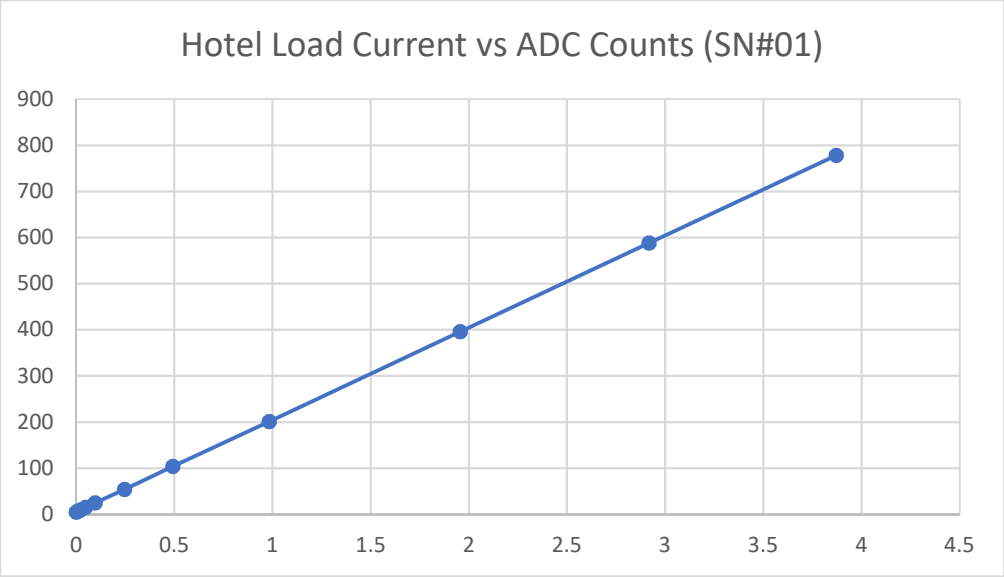

Figure Three: SN#01 Hotel load plot (Measured current vs i2c ADC counts)

Hotel Path

ILoad (nom)	RLoad (ohms)	VLoad (volts)	ILoad (amps)	Volt (Cts)	Amps (Cts)
0			0	954	5
0.01	2400	23.87	0.010	954	7
0.025	960	23.85	0.024	954	10
0.05	480	23.84	0.049	953	15
0.1	240	23.82	0.098	953	25
0.25	96	23.78	0.247	951	54
0.5	48	23.73	0.493	950	104
1	24	23.65	0.984	949	202
2	12	23.50	1.956	946	396
3	8	23.36	2.918	944	589
4	6	23.23	3.869	941	779

Table Five: SN#02 Hotel load values

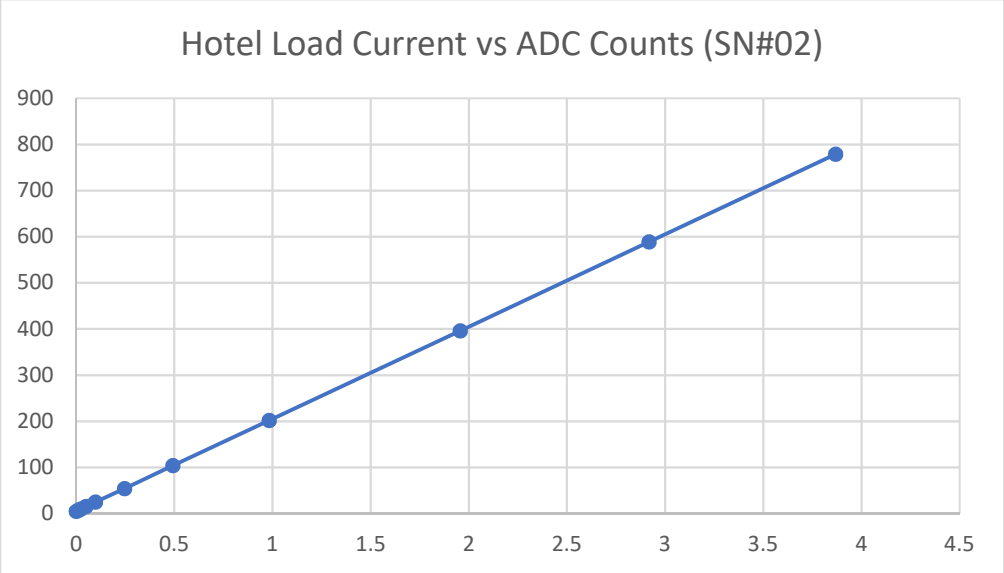

Figure Four: SN#02 Hotel load plot (Measured current vs i2c ADC counts)

In addition to the load current measurements, I also tested the undervoltage warning and shutdown functionality. An undervoltage warning is flagged when the battery voltage reaches nominally 18Vdc; the system will experience a hardware shutdown when the battery voltage reaches nominally 16Vdc.

	SN# 01	SN# 02
Signal	(volts)	(volts)
N_UV_WARN	18.09	17.94
Shutdown	16.11	16.12

Table Six: Undervoltage measurements

Pump Load

To test the pump power path, I used a test cable to connect J4 to the electronic dummy load. I varied the load resistance and measured both the analog voltage and current, and also used the i2c bus to read back the energy monitor readings. These values were then plotted and a conversion factor found.

Pump Path

ILoad (nom)	RLoad (omhs)	VLoad (volts)	ILoad (amps)	Volt (Cts)	Amps (Cts)
0	None	0.34	0	15	0
0	None	23.88	0	954	0
0.5	48	23.78	0.493	950	59
1	24	23.74	0.987	949	117
2	12	23.67	1.970	947	234
3	8	23.61	2.950	945	350
4	6	23.56	3.925	944	466
6	4	23.45	5.863	941	696
8	3	23.35	7.785	938	924
10	2.4	23.26	9.690	936	1150
12	2	23.16	11.578	933	1375
13	1.85	23.10	12.484	931	1483

Table Seven: SN#01 Pump power path load values

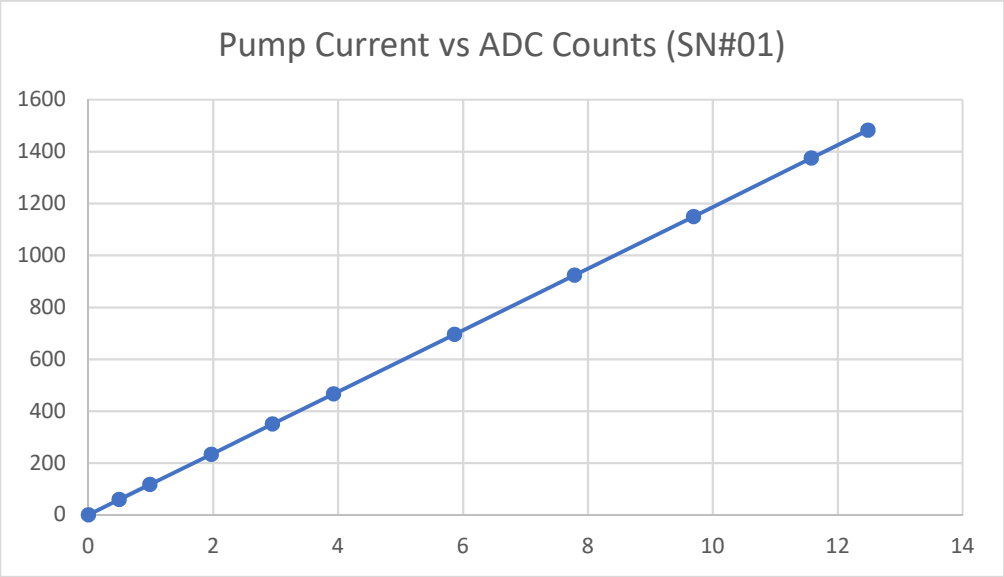

Figure Five: SN#01 Pump power plot (Measured current vs i2c ADC counts)

Pump Path

ILoad (nom)	RLoad (ohms)	VLoad (volts)	ILoad (amps)	Volt (Cts)	Amps (Cts)
0	None	0.36	0	15	0
0	None	23.87	0	954	1
0.5	48	23.77	0.492	950	60
1	24	23.73	0.985	949	118
2	12	23.66	1.968	947	236
3	8	23.61	2.949	945	353
4	6	23.56	3.925	944	469
6	4	23.45	5.863	941	700
8	3	23.36	7.785	938	928
10	2.4	23.26	9.690	935	1156
12	2	23.16	11.579	932	1382
13	1.85	23.10	12.484	931	1490

Table Eight: SN#02 Pump power path load values

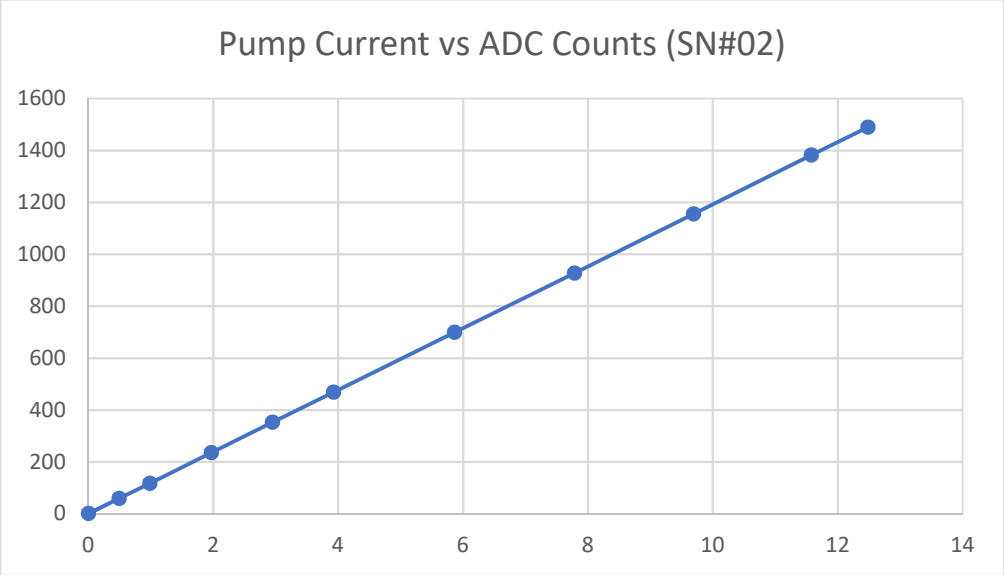

Figure Six: SN#02 Pump power plot (Measured current vs i2c ADC counts)

Sleep Circuit

In order to save battery energy, the LHE board can be put into sleep mode from 2^(n-1) minutes at a time where n is an integer from 1 to 7. This corresponds to fixed sleep times of 1, 2, 4, 8, 16, 32, or 64 minutes. The heart of the sleep circuit is a MC14536 timer chip. A combination of an analog (RC) frequency clock and digital inputs determine how often the output signal changes state, thus initiating a sleep or non-sleep cycle. I ran through each of the seven fixed sleep timers and measured the actual sleep time.

			(minutes)	(minutes)	(seconds)	(seconds)	(seconds)	(minutes)	(minutes)
Command	**n**	**n-1**	**2^(n-1)**	**Meas Time**	**Meas Time**	**Nom Time**	**Delta**	**Expected**	**Measured**
	0								
Sleep 1	1	0	1	1:08	68	60	8	1	1.13
Sleep 2	2	1	2	2:16	136	120	16	2	2.27
Sleep 3	3	2	4	4:31	271	240	31	4	4.52
Sleep 4	4	3	8	9:01	541	480	61	8	9.02
Sleep 5	5	4	16	18:00	1080	960	120	16	18.00
Sleep 6	6	5	32	35:57	2157	1920	237	32	35.95
Sleep 7	7	6	64	71:51	4311	3840	471	64	71.85

Table Nine: SN#01 Sleep circuit measurements

			(minutes)	(minutes)	(seconds)	(seconds)	(seconds)	(minutes)	(minutes)
Command	**n**	**n-1**	**2^(n-1)**	**Meas Time**	**Meas Time**	**Nom Time**	**Delta**	**Expected**	**Measured**
	0								
Sleep 1	1	0	1	1:09	69	60	9	1	1.15
Sleep 2	2	1	2	2:17	137	120	17	2	2.28
Sleep 3	3	2	4	4:34	274	240	34	4	4.57
Sleep 4	4	3	8	9:06	546	480	66	8	9.10
Sleep 5	5	4	16	18:09	1089	960	129	16	18.15
Sleep 6	6	5	32	36:16	2176	1920	256	32	36.27
Sleep 7	7	6	64	72:28	4348	3840	508	64	72.47

Table Ten: SN#02 Sleep circuit measurements

Issues

Both boards ran slow on the sleep timer by about eight seconds per minute. At the longest sleep period of 64 minutes, this results in an actual sleep time of 72 minutes. I am currently leaving the sleep circuit as is. If needed, the timing could be modified by changing the RC values for the MC4536 timer.

Sleep Power Consumption

While the LHE board was in sleep mode, I measured the Batt5V+ current draw by monitoring TP5 and TP6. I measured 4.14mV. The sense resistor measured 0.98 ohms, which results in a sleep current of 4.22mA. This is significantly higher than the design goal of ~100uA. It appears that the bulk of this excess sleep current is originating from the two LTC2946 energy monitor chips. According to the datasheet, they need to be put into a shutdown mode via an i2c command before the LHE board is put to sleep. I verified from Eric Martin that this is not part of the current code. This can be retested after Eric has a chance to modify the code.

Conclusion

Overall, the initial bring-up of the LHE board was very successful, with the exception of a few minor problems.

- Both energy monitor chips (U1 and U5) need to be placed in shutdown mode prior to the LHE board going into sleep mode. This is done via a software command over the i2c bus.
- Sleep timer is slow by eight seconds per minute. This delay is linear with increasing sleep times.
- The largest sleep period is ~1hr (72 minutes with the accumulated delays)
- Reminder to remove the LED jumpers prior to deployment
- Document all solder bridge connections for i2c addresses
- The Pumpmon command appears to be reading the Hotel load (maybe from the Mobo?)