Design Notes
Lower Half Elex Board, *Primary* Battery System, Coastal Profiling Float

2021-07-26	ECM	adapt from HD Battery req'ts doc
2021-10-30	ECM	update per 1st design review -- parallel power/coulomb counter paths
2021-01-04	ECM	uprate Pump power switch but leave CB limit at 12 A for now

1. Requirements

1.1. Manage 8S4P pack of Electrochem 3B0036 Li primary cells. Pack wired in four parallel strings, cells independently fused at ?? amps, diode or'd, master pack fuse at TBD amps, and brought out on four heavy wires.

1.2 Typical discharge profile is 10 min pumping at 8 A, 1 hr profiling at 0.3 A, and 1-23 hr sleeping at 0.004 A. Float system max current draw is TBD A. Wiring and fusing should support this load.

1.3 Expected pack operating voltage range is 31.4 V max (beginning of life, open circuit), 16 V min (end of life, full load, 0 degC). Estimated capacity at 0 degC and 8 A load is approx 2.55 V/cell x 8 cells x 26 A-hr/string x 4 strings = 2100 W-hr. (C.f. Inspired Energy @ 28V x 3.2 A-hr x 6 sticks = 540 W-hr.)

1.4 LHE should provide pack undervoltage cutoff, CPU-controlled sleep function, endcap reed switch (power on/off) support, and parallel Hotel and Pump power paths each with on/off control, overcurrent protection, and coulomb counting.

1.5 LHE pack undervoltage should shut down input from battery pack, after ~100 msec at pack voltage of 16.0 (TBD) V falling. Undervoltage warning (optional) should be at 18.0 (TBD) V falling

1.6 LHE sleep function should switch hotel and pump power off for programmable periods from 1 to 64 minutes (+/- 5%). The sleep function should be armed and triggered over the I2C connection to the Mobo/Micro. Standby power in the sleep state should be less than 2.5 mW (100 uA at 25 V), with a goal of using less than 1% of battery energy during a year.

1.7 LHE should accept input from two endcap momentary contact reed switches and should switch hotel power on or off respectively, and should enable pump power or switch it off, respectively. Standby power of the LHE in the reed-switch-off state should be less than 2.5 mW.

1.8 The Hotel power path should include soft-start inrush control with a current limit of 6 A (TBD) and be able to charge 1000 uF of downstream capacitance. The Hotel power path

should include Electronic Circuit Breaker (ECB) function with a trip rating of 6A and trip time of 15 msec. ECB latch-off vs auto-retry is TBD. The Hotel power path should include an I2C Ammeter/Coulomb Counter with <5 mA/count current resolution and >100 A-hr capacity.

1.9 The Pump power path should include a power switch with on/off control and fault reporting accessible over the I2C bus from the Mobo/Micro. The power switch should include soft-start inrush control with a current limit of 12 A (TBD) and be able to charge 1000 uF of downstream capacitance. The Pump power path should include Electronic Circuit Breaker (ECB) function with a trip rating of 12 A and trip time of 15 msec. ECB latch-off vs auto-retry is TBD. The Pump power path should include an I2C Ammeter/Coulomb Counter with <10 mA/count current resolution and >200 A-hr capacity. The Pump power path should use a large TVS diode(s) for motor regen control; an active regen control circuit is not required.

1.10 LHE interface to Mobo/Micro should present I2C on two signal lines at 100 kbit/s, 24 V battery power output at TBD A max, and should receive I2C 5 V logic power input at 100 mA max (for Mobo-related interface circuits in the battery pack). The I2C signals should be buffered by an NXP PCA9512 Buffer device.

1.11 LHE available board area is ~8.6" x ~2.2" with ~6 standoff screw mounting holes. Vertical clearance is TBD.

2. Description

2.1 Input undervoltage. An LTC2934 supervisor monitors pack discharge voltage via divider network. At low pack voltage (18V TBD), this generates the warning N_UV_Warn, which can be read by polling the PIO interface by the Mobo/Micro. At a lower voltage (16V TBD), this causes Undervoltage Shutdown by disabling FloatPwrOn, which disables both power path switches. The auxilliary n_MR input to the supervisor allows the PwrOnEnb signal from the sleep timer to control the power switches when pack voltage is within tolerance.

2.2 Power path switch and overcurrent Two LTC4380 circuits are present to provide power switching and soft start for the Sleep and Endcap Power functions. Their overcurrent function is used to protect the system from downstream shorts or overcurrent demands. The Hotel power switch is controlled only by the FloatPwrOn signal from the undervoltage circuit, while the Pump power switch is gated both by FloatPwrOn and by Pump_Pwr_On from the PIO port.

2.3 Sleep Timer and On/Off Control: Flip-Flop 741G74 is the manual power control for the Float. It is set or reset by momentary closure of the endcap Pwr_On and Pwr_off reed switches, respectively, and its output is gated to become the PwrOnEnb enable signal which controls the two power path power switches via the undervoltage monitor circuit.

The sleep timer is an MC14536 oscillator/timer set for 2.185 kHz, with inputs ABC that can be configured for delays from 1 to 64 minutes. The sleep time is set by Mobo PIO outputs SleepTime0-2, which are clocked into a 74HC174 latch by raising Mobo PIO signal SleepTrig

high.

During normal (non-sleep) float operation, SleepTime0-2 is held to 000, which when latched is applied to AND gate 741G27 to produce the Sleep_Dis signal. Sleep_Dis resets the sleep timer, stops its oscillator, and forces its output high, which allows AND gate 741G00 to be controlled by the reed switch power flip-flop to set MasterPwrOn to either the on or off state.

Sleep is enabled by writing a non-zero value to SleepTime0-2, and triggered by raising SleepTrig high to latch the value into the 74HC174. The SleepTime value n is applied to the timer's ABC inputs, selecting decoder stages corresponding to delays of 2^(n-1) minutes at the timer output. At the same time, the non-zero value applied to the 741G27 gate allows SleepDis to go low and the timer to begin counting.

The timer output goes low after one timer clock cycle (~0.5 msec), which forces the AND gate to
override the manual power flip-flop and set PwrOnEnb to the off state. The timer output remains low for the commanded sleep time and then goes high, gating PwrOnEnb back to the on state which enables the two power path switches via the undervoltage monitor circuit.

The sleep cycle will repeat after another 2^(n-1) minutes, so upon awaking from sleep the Mobo controller should write 000 to SleepTime0-2, and latch it by cycling SleepTrig high and then low. (This should be part of normal power-on initialization as well.)

After initialization the SleepTime and SleepTrig PIO port bits can be re-configured as inputs, for some additional insurance against inadvertent writes, as they are held in inactive states by pulldowns.

The Float can be powered on or off from any state, asleep or awake, via the momentary operation of the endcap reed switches. If the Float is in sleep mode, the endcap Pwr_On reed switch will set the power control flip-flop and also reset the SleepTime latch to 000, setting SleepDis, disabling the sleep timer, and gating MasterPwrOn to the the on state.

2.4 Coulomb Counters: Two LTC2946 Energy Monitors in the power paths 'borrow' the current-sense signals used by the LTC4380 overcurrent circuits. Each monitor's Charge accumulator provides a 32-bit reading of current demand times time. The monitors are powered from the always-on Batt5V bus in order to retain accumulator data throughout a deployment; they should be placed in Shutdown Mode before the Float is put to sleep or powered down, in order to reduce current demand from ~1 mA active to ~20 uA quiescent values.

2.5 Mobo PIO Port: The Mobo controls the LHE board via two TCA6408 8-bit I2C/PIO ports. The ports can be bitwise configured as either inputs or outputs. The first port, I2C address 0x21, is largely an output port, and generates the pump power and sleep trigger signals. The second port, I2C address 0x20, has the Undervoltage Warn and pump power fault (circuit breaker tripped) inputs. The second port also has the sleep timer control bit outputs SleepTime0-2.

2.6 Power Supplies: The LHE board generates the always-on 5V logic supply Batt5V from

the pack input, via a TPS7A16 LDO regulator. An additional 5V logic supply Mobo5V is derived from the 5 V logic power provided by the Mobo interface when the Mobo is on. Batt5V powers the sleep timer and coulomb counter, while Mobo5V is used for the Mobo-facing portions of the PIO port and I2C interface.

3. Design Notes

3.1 Undervoltage Supervisor Desired trip voltages are 18V UV Warn, 16V UV Shutdown (2.0 V/cell). Allow 10 uA for divider to keep impedances low, 16V/10uA = 1.6 Mohm total divider impedance. (Supervisor input current 1 nA so no worreis.) PFI (warn) threshold is 0.400 V, bottom R value is 0.4V/18V x 1.6M = 35.5k use 35.7k. ADJ (shutdown) threshold is 0.400, R value is, 0.4/16V x 1.6M = 40.0k, subtract bottom R to get middle R: 40.0 - 35.7 = 4.30k, use 4.32k. Top R should be 1.6M - 35.5k - 4.32k = 1.56M use 1.58M to wind up a bit low.

LTC2934 ADJ input has 5% hysteresis which will be 0.8V at 16V. Per Electrochem data (0 degC/2A pulse), voltage drop when loaded is ~0.5V, so 0.8V should be adequate to prevent repetitive tripping. If needed, a positive-feedback resistor location is provided and a large-value resistor can be added to further increase hysteresis.

3.2 Hotel Power/Inrush/CB Switch LTC4380 current limit threshold at Sns input is 50 mV. 6 A limit needs 8 mohm. 6 A x 15 msec x 30V is right at SOA limit for PSMN1R7-60 MOSFET.

3.3 Hotel Coulomb Counter LTC2946 full scale Sense input is 102.4 mV, LSB is 25 uV. With 8 mohm shunt, full scale is 12.8 A and LSB is 3.125 mA. Set CLK_DIV divider to 4 (default) to divide 4 MHz clock to target 250 kHz for A/D, should give 16.4 msec conversion/accumulate time, 2.23 year time counter overflow (per datasheet).

1 charge accumulator count should be 1 A/D LSB x 1 count = 3.125 mA x 16.4 msec = 51.25 uC.

Charge accumulator is 36 bits with top 32 bits read back, so 16 accumulator counts for 1 LSB read back. 1 LSB read back = 51.25 uC x 16 counts = 0.82 mC/LSB readback resolution. Full scale should be 0.82 mC x 2**32 = 3.52 E6 C (A-sec). 3.52 E6 C / 3600 sec/hr = 978 A-hr. (C.f. 104 A-hr pack size.)

3.4 Pump Power/Inrush/CB Switch LTC4380 current limit threshold at Sns input is 50 mV. 12.5A limit needs 4mohm. (If 4 mohm is still out of stock, use 7.5 and 9 mohm in parallel (stacked) for 4.1mohm and 12.2 A limit if needed?) 12 A x 15 msec x 30V is right at SOA limit for most TO-220 MOSFETs so use IXTX200N10L2 in TO-247 which is optimized for linear-region SOA and can handle 12Ax30V for 100+ msec (limited by package heating).

3.5 Pump Coulomb Counter LTC2946 full scale Sense input is 102.4 mV, LSB is 25 uV. With 4 mohm shunt, full scale is 25.6 A and LSB is 6.25 mA. Set CLK_DIV divider to 4 (default) to divide 4 MHz clock to target 250 kHz for A/D, should give 16.4 msec conversion/accumulate time, 2.23 year time counter overflow (per datasheet).

1 charge accumulator count should be 1 A/D LSB x 1 count = 6.25 mA x 16.4 msec = 102.5 uC.

Charge accumulator is 36 bits with top 32 bits read back, so 16 accumulator counts for 1 LSB read back. 1 LSB read back = 102.5 uC x 16 counts = 1.64 mC/LSB readback resolution. Full scale should be 1.64mC x 2**32 = 7.04 E6 C (A-sec). 7.04 E6 C / 3600 sec/hr = 1957 A-hr. (C.f. 104 A-hr pack size.)

To repeat: The 2946 chips (both of them) are powered from the always-on Batt5V bus in order to retain accumulator data throughout a deployment. They must be placed in its Shutdown Mode before the Float is put to sleep or powered down, in order to reduce current demand from ~1 mA active to ~20 uA quiescent values.

3.6 Sleep Timer

MC14536 Configuration: Keep RC osc above 400 Hz based on note in old Motorola HC4060 spec sheet. Dynamic Icc per specs is 1.5uA/kHz @ 5V. Minimum sleep time 1 min which is a half period so minimum count period is 2 min or 120 sec. 120 / 2^18 = 458 usec period or 2.185 kHz frequency. Spec sheet Fig.12 says Fosc = 1 / 2.3*R*C, 2.0 k and 0.1uF give 2.174 kHz with a 5% tol X7R capacitor (available NP0 caps are all 1206 or 1210 size, with boardflex concerns).

3.7 Overcurrent Coordination

3.8 Power Supplies Batt5V loads are

Timer MC14536 dynamic	6 uA
Other logic, LDO quiescent	~20
Reed switch pullups	1000
Energy monitor 4 MHz 2@950uA	1900
	2926 uA total

For 32V input and ~3 mA load, TPS7A16 LDO dissipation should be (32-5) V x 3 mA = 81 mW. LDO junction-ambient resistance is 66 K/W so rise is 66 K/W x 81 mW = ~5 degC which is negligible.

3.X Standby Power Budget: Focus on sleep/shutdown power since Float power should dominate when power is on. 4 strings x 26 A-hr/string = 104 A-hr for pack. Target 1% for sleep, gives 1.04 A-hr. 1 A-hr / 24 hr / 365 d = 114 uA sleep budget.

UV divider	10 uA
LTC4380 shutdown @ 8uA x2	16
TPS7A16 LDO	10
MC14536 dynamic	6
TCA6408 ports, static, 2 @ 7uA	14
Energy Monitor shutdown 2@30uA	+ 60
	106 uA

Questions/Comments for Review

1. ~~Reed/Sleep interaction logic looks backwards, Reed_On can't override Sleep -- reverse reed labelling and use n_Q output?~~
2. Both overcurrent are latch-off. OK? (Retry available but req. different 4380 chip)
3. Need: Final numbers for Float 5V and 12V loads, and/or Mobo max VBatt current draw.
4. Need: LHE and DC-DC board vertical clearance dimension(s).
5. ~~Ed check sequencing of PIO power and need for Joint4V7 power rail.~~
6. Energy Monitors on Batt pwr (requires shutdown) or Mobo pwr (requires saving data)?
7. UV Warning to Mobo interrupt (as was planned for Alert signal)?

Questions for Electrochem/BattSpecialties

What is 3B0036 internal fuse?
Recc fuse to coordinate (blow first) for 4 parallel strings
Suggested UV Warn and Shutdown voltages for 8 series 3B0036

Programming Notes

1. Both energy monitors (LTC2946) must be put into shutdown mode (<40uA) before float is put to sleep or turned off; when active they draw ~1 mA.