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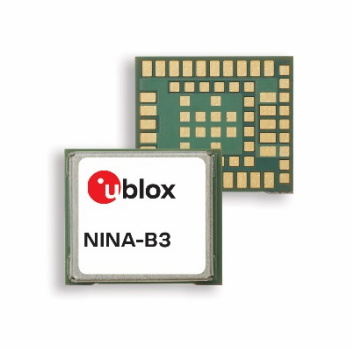
NINA-B3 series

Stand-alone Bluetooth 5 low energy modules

Data Sheet



Abstract

This technical data sheet describes the stand-alone NINA-B3 series Bluetooth® 5 low energy modules. The NINA-B3 series includes two variants - NINA-B30 and NINA-B31 series. The NINA-B30 series provides an open CPU architecture with a powerful MCU for customer applications, while the NINA-B31 series are delivered with u-blox connectivity software pre-flashed.

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Document Information

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Initial Production	Early Production Information	Data from product verification. Revised and supplementary data may be published later.
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This document applies to the following products:

Product name	**Type number**	**u-blox connectivity software version**	**PCN reference**	**Product status**
NINA-B311	NINA-B311-00B-00	1.0.0	N/A	Initial Production
NINA-B312	NINA-B312-00B-00	1.0.0	N/A	
NINA-B301	NINA-B301-00B-00	-	N/A	
NINA-B302	NINA-B302-00B-00	-	N/A	

Contents

1 Functional description

1.1 Overview

The NINA-B3 series modules are small stand-alone Bluetooth 5 low energy modules featuring full Bluetooth 5 support, a powerful Arm® Cortex®-M4 with FPU, and state-of-the-art power performance. The embedded low power crystal improves power consumption by enabling optimal power save modes.

The NINA-B3 series includes the following two variants as listed in the table below:

Model	Description
NINA-B30 series	Bluetooth 5 module with a powerful Arm Cortex-M4 with FPU, and state-of-the-art power performance. Both the variants of NINA-B30 are open CPU modules that enable customer applications to run on the built-in Arm Cortex-M4 with FPU. With 1 MB flash and 256 kB RAM, they offer the best-in-class capacity for customer applications on top of the Bluetooth low energy stack. NINA-B302 comes with an internal antenna, while NINA-B301 has a pin for use with an external antenna. The internal PIFA antenna is specifically designed for the small NINA form factor and provides an extensive range, independent of ground plane and component placement.
NINA-B31 series	Bluetooth 5 module with a powerful Arm Cortex-M4 with FPU and u-blox connectivity software pre-flashed. The connectivity software in NINA-B31 modules provides support for u-blox Bluetooth low energy Serial Port Service, GATT client and server, beacons, NFC™, and simultaneous peripheral and central roles – all configurable from a host using AT commands. The NINA-B31x modules provide top grade security, thanks to secure boot, which ensures the module only boots up with original u-blox software. NINA-B312 comes with an internal antenna, while NINA-B311 has a pin for use with an external antenna. The internal PIFA antenna is specifically designed for the small NINA form factor and provides an extensive range, independent of ground plane and component placement.

The NINA-B3 series modules are globally certified for use with the internal antenna or a range of external antennas. This greatly reduces time, cost, and effort for customers integrating these modules in their designs.

1.2 Applications

- Industrial automation
- Smart buildings and cities
- Low power sensors
- Wireless-connected and configurable equipment
- Point-of-sales
- Health devices

1.3 Product features

1.3.1 NINA-B30 series

Model		Radio						Interfaces										Features		Grade		
	Software application	Bluetooth® qualification	Bluetooth profiles	NFC for "Touch to Pair"	Maximum conducted output power [dBm]	Maximum range [m]	Antenna type	UART	SPI	I²C	I²S	USB	QDEC	PDM	PWM	GPIO pins	AD converters (ADC)	Secure boot	Over-the-air firmware update	Standard	Professional	Automotive
NINA-B301	Open CPU*	v5.0	G	●	8	1400	P	2	3	2	1	1	1	1	12	38	8	●	●		●	
NINA-B302	Open CPU*	v5.0	G	●	8	1400	I	2	3	2	1	1	1	1	12	38	8	●	●		●	

* = Features enabled by hardware. The actual support depends on the open CPU application software / P = antenna pin / I = internal antenna / G = GATT

Table 1: NINA-B30 series main features summary

1.3.2 NINA-B31 series

Model		Radio						Interfaces		Features					Grade		
	Software application	Bluetooth® qualification	Bluetooth profiles	NFC for "Touch to Pair"	Maximum conducted output power [dBm]	Maximum range [m]	Antenna type	UART	GPIO pins	u-blox Low Energy Serial Port Service	Extended Data Mode protocol	GATT server and GATT client	Secure boot	AT command support	Standard	Professional	Automotive
NINA-B311	uCS	v5.0	G	●	8	1400	P	1	28	●	●	●	●	●		●	
NINA-B312	uCS	v5.0	G	●	8	1400	I	1	28	●	●	●	●	●		●	

uCS = u-blox connectivity software / G = GATT / P = antenna pin / I = internal antenna

Table 2: NINA-B31 series main features summary

1.4 Block diagram

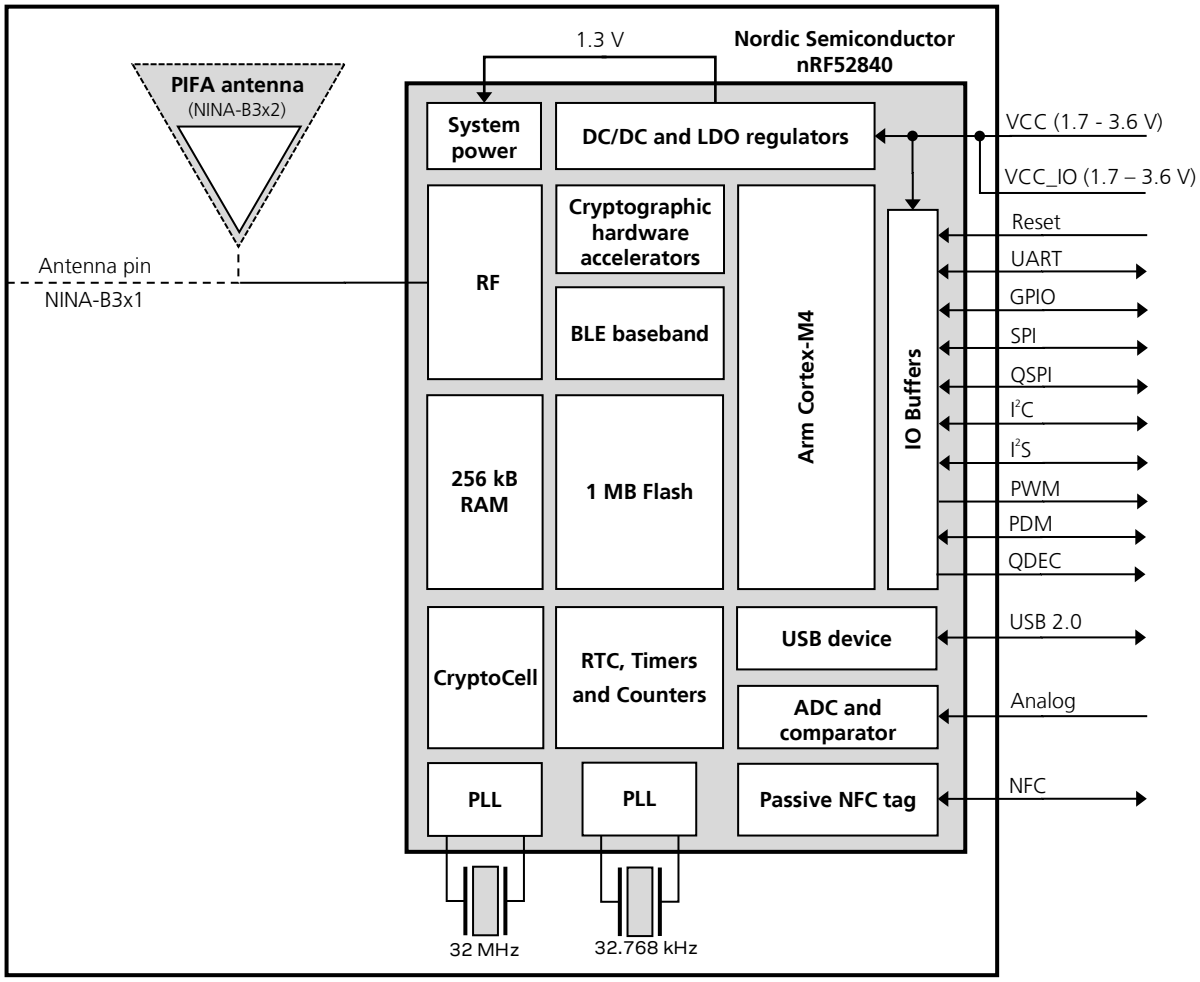


Figure 1: Block diagram of NINA-B3 series

1.4.1 NINA-B311

The NINA-B311 modules do not use the internal antenna and thus the PCB has been trimmed to allow for a smaller module (10.0 x 11.6 mm). Instead of an internal antenna, the RF signal is available at a module pin for routing to an external antenna or antenna connector.

1.4.2 NINA-B312

The NINA-B312 modules use an internal metal sheet PIFA antenna mounted on the PCB (10.0 x 15.0 mm). The RF signal pin is not connected to any signal path.

1.5 Product description

Item	NINA-B3x1	NINA-B3x2
Bluetooth version	5.0	5.0
Band support	2.4 GHz, 40 channels	2.4 GHz, 40 channels
Typical conducted output power	+7.5 dBm	+8 dBm
Radiated output power (EIRP)	+10.5 dBm (with approved antennas)	+10 dBm
RX sensitivity (conducted)	-94 dBm	-94 dBm
RX sensitivity, long range mode (conducted)	-100 dBm	-100 dBm
Supported BLE data rates	1 Mbps 2 Mbps 500 kbps 125 kbps	1 Mbps 2 Mbps 500 kbps 125 kbps
Module size	10.0 x 11.6 mm	10.0 x 15.0 mm

Table 3: NINA-B3 series characteristics summary

1.6 Hardware options

Except for the different PCB sizes and antenna solutions, the NINA-B3 series modules use an identical hardware configuration. An on-board 32.768 KHz crystal is included as well as an integrated DC/DC converter for higher efficiency under heavy load situations (see section 2.1.1 for more information).

1.7 Software options

The integrated application processor of the NINA-B3 module is an Arm Cortex-M4 with FPU that has 1 MB flash memory and 256 kB RAM. The NINA-B3 modules support additional external memory that can be connected to the Quad Serial Peripheral Interface (QSPI); see section 2.4.3 for additional information. The software structure of any program running on the module can be broken down into the following components:

- Radio stack
- Bootloader (optional)
- Application

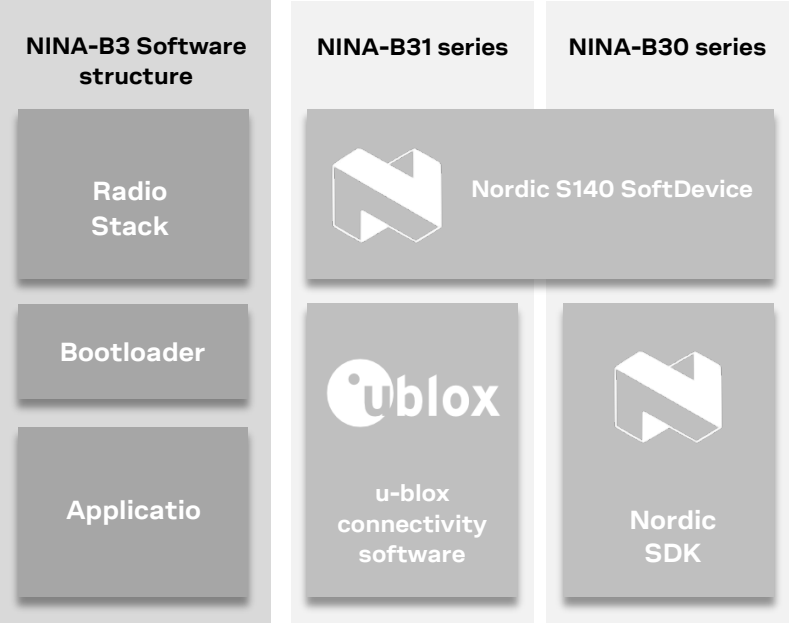


Figure 2: NINA-B3 software structure and available software options

1.7.1 u-blox connectivity software

The NINA-B31 series modules are pre-flashed with u-blox connectivity software.
The u-blox connectivity software enables use of the u-blox Low Energy Serial Port Service, controlled by AT commands over the UART interface. The NINA-B31 modules can be configured using the u-blox s-center evaluation software, which can be downloaded from the u-blox website and is available free of charge.

Much more information on the features and capabilities of the u-blox connectivity software and how to use it can be found in the u-blox Short Range AT Commands Manual [2] and the NINA-B31 Getting Started [4].

1.7.2 Open CPU

The open CPU architecture in the NINA-B30 series modules allows you to build your own applications. u-blox recommends the following development approaches to speed up the process:

1.7.2.1 Nordic SDK

The Nordic Semiconductors nRF5 SDK provides a rich and well-tested software development environment for nRF52 based devices. It includes a broad selection of drivers, libraries, and example applications. It also includes other radio stacks.

The NINA-B3 series modules are only certified for use with the S140 Bluetooth Low Energy SoftDevice. If you would like to use another 2.4 GHz radio protocol, contact u-blox support for your area as listed in the Contact section.

1.8 Bluetooth device address

Each NINA-B31 module is pre-programmed with a unique 48-bit Bluetooth device address. For NINA-B30 series modules, or if the memory of a NINA-B31 module is corrupted or otherwise lost, the address can be recovered from the data matrix barcode printed on the module label.

2 Interfaces

2.1 Power management

2.1.1 Module supply input (VCC)

The NINA-B3 series uses integrated step-down converters to transform the supply voltage presented at the **VCC** pin into a stable system voltage. Because of this, the NINA-B3 modules are compatible for use in battery powered designs without the use of an additional voltage converter. You can choose one of the following two on-board voltage converter options:

- A low-dropout (LDO) converter
- A DC/DC buck converter

Normally, the module will automatically switch between these options depending on the current consumption of the module. Under high loads such as when the radio is active, the DC/DC converter is more efficient, while the LDO converter is more efficient in the power saving modes.

2.1.2 Digital I/O interfaces reference voltage (VCC_IO)

All modules in the u-blox NINA series provide an additional voltage supply input for setting the I/O voltage level. In NINA-B3 series modules, the I/O voltage level is similar to the supply voltage and **VCC_IO** is internally connected to the supply input. Therefore, only a single supply voltage is needed for NINA-B3, which makes it ideal for battery powered designs.

☞ This may not be the case for other modules in the NINA series. A design that should be pin compatible with other NINA-series modules should keep the **VCC** and **VCC_IO** supply rails separate.

2.2 RF antenna interfaces

2.2.1 2.4 GHz Bluetooth low energy (ANT)

The three NINA-B3 model versions have their own 2.4 GHz antenna solutions respectively:

- The NINA-B311 modules provide an antenna pin (**ANT**) with a nominal characteristic impedance of
  50 Ω. This pin can be connected to an onboard antenna or antenna connector using a controlled impedance trace.
- The NINA-B312 modules use an integrated antenna solution; no additional components are required. The antenna is a metal sheet PIFA antenna that makes the module insensitive to placement on the carrier board or the size of the carrier board, when compared to other integrated antenna solutions. The **ANT** pin is internally disconnected on these models.

2.2.2 Near Field Communication (NFC)

The NINA-B3 series modules include a Near Field Communication interface, capable of operating as a 13.56 MHz NFC tag at a bit rate of 106 kbps. As an NFC tag, the data can be read from or written to the NINA-B3 modules using an NFC reader; however, the NINA-B3 modules are not capable of reading other tags or initiating NFC communications. The NFC interface can be used to wake the module from sleep mode, meaning that the module can be kept in the deepest power save mode and wake up and properly react to an NFC field.

Two pins are available for connecting to an external NFC antenna: **NFC1** and **NFC2**.

2.3 System functions

The NINA-B3 series modules are power efficient devices capable of operating in different power saving modes and configurations. Different sections of the module can be powered off when not needed and complex wake- up events can be generated from different external and internal inputs. The radio part of the module operates independently from the CPU. The three main power modes are:

- Active
- Standby
- Sleep

Depending on the application, the module should spend most of its time in either standby or sleep mode to minimize current consumption.

2.3.1 Module power-on

You can switch on or reboot the NINA-B3 modules in one of the following ways:

- Rising edge on the VCC pin to a valid supply voltage
- Issuing a reset of the module (see section 2.3.5)

An event to wake up from the sleep mode to the active mode can be triggered by:

- A programmable digital or analog sensor event. For example, rising voltage level on an analog comparator pin
- Detecting an NFC field
- Supplying 5 V to the **VBUS** pin (plugging in the USB interface)

While waking up from the standby mode to active mode, an event can also be triggered by:

- The on-board Real Time Counter (RTC)
- The radio interface

2.3.2 Module power off

There is no dedicated pin to power off the NINA-B3 modules. You can configure any GPIO pin to enter or exit the sleep mode (see section 2.3.4), which essentially powers down the module.

An under-voltage (brown-out) shutdown occurs on the NINA-B3 modules when the **VCC** supply drops below the operating range minimum limit. If this occurs, it is not possible to store the current parameter settings in the module's non-volatile memory. An over temperature and under temperature shutdown can be enabled on the NINA-B3 modules, and is initiated if the temperature measured within the module is outside operating conditions. The temperature is measured by an integrated temperature sensor in the radio chip.

2.3.3 Standby mode

Standby mode is one of the power saving modes in NINA-B3 modules that essentially powers down the module but keeps the system RAM and configurations intact. It also allows for complex, autonomous power-up events including periodic RTC events and radio events.

The following events can be used to bring the module out of the standby mode:

- Internal wake-up events from the RTC, radio, NFC and so on.
- Analog or digital sensor events (programmable voltage level or edge detection)

During standby mode, the module is clocked at 32 kHz, which is generated by an internal 32 kHz crystal oscillator.

2.3.4 Sleep mode

Sleep mode is the deepest power saving mode of NINA-B3 modules. During sleep mode, all functionality is stopped to ensure minimum power consumption. The module needs an external event in order to wake up from the sleep mode. The module will always reboot after waking up from the sleep mode; however different sections of the RAM can be configured to remain intact during and after going to the sleep mode.

The following events can be used to wake up the module out of the sleep mode:

- External event on a digital pin
- External analog event on a low power comparator pin
- Detection of an NFC field

When using the u-blox connectivity software, the module can be manually switched on or off with proper storage of the current settings using the UART **DSR** pin.

The module can be programmed to latch the digital values present at its GPIO pins during sleep. The module will keep the values latched, and a change of state on any of these pins will trigger a wake-up to active mode.

2.3.5 Module reset

You can reset the NINA-B3 modules using one of the following ways:

- Low level on the **RESET_N** input pin, normally kept high using an internal pull-up. This causes an “external” or “hardware” reset of the module. The current parameter settings are not saved in the module’s non-volatile memory and a proper network detach is not performed.
- Using the AT+CPWROFF command. This causes an “internal” or “software” reset of the module. The current parameter settings are saved in the module’s non-volatile memory and a proper network detach is performed.

2.3.6 CPU and memory

The Nordic Semiconductor nRF52840 chip in the NINA-B3 series modules includes a powerful Arm Cortex M4 processor. The processor works with a superset of 16 and 32-bit instructions (Thumb-2) at 64 MHz clock speed. It can use up to 37 interrupt vectors and 3 priority bits.

The nRF52840 chip has 1 MB of flash and 256 KB of RAM for code and data storage. Additionally, up to 4 GB of external memory can be addressed with Execute in Place (XIP) support via the QSPI interface. See Section 2.4.3 for additional information.

2.3.7 Direct Memory Access

All interfaces described in this data sheet support Direct Memory Access (DMA) to move any data generated from the interface directly into the RAM, without involving the CPU. This ensures fluent operation of the CPU with minimal need for interruption. To reduce the overall power consumption, DMA should be used as often as possible.

2.3.8 Programmable Peripheral Interconnect

The Nordic Semiconductor nRF52840 chip in the NINA-B3 series modules include a programmable peripheral interconnect (PPI), which is basically a switch matrix that connects various control signals between different interfaces and system functions. This allows most interfaces to bypass the CPU in order to trigger a system function, that is, an incoming data packet may trigger a counter or a falling voltage level on an ADC, might toggle a GPIO, all without having to send an interrupt to the CPU. This enables smart applications that are extremely power efficient that wake up the CPU only when it is needed.

2.3.9 Real Time Counter (RTC)

A key system feature available on the module is the Real Time Counter. This counter can generate multiple interrupts and events to the CPU and radio as well as internal and external hardware blocks. These events can be precisely timed ranging from microseconds up to hours, and allows for periodic BLE advertising events etc., without involving the CPU. The RTC can be operated in the active and standby modes.

2.4 Serial interfaces

NINA-B3 modules provide the following serial communication interfaces:

- 2x UART interfaces: 4-wire universal asynchronous receiver/transmitter interface used for AT command interface, data communication, and u-blox connectivity software upgrades using the Software update+UFWUPD AT command.
- 3x SPI interfaces: Up to three serial peripheral interfaces can be used simultaneously.
- 1x QSPI interface: High speed interface used to connect to the external flash memories.
- 2x I^2C interfaces: Inter-Integrated Circuit (I^2C) interface for communication with digital sensors.
- 1x I^2S interface: Used to communicate with external audio devices.
- 1x USB 2.0 interface: The USB device interface to connect to the upstream host.

☞ Most digital interface pins on the module are shared between the digital, analog interfaces and GPIOs. Unless otherwise stated, all functions can be assigned to any pin that is not already occupied.

☞ Two of the SPI interfaces share common hardware with the I^2C interfaces and they cannot be used simultaneously. That is, if both the I^2C interfaces are in use then only one SPI interface will be available.

2.4.1 Universal Asynchronous Receiver/Transmitter (UART)

The 4-wire UART interface supports hardware flow control and baud rates up to 1 Mbps. Other characteristics of the UART interface are listed below:

- Pin configuration:
    - TXD, data output pin
    - RXD, data input pin
    - RTS, Request To Send, flow control output pin (optional)
    - CTS, Clear To Send, flow control input pin (optional)
- Hardware flow control or no flow control (default) is supported.
- Power saving indication available on the hardware flow control output (**RTS** pin): The line is driven to the OFF state when the module is not ready to accept data signals.
- Programmable baud rate generator allows most industry standard rates, as well as non-standard rates up to 1 Mbps.
- Frame format configuration:
    - 8 data bits
    - Even or no-parity bit
    - 1 stop bit
- Default frame configuration is 8N1, meaning eight (8) data bits, no (N) parity bit, and one (1) stop bit.
- Frames are transmitted in such a way that the least significant bit (LSB) is transmitted first.

2.4.2 Serial peripheral interface (SPI)

NINA-B3 supports up to three Serial Peripheral Interfaces with serial clock frequencies of up to 8 MHz. Characteristics of the SPI interfaces are listed below:

- Pin configuration in master mode:
    - SCLK, Serial clock output, up to 8 MHz
    - MOSI, Master Output Slave Input data line
    - MISO, Master Input Slave Output data line
    - CS, Chip/Slave select output, active low, selects which slave on the bus to talk to. Only one select line is enabled by default but more can be added by customizing a GPIO pin.
    - DCX, Data/Command signal, this signal is optional but is sometimes used by the SPI slaves to distinguish between SPI commands and data
- Pin configuration in slave mode:
    - SCLK, Serial clock input
    - MOSI, Master Output Slave Input data line
    - MISO, Master Input Slave Output data line
    - CS, Chip/Slave select input, active low, connects/disconnects the slave interface from the bus.
- Both master and slave modes are supported on all the interfaces.
- The serial clock supports both normal and inverted clock polarity (CPOL) and data should be captured on rising or falling clock edge (CPHA).

2.4.3 Quad serial peripheral interface (QSPI)

The Quad Serial Peripheral Interface enables external memory to be connected to the NINA-B3 module to increase the application program size. The QSPI supports “Execute In Place (XIP)”, which allows CPU instructions to be read and executed directly from the external memory (128 MB at a time with a programmable offset). Characteristics for the QSPI are listed below:

- The QSPI always operates in master mode and uses the following pin configuration:
    - **CLK**, serial clock output, up to 32 MHz
    - **CS**, Chip/Slave select output, active low, selects which slave on the bus to talk to
    - **D0**, MOSI serial output data in single mode, data I/O signal in dual/quad mode
    - **D1**, MISO serial input data in single mode, data I/O signal in dual/quad mode
    - **D2**, data I/O signal in quad mode (optional)
    - **D3**, data I/O signal in quad mode (optional)
- Single/dual/quad read and write operations (1/2/4 data signals)
- Clock speeds between 2 – 32 MHz
- Data rates up to 128 Mbit/s in the quad mode
- 32 bit addressing can address up to 4 GB of data
- Instruction set includes support for deep power down mode of the external flash
- Possible to generate custom flash instructions containing a 1 byte opcode and up to 8 bytes of additional data and read its response

2.4.4 I^2C interface

The Inter-Integrated Circuit interfaces can be used to transfer and/or receive data on a 2-wire bus network. The NINA-B3 modules can operate as both master and slave on the I^2C bus using standard (100 kbps), fast (400 kbps), and 250 kbps transmission speeds. The interface supports clock stretching, thus allowing NINA-B3 to temporarily pause any I^2C communications. Up to 127 individually addressable I^2C devices can be connected to the same two signals.

- Pin configuration:
    - SCL, clock output in master mode, input in slave mode

- SDL, data input/output pin

This interface requires external pull-up resistors to work properly in the master mode; see section 4.2.7 for suggested resistor values. The pull-up resistors are required in the slave mode as well but should be placed at the master end of the interface.

2.4.5 I²S interface

The Inter-IC Sound (I^2S) interface can be used to transfer audio sample streams between NINA-B3 and external audio devices such as codecs, DACs, and ADCs. It supports original I^2S and left or right-aligned interface formats in both master and slave modes.

- Pin configuration:
  - MCK, Master clock
  - LRCK, Left Right/Word/Sample clock
  - SCK, Serial clock
  - SDIN, Serial data in
  - SDOUT, Serial data out

The Master side of an I^2S interface always provides the **LRCK** and **SCK** clock signals, but some master devices cannot generate a **MCK** clock signal. NINA-B3 can supply a **MCK** clock signal in both master and slave modes to provide to those external systems that cannot generate their own clock signal. The two data signals - **SDIN** and **SDOUT** allow for simultaneous bi-directional audio streaming. The interface supports 8, 16, and 24-bit sample widths with up to 48 kHz sample rate.

2.4.6 USB 2.0 interface

The NINA-B3 series modules include a full speed Universal Serial Bus (USB) device interface which is compliant to version 2.0 of the USB specification. Characteristics of the USB interface include:

- Full speed device, up to 12 Mbit/s transfer speed
- MAC and PHY implemented in the hardware
- Pin configuration:
  - VBUS, 5 V supply input, required to use the interface
  - USB_DP, USB_DM, differential data pair
- Automatic or software controlled pull-up of the **USB_DP** pin

The USB interface has a dedicated power supply that requires a 5 V supply voltage to be applied to the **VBUS** pin. This allows the USB interface to be used even though the rest of the module might be battery powered or supplied by a 1.8 V supply etc.

2.5 Digital interfaces

2.5.1 PWM

The NINA-B3 modules provide up to 12 independent PWM channels that can be used to generate complex waveforms. These waveforms can be used to control motors, dim LEDs, or as audio signals if connected to the speakers. Duty-cycle sequences may be stored in the RAM to be chained and looped into complex sequences without CPU intervention. Each channel uses a single GPIO pin as output.

2.5.2 PDM

The pulse density modulation interface is used to read signals from external audio frontends like digital microphones. It supports single or dual-channel (left and right) data input over a single GPIO pin. It supports up to 16 kHz sample rate and 16 bit samples. The interface uses the DMA to automatically move the sample data into RAM without CPU intervention. The interface uses two signals - **CLK** to output the sample clock and **DIN** to read the sample data.

2.5.3 QDEC

The quadrature decoder is used to read quadrature encoded data from mechanical and optical sensors in the form of digital waveforms. Quadrature encoded data is often used to indicate rotation of a mechanical shaft in either a positive or negative direction. The QDEC uses two inputs - **PHASE_A** and **PHASE_B**, and an optional **LED** output signal. The interface has a selectable sample period ranging from 128 µs to 131 ms.

2.6 Analog interfaces

8 out of the 38 digital GPIOs can be multiplexed to analog functions. The following analog functions are available:

- 1x 8-channel ADC
- 1x Analog comparator*
- 1x Low-power analog comparator*

*Only one comparator can be used at any given point of time.

2.6.1 ADC

The Analog to Digital Converter (ADC) is used to sample an analog voltage on the analog function enabled pins of the NINA-B3. Any of the 8 analog inputs can be used. Characteristics of the comparator include:

- Full swing input range of 0 V to **VCC**.
- 8/10/12-bit resolution
- 14-bit resolution while using oversampling
- Up to 200 kHz sample rate
- Single shot or continuous sampling
- Two operation modes: Single-ended or Differential
- Single-ended mode:
    - A single input pin is used
- Differential mode:
    - Two inputs are used and the voltage level difference between them is sampled

If the sampled signal level is much lower than the **VCC**, it is possible to lower the input range of the ADC to better encompass the wanted signal, and achieve a higher effective resolution. Continuous sampling can be configured to sample at a configurable time interval, or at different internal or external events, without CPU involvement.

2.6.2 Comparator

The analog comparator compares the analog voltage on one of the analog enabled pins in NINA-B3 with a highly configurable internal or external reference voltage. Events can be generated and distributed to the rest of the system when the voltage levels cross. Further characteristics of the comparator include:

- Full swing input range of 0 V to VCC.
- Two operation modes: Single-ended or Differential
- Single-ended mode:
    - A single reference level or an upper and lower hysteresis selectable from a 64-level reference ladder with a range from 0 V to VREF (described in Table 4)
- Differential mode:
    - Two analog pin voltage levels are compared, optionally with a 50 mV hysteresis
- Three selectable performance modes - High speed, balanced, or power save

See section 4.2.8 for a comparison of the various analog comparator options.

2.6.3 Low power comparator

In addition to the power save mode available for the comparator, there is a separate low power comparator available on the NINA-B3 module. This allows for even lower power operation, at a slightly lower performance and with less configuration options. Characteristics of the low power comparator include:

- Full swing input range of 0 to **VCC**.
- Two operation modes - Single-ended or Differential
- Single-ended mode:
    - The reference voltage LP_VIN- is selected from a 15-level reference ladder
- Differential mode:
    - Pin **GPIO_16** or **GPIO_18** is used as reference voltage LP_VIN-
- Can be used to wake the system from sleep mode

See section 4.2.8 for the electrical specifications of the different analog comparator options. See Table 4 for a summary of the analog pin options. Since the run current of the low power comparator is very low, it can be used in the module sleep mode as an analog trigger to wake up the CPU. See section 2.3.4 for additional information.

2.6.4 Analog pin options

Table 4 shows the supported connections of the analog functions.

☞ An analog pin may not be simultaneously connected to multiple functions.

Symbol	Analog function	Can be connected to
ADCP	ADC single-ended or differential positive input	Any analog pin or **VCC**
ADCN	ADC differential negative input	Any analog pin or **VCC**
VIN+	Comparator input	Any analog pin
VREF	Comparator single-ended mode reference ladder input	Any analog pin, **VCC**, 1.2 V, 1.8V or 2.4V
VIN-	Comparator differential mode negative input	Any analog pin
LP_VIN+	Low-power comparator IN+	Any analog pin
LP_VIN-	Low-power comparator IN-	**GPIO_16** or **GPIO_18**, 1/16 to 15/16 **VCC** in steps of 1/16 **VCC**

Table 4: Possible uses of the analog pins

2.7 GPIO

The NINA-B3 series modules are versatile concerning pin-out. In an un-configured state, there will be 38 GPIO pins in total and no analog or digital interfaces. All interfaces or functions must then be allocated to a GPIO pin before use. 8 out of the 38 GPIO pins are analog enabled, meaning that they can have an analog function allocated to them. In addition to the serial interfaces, Table 5 shows the number of digital and analog functions that can be assigned to a GPIO pin.

2.7.1 Drive strength

All GPIO pins are normally configured for low current consumption. Using this standard drive strength, a pin configured as output can only source or sink a certain amount of current. If the timing requirements of a digital interface cannot be met, or if an LED requires more current etc., a high drive strength mode is available, which allows the digital output to draw more current. See section 4.2.6 for more information.

Function	Description	Default NINA pin	Configurable GPIOs
General purpose input	Digital input with configurable pull-up, pull-down, edge detection and interrupt generation		Any
General purpose output	Digital output with configurable drive strength, push-pull, open collector or open emitter output		Any
Pin disabled	Pin is disconnected from the input and output buffers	All*	Any
Timer/ counter	High precision time measurement between two pulses/ Pulse counting with interrupt/event generation		Any
Interrupt/ Event trigger	Interrupt/event trigger to the software application/ Wake up event		Any
HIGH/LOW/Toggle on event	Programmable digital level triggered by internal or external events without CPU involvement		Any
ADC input	8/10/12/14-bit analog to digital converter		Any analog
Analog comparator input	Compare two voltages, capable of generating wake-up events and interrupts		Any analog
PWM output	Output simple or complex pulse width modulation waveforms		Any
Connection status indication	Indicates if a BLE connection is maintained	BLUE**	Any

* = If left unconfigured ** = While using the u-blox connectivity software

Table 5: GPIO custom functions configuration

2.8 u-blox connectivity software features

This section describes some of the system related features in the u-blox connectivity software. For additional information, see the u-blox Short Range AT Commands Manual [2].

2.8.1 u-blox Serial Port Service (SPS)

The serial port service feature enables serial port emulation over Bluetooth low energy.

2.8.2 System status signals

The **RED, GREEN, and BLUE** pins are used to signal the system status as shown in Table 6. They are active low and are intended to be routed to an RGB LED.

Mode	Status	RGB LED Color	RED	GREEN	BLUE
Data mode/Extended Data mode (EDM)	IDLE	Green	HIGH	LOW	HIGH
Command mode	IDLE	Orange	LOW	LOW	HIGH
EDM/Data mode, Command mode	CONNECTING	Purple	LOW	HIGH	LOW
EDM/Data mode, Command mode	CONNECTED**	Blue	HIGH	HIGH	LOW

* = LED flashes on data activity

Table 6: System status indication

☞ The CONNECTING and CONNECTED statuses indicate u-blox SPS connections.

2.8.3 System control signals

The following input signals are used to control the system:

- **RESET_N** is used to reset the system. See section 2.3.5 for detailed information.
- If **SWITCH_2** is driven low during start up, the UART serial settings are restored to their default values.
- The **SWITCH_2** can be used to open a Bluetooth LE connection with a peripheral device.

- If both **SWITCH_1** and **SWITCH_2** are driven low during start up, the system will enter bootloader mode.
- If both **SWITCH_1** and **SWITCH_2** are driven low during start up and held low for 10 seconds, the system will exit the bootloader mode and restore all settings to their factory default.

2.8.4 UART signals

In addition to the normal **RXD**, **TXD**, **CTS,** and **RTS** signals, the u-blox connectivity software adds the **DSR** and **DTR** pins to the UART interface. Note that they are not used as originally intended, but to control the state of the NINA module. For example, depending on the current configuration:

The **DSR** pin can be used to:

- Enter the command mode
- Disconnect and/or toggle connectable status
- Enable/disable the rest of the UART interface
- Enter/wake up from the sleep mode

The **DTR** pin can be used to indicate:

- The System mode
- If the SPS peers are connected
- If a Bluetooth LE bonded device is connected
- A Bluetooth LE GAP connection

☞ See the u-blox Short Range AT Commands Manual [2] for more information.

2.9 Debug interfaces

2.9.1 SWD

The NINA-B30 series modules provide an SWD interface for flashing and debugging. The SWD interface consists of two pins - **SWDCLK** and **SWDIO**. The SWD interface is disabled on the NINA-B31 series modules.

2.9.2 Trace – Serial Wire Output

A serial trace option is available on the NINA-B30 series modules as an additional pin- **SWO**. The Serial Wire Output (SWO) is used to:

- Support printf style debugging
- Trace OS and application events
- Emit diagnostic system information

A debugger that supports Serial Wire Viewer (SWV) is required.

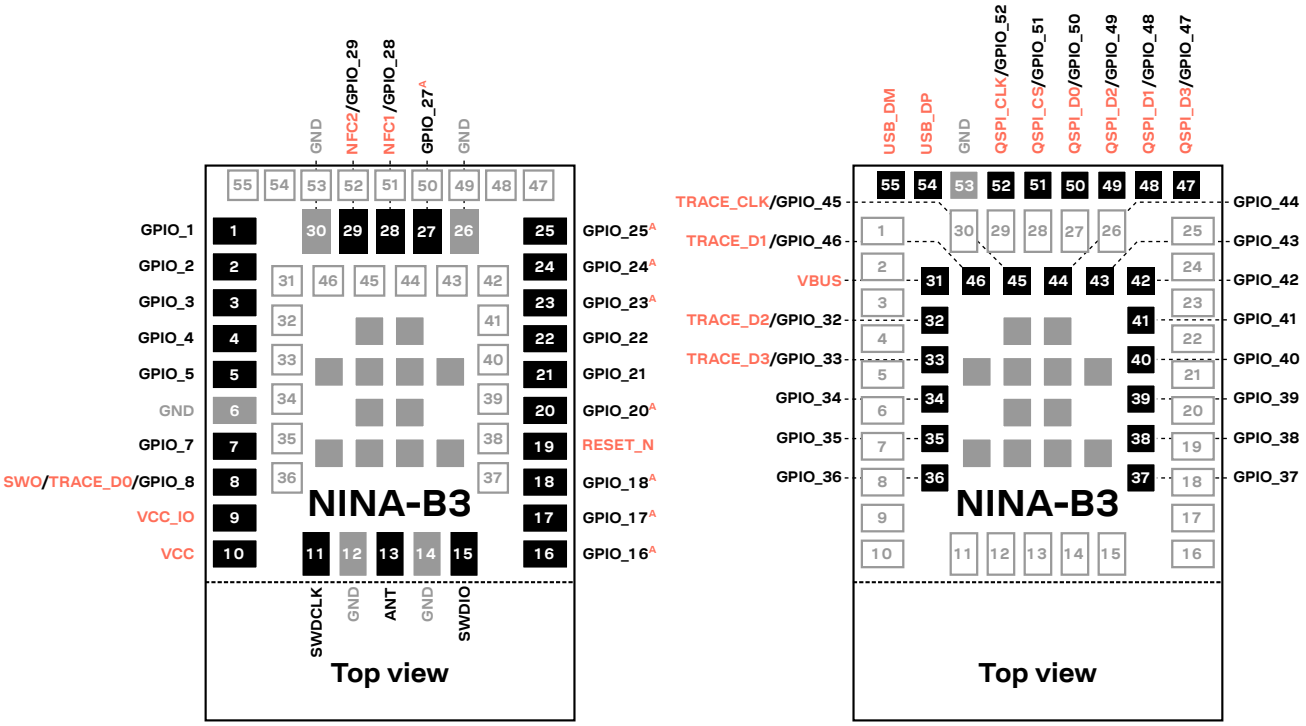
2.9.3 Parallel Trace

The NINA-B30 series modules support parallel trace output as well. This allows output from the Embedded Trace Macrocell (ETM) and Instrumentation Trace Macrocell (ITM) embedded in the Arm Cortex-M4 core of the nRF52840 chip in the NINA-B3. The ETM trace data allows a user to record exactly how the application goes through the CPU instructions in real time. The parallel trace interface uses 1 clock signal and 4 data signals respectively - **TRACE_CLK**, **TRACE_D0**, **TRACE_D1**, **TRACE_D2** and **TRACE_D3**.

3 Pin definition

3.1 NINA-B30 series pin assignment

The pin-out described in Figure 3 is an example assignment that shows the module in an unconfigured state.



A = Analog function capable pin

Figure 3: NINA-B30 series pin assignment (top view)

The grey pins in the center of the modules are GND pins. The outline of NINA-B301 ends at the dotted line as shown in Figure 3, where the antenna area of the NINA-B302 begins.

Most of the digital or analog functions described in this data sheet may be freely assigned to any GPIO pin. Analog functions are limited to analog capable pins. Signals that are highlighted in red in Figure 3 are not freely assignable but locked to a specific pin.

Some GPIO pins are connected to the pins located close to the radio part of the RF chip. Digital noise on these pins can reduce the radio sensitivity.

Do not apply an NFC field to the NFC pins when they are configured as GPIOs as this can cause permanent damage to the module. When driving different logic levels on these pins in the GPIO mode, a small current leakage will occur. Ensure that they are set to the same logic level before entering into any power saving modes. See section 4.2.6 for more information.

No.	Name	I/O	Description	nRF52 pin	Remarks
1	GPIO_1	I/O	General purpose I/O	P0.13	
2	GPIO_2	I/O	General purpose I/O	P0.14	
3	GPIO_3	I/O	General purpose I/O	P0.15	
4	GPIO_4	I/O	General purpose I/O	P0.16	
5	GPIO_5	I/O	General purpose I/O	P0.24	
6	GND	-	Ground		
7	GPIO_7	I/O	General purpose I/O	P0.25	
8	SWO/TRACE_D0/ GPIO_8	I/O	General purpose I/O	P1.00	May be used for parallel/serial trace debug
9	VCC_IO	I	Module I/O level voltage input		Must be connected to VCC on NINA-B3
10	VCC	I	Module supply voltage input		1.7-3.6 V range
11	SWDCLK	I	Serial Wire Debug port clock signal	SWDCLK	
12	GND	-	Ground		
13	ANT	I/O	Tx/Rx antenna interface		50 Ω nominal characteristic impedance, only used with NINA-B3x1 modules
14	GND	-	Ground		
15	SWDIO	I/O	Serial Wire Debug port data signal	SWDIO	
16	GPIO_16	I/O	Analog function enabled GPIO	P0.03	Pin is analog capable, radio sensitive pin[1]
17	GPIO_17	I/O	Analog function enabled GPIO	P0.28	Pin is analog capable, radio sensitive pin[1]
18	GPIO_18	I/O	Analog function enabled GPIO	P0.02	Pin is analog capable, radio sensitive pin[1]
19	RESET_N	I/O	System reset input	P0.18	Active low
20	GPIO_20	I/O	Analog function enabled GPIO	P0.31	Pin is analog capable, radio sensitive pin[1]
21	GPIO_21	I/O	General purpose I/O	P1.12	Radio sensitive pin[1]
22	GPIO_22	I/O	General purpose I/O	P1.13	Radio sensitive pin[1]
23	GPIO_23	I/O	Analog function enabled GPIO	P0.29	Pin is analog capable, radio sensitive pin[1]
24	GPIO_24	I/O	Analog function enabled GPIO	P0.30	Pin is analog capable, radio sensitive pin[1]
25	GPIO_25	I/O	Analog function enabled GPIO	P0.04	Pin is analog capable
26	GND	-	Ground		
27	GPIO_27	I/O	Analog function enabled GPIO	P0.05	Pin is analog capable
28	NFC1/GPIO_28	I/O	NFC pin 1 (default)	P0.09	May be used as a GPIO, radio sensitive pin[1]
29	NFC2/GPIO_29	I/O	NFC pin 2 (default)	P0.10	May be used as a GPIO, radio sensitive pin[1]
30	GND	-	Ground		
31	VBUS	I	USB interface 5 V input	VBUS	Must be connected to 5 V for the USB interface to work
32	TRACE_D2/GPIO_32	I/O	General purpose I/O	P0.11	May be used for parallel trace debug
33	TRACE_D3/GPIO_33	I/O	General purpose I/O	P1.09	May be used for parallel trace debug
34	GPIO_34	I/O	General purpose I/O	P1.08	
35	GPIO_35	I/O	General purpose I/O	P1.01	Radio sensitive pin[1]

No.	Name	I/O	Description	nRF52 pin	Remarks
36	GPIO_36	I/O	General purpose I/O	P1.02	Radio sensitive pin[1]
37	GPIO_37	I/O	General purpose I/O	P1.03	Radio sensitive pin[1]
38	GPIO_38	I/O	General purpose I/O	P1.10	Radio sensitive pin[1]
39	GPIO_39	I/O	General purpose I/O	P1.11	Radio sensitive pin[1]
40	GPIO_40	I/O	General purpose I/O	P1.15	Radio sensitive pin[1]
41	GPIO_41	I/O	General purpose I/O	P1.14	Radio sensitive pin[1]
42	GPIO_42	I/O	General purpose I/O	P0.26	
43	GPIO_43	I/O	General purpose I/O	P0.06	
44	GPIO_44	I/O	General purpose I/O	P0.27	
45	TRACE_CLK/GPIO_45	I/O	General purpose I/O	P0.07	May be used for parallel trace debug
46	TRACE_D1/GPIO_46	I/O	General purpose I/O	P0.12	May be used for parallel trace debug
47	QSPI_D3/GPIO_47	I/O	General purpose I/O	P0.23	Recommended pin for QSPI_D3
48	QSPI_D1/GPIO_48	I/O	General purpose I/O	P0.21	Recommended pin for QSPI_D1
49	QSPI_D2/GPIO_49	I/O	General purpose I/O	P0.22	Recommended pin for QSPI_D2
50	QSPI_D0/GPIO_50	I/O	General purpose I/O	P0.20	Recommended pin for QSPI_D0
51	QSPI_CS/GPIO_51	I/O	General purpose I/O	P0.17	Recommended pin for QSPI_CS
52	QSPI_CLK/GPIO_52	I/O	General purpose I/O	P0.19	Recommended pin for QSPI_CLK
53	GND	-	Ground		
54	USB_DP	I/O	USB differential data signal	USB_DP	
55	USB_DM	I/O	USB differential data signal	USB_DM	
	EGP	-	Exposed Ground Pins		The exposed pins in the center of the module should be connected to GND

Table 7: NINA-B30 series pin-out

[1] It is recommended to keep frequencies below 10 kHz, and only use standard drive strength on these digital pins.

3.2 NINA-B31 series pin assignment (with u-blox connectivity software)

The pin-out as shown in Figure 4 describes the pin configuration used by the u-blox connectivity software.

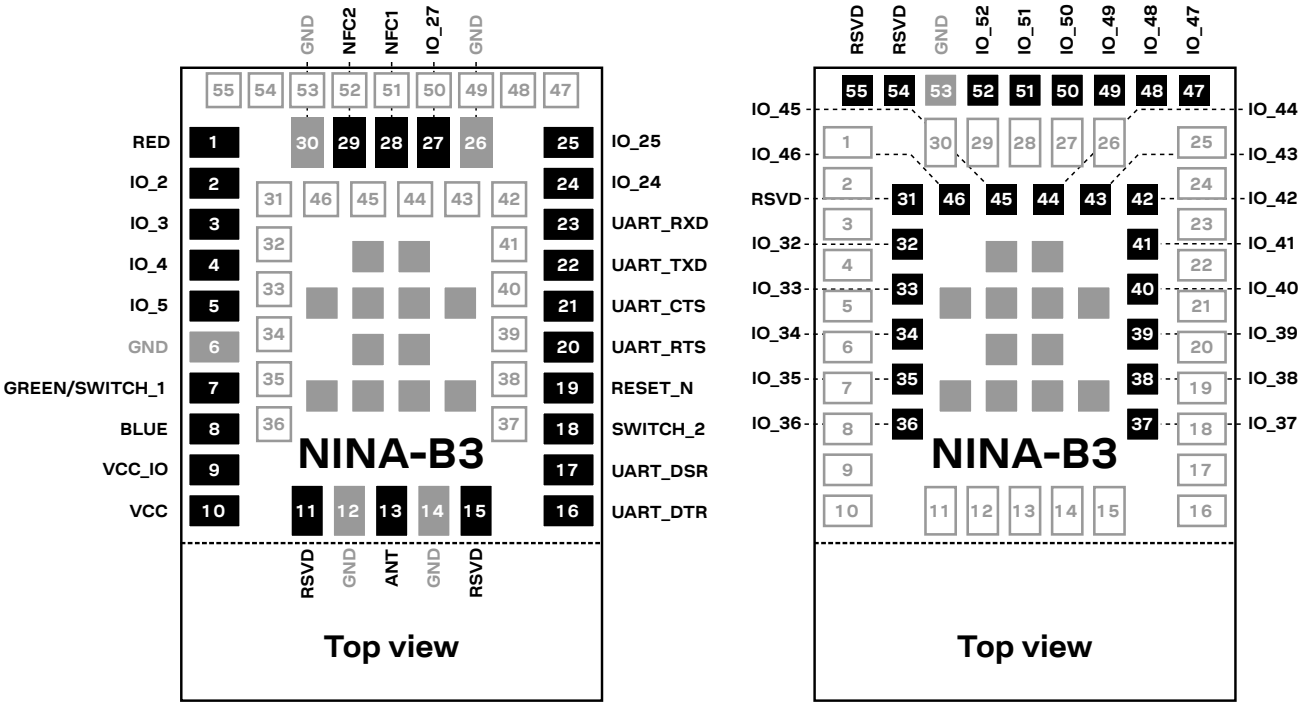


Figure 4: NINA-B31 series pin assignment (top view)

The grey pins in the center of the modules are GND pins. The outline of NINA-B311 ends at the dotted line as shown in Figure 4, where the antenna area of NINA-B312 begins.

⚠ Follow this pin layout when using the u-blox connectivity software. No interfaces can be moved or added.

⚠ Do not apply an NFC field to the NFC pins when they are configured as GPIOs as it can cause permanent damage to the module. While using the u-blox connectivity software, these pins will always be set to the NFC mode. See section 4.2.6 for more information.

No.	Name	I/O	Description	Remarks
1	RED	O	RED system status signal	Active low, should be routed to an RGB LED
2	IO_2	-	u-blox connectivity software (uCS) IO pin	Can be used for manual digital I/O
3	IO_3	-	uCS IO pin	Can be used for manual digital I/O
4	IO_4	-	uCS IO pin	Can be used for manual digital I/O
5	IO_5	-	uCS IO pin	Can be used for manual digital I/O
6	GND	-	Ground	
7	GREEN/SWITCH_1	I/O	This signal is multiplexed: GREEN: System status signal. SWITCH_1: Multiple functions	Active low. GREEN: Should be routed to an RGB LED. SWITCH_1: See section 2.8.3 for more information.
8	BLUE	O	BLUE system status signal	Active low, should be routed to an RGB LED
9	VCC_IO	I	Module I/O level voltage input	Must be connected to VCC on NINA-B3
10	VCC	I	Module supply voltage input	1.7-3.6 V range
11	RSVD	-	RESERVED pin	Leave unconnected
12	GND	-	Ground	
13	ANT	I/O	Tx/Rx antenna interface	50 Ω nominal characteristic impedance, only used with NINA-B3x1 modules
14	GND	-	Ground	
15	RSVD	-	RESERVED pin	Leave unconnected
16	UART_DTR	O	UART data terminal ready signal	Used to indicate system status
17	UART_DSR	I	UART data set ready signal	Used to change the system modes
18	SWITCH_2	I	Multiple functions	Active low, see section 2.8.3 for more information.
19	RESET_N	I	External system reset input	Active low
20	UART_RTS	O	UART request to send control signal	Used only when hardware flow control is enabled
21	UART_CTS	I	UART clear to send control signal	Used only when hardware flow control is enabled
22	UART_TXD	O	UART data output	
23	UART_RXD	I	UART data input	
24	IO_24	-	uCS IO pin	Can be used for manual digital I/O
25	IO_25	-	uCS IO pin	Can be used for manual digital I/O
26	GND	-	Ground	
27	IO_27	-	uCS IO pin	Can be used for manual digital I/O
28	NFC1	I/O	NFC pin 1	
29	NFC2	I/O	NFC pin 2	
30	GND	-	Ground	
31	RSVD	-	RESERVED pin	Leave unconnected
32	IO_32	-	uCS IO pin	Can be used for manual digital I/O
33	IO_33	-	uCS IO pin	Can be used for manual digital I/O
34	IO_34	-	uCS IO pin	Can be used for manual digital I/O
35	IO_35	-	uCS IO pin	Can be used for manual digital I/O
36	IO_36	-	uCS IO pin	Can be used for manual digital I/O
37	IO_37	-	uCS IO pin	Can be used for manual digital I/O
38	IO_38	-	uCS IO pin	Can be used for manual digital I/O
39	IO_39	-	uCS IO pin	Can be used for manual digital I/O
40	IO_40	-	uCS IO pin	Can be used for manual digital I/O
41	IO_41	-	uCS IO pin	Can be used for manual digital I/O

No.	Name	I/O	Description	Remarks
42	IO_42	-	uCS IO pin	Can be used for manual digital I/O
43	IO_43	-	uCS IO pin	Can be used for manual digital I/O
44	IO_44	-	uCS IO pin	Can be used for manual digital I/O
45	IO_45	-	uCS IO pin	Can be used for manual digital I/O
46	IO_46	-	uCS IO pin	Can be used for manual digital I/O
47	IO_47	-	uCS IO pin	Can be used for manual digital I/O
48	IO_48	-	uCS IO pin	Can be used for manual digital I/O
49	IO_49	-	uCS IO pin	Can be used for manual digital I/O
50	IO_50	-	uCS IO pin	Can be used for manual digital I/O
51	IO_51	-	uCS IO pin	Can be used for manual digital I/O
52	IO_52	-	uCS IO pin	Can be used for manual digital I/O
53	GND	-	Ground	
54	RSVD	-	RESERVED pin	Leave unconnected
55	RSVD	-	RESERVED pin	Leave unconnected
	EGP	-	Exposed Ground Pad	The exposed pads in the center of the module should be connected to the GND

Table 8: NINA-B3 series and u-blox connectivity software pin-out

4 Electrical specifications

⚠ Stressing the device above one or more of the ratings listed in the Absolute maximum rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating conditions section of this document should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ Operating condition ranges define those limits within which the functionality of the device is guaranteed. Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Condition	Min	Max	Unit
VCC	Module supply voltage	Input DC voltage at VCC pin	-0.3	3.9	V
V_DIO	Digital pin voltage	Input DC voltage at any digital I/O pin, VCC ≤ 3.6 V	-0.3	VCC + 0.3	V
		Input DC voltage at any digital I/O pin, VCC > 3.6 V	-0.3	3.9	V
P_ANT	Maximum power at receiver	Input RF power at antenna pin		+10	dBm

Table 9: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. The voltage spikes exceeding the power supply voltage specification, provided in Table 9, must be limited to the values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD ratings

Parameter	Min	Typical	Max	Unit	Remarks
ESD sensitivity for all pins except **ANT** pin			4	kV	Human body model according to JEDEC JS001
			750	V	Charged device model according to JESD22-C101
ESD indirect contact discharge			±8	kV	According to EN 301 489-1

Table 10: Maximum ESD ratings

⚠ NINA-B3 series modules are Electrostatic Sensitive Devices and require special precautions while handling. See section 8.4 for ESD handling instructions.

4.2 Operating conditions

☞ Unless otherwise specified, all operating condition specifications are at an ambient temperature of 25 °C and a supply voltage of 3.3 V.

⚠ Operation beyond the specified operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating temperature range

Parameter	Min	Max	Unit
Storage temperature	-40	+125	°C
Operating temperature	-40	+85	°C

Table 11: Temperature range

4.2.2 Supply/Power pins

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input supply voltage	1.7	3.3	3.6	V
t_RVCC	Supply voltage rise time			60	ms
VCC_ripple	VCC input noise peak to peak, 10 - 100 KHz			TBD	mV
	VCC input noise peak to peak, 100 KHz - 1 MHz			TBD	mV
	VCC input noise peak to peak, 1 - 3 MHz			TBD	mV
VCC_IO	I/O reference voltage		VCC		V

Table 12: Input characteristics of voltage supply pins

4.2.3 Current consumption

Table 13 shows the typical current consumption of a NINA-B3 module, independent of the software used.

Mode	Condition	Typical	Peak
Sleep	No clocks running, no RAM data retention	400 nA	
Sleep	No clocks running, 64 kB RAM data retention	880 nA	
Sleep	No clocks running, 256 kB RAM data retention	2.3 µA	
Standby	RTC and 64 kB RAM data retention. System running on 32.768 kHz clock from crystal.	1.3 µA	
Active	CPU running benchmarking tests @ 64 MHz clock speed, all interfaces idle	3.6 mA	
Active	Radio RX only	4.8 mA	
Active	Radio TX only, 0 dBm output power	4.9 mA	
Active	Radio TX only, +8 dBm output power	14.1 mA	
Active	CPU running benchmarking tests @ 64 MHz clock speed, Radio TX 0 dBm output power	9.1 mA	

Table 13: Module VCC current consumption

Table 14 shows the current consumption during some typical use cases when using the u-blox connectivity software:

		3.3 V VCC		1.8 V VCC	
Mode	Condition	Average	Peak	Average	Peak
Active	Advertising 1 s periods with +8 dBm output power and 31 bytes payload, CPU and UART interface is running	0.93 mA	20 mA		
Standby	Advertising 1 s periods with +8 dBm output power and 31 bytes payload	50 uA	19 mA		
Standby	One advertisement event (4.7 ms), +8 dBm output power and 31 bytes payload	4.9 mA	19 mA		
Active	Connected as peripheral, connection events 30 ms periods, +8 dBm output power and 0 bytes payload, CPU and UART interface is running	0.98 mA	20 mA		
Standby	Connected as peripheral, connection events 30 ms periods, +8 dBm output power and 0 bytes payload	110 uA	19 mA		
Sleep	UART DSR pin is used to enter the sleep mode. No RAM retention.	400 nA	4 mA		

Table 14: Current consumption during typical use cases

Mode	Condition	Typical	Peak
Active	USB interface active, current drawn from the VBUS supply	2.4 mA	
Suspended	USB interface suspended, the CPU is sleeping, current drawn from the VBUS supply	262 µA	

Table 15: USB VBUS current consumption

4.2.4 RF performance

Parameter	Test condition	Min	Typ	Max	Unit
Receiver input sensitivity	Conducted at 25 °C, 1 Mbit/s BLE mode		-94		dBm
	Conducted at 25 °C, 2 Mbit/s BLE mode		-91		dBm
	Conducted at 25 °C, 500 kbit/s BLE mode		-97		dBm
	Conducted at 25 °C, 125 kbit/s BLE mode		-100		dBm
Maximum output power	Conducted at 25 °C		+8		dBm

Table 16: RF performance

4.2.5 RESET_N pin

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
RESET_N	Low-level input	0		0.3*VCC	V	
	Internal pull-up resistance		13		kΩ	
	RESET duration			55	ms	Time taken to release a pin reset.

Table 17: RESET_N pin characteristics

4.2.6 Digital pins

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
Any digital pin	Input characteristic: Low-level input	0		0.3*VCC	V	
	Input characteristic: high-level input	0.7*VCC		VCC	V	
	Output characteristic: Low-level output	0		0.4	V	Standard drive strength
		0		0.4	V	High drive strength
	Output characteristic: High-level output	VCC-0.4		VCC	V	Standard drive strength
		VCC-0.4		VCC	V	High drive strength
	Sink/Source current	1	2	4	mA	Standard drive strength
		3			mA	High drive strength, VCC < 2.7 V
		6	9	14	mA	High drive strength, VCC ≥ 2.7 V
	Rise/Fall time		9 – 25		ns	Standard drive strength, depending on load capacitance
			4 – 8		ns	High drive strength, depending on load capacitance
	Input pull-up resistance		13		kΩ	Can be added to any GPIO pin configured as input
	Input pull-down resistance		13		kΩ	Can be added to any GPIO pin configured as input
GPIO_28, GPIO_29	Leakage current		1	4	µA	When not configured for NFC and driven to different logic levels

Table 18: Digital pin characteristics

4.2.7 I²C pull-up resistor values

Symbol	Parameter	Bus capacitance	Min	Typ	Max	Unit
R_PUstandard	External pull-up resistance required on I²C interface in standard mode (100 Kbps)	10 pF	1	-	115	kΩ
		50 pF	1	-	23	kΩ
		200 pF	1	-	6	kΩ
		400 pF	1	-	3	kΩ
R_PUfast	External pull-up resistance required on I²C interface in fast mode (400 Kbps)	10 pF	1	-	35	kΩ
		50 pF	1	-	7	kΩ

Symbol	Parameter	Bus capacitance	Min	Typ	Max	Unit
		200 pF	1	-	1.5	kΩ
		400 pF	1	-	1	kΩ

Table 19: Suggested pull-up resistor values

4.2.8 Analog comparator

Symbol	Parameter	Min	Typ	Max	Unit
I_powersave	Current consumption when the comparator is in 'power save' mode		2		µA
I_balenced	Current consumption when the comparator is in 'balanced' mode		5		µA
I_speed	Current consumption when the comparator is in 'high speed' mode		10		µA
I_lowpower	Current consumption of the low power comparator		0.5		µA
t_powersave	Time to generate interrupt/event when the comparator is in 'power save' mode		0.6		µs
t_balanced	Time to generate interrupt/event when the comparator is in 'balanced' mode		0.2		µs
t_speed	Time to generate interrupt/event when the comparator is in 'high speed' mode		0.1		µs
t_lowpower	Time to generate interrupt/event for the low power comparator		5		µs

Table 20: Electrical specification of the two analog comparators

5 Mechanical specifications

5.1 NINA-B3x1 Mechanical specification

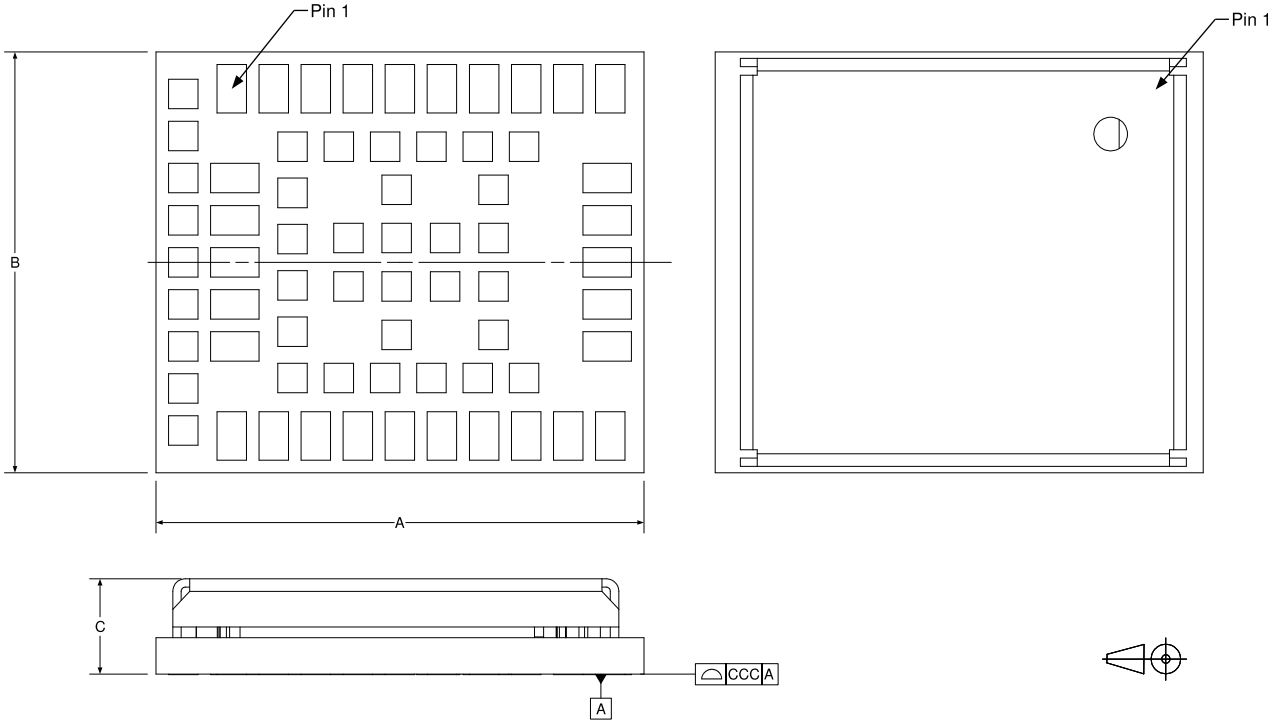


Figure 5: NINA-B3x1 mechanical outline

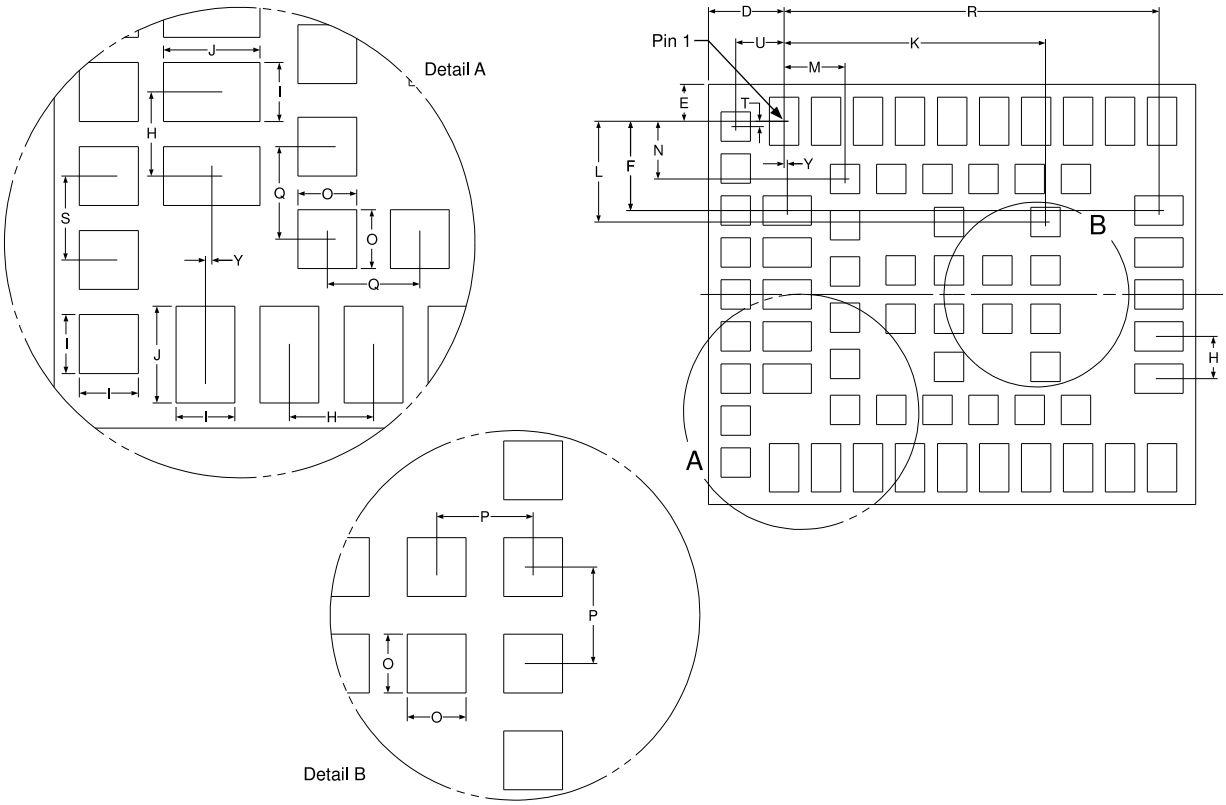


Figure 6: NINA-B3 detailed dimensions

Parameter	Description	Typical [mm]	[mil]	Tolerance [mm]	[mil]
A	Module PCB length	11.6			
B	Module PCB width	10.0			
C	Module thickness	2.23			
ccc	Seating plane coplanarity	0.10			
D	Horizontal edge to pin no. 1 center	1.80			
E	Vertical edge to pin no. 1 center	0.875			
F	Vertical pin no. 1 center to lateral pin center	2.125			
H	Lateral and antenna row pin to pin pitch	1.00			
I	Lateral, antenna row and outer pin width	0.70			
J	Lateral and antenna row pin length	1.15			
K	Horizontal pin no. 1 center to central pin center	6.225			
L	Vertical pin no. 1 center to central pin center	2.40			
M	Horizontal pin no. 1 center to inner row pin center	1.45			
N	Vertical pin no. 1 center to inner row pin center	1.375			
O	Central, inner and outer row pin width and length	0.70			
P	Central pin to central pin pitch	1.15			
Q	Inner row pin to pin pitch	1.10			
R	Horizontal pin no. 1 center to antenna row pin center	8.925			
S	Outer row pin to pin pitch	1.0			
T	Vertical pin no. 1 center to outer row pin center	0.125			
U	Horizontal pin no. 1 center to outer row pin center	1.15			
Y	Horizontal pin no. 1 center to lateral pin center	0.075			
	Module weight [g]	<1.0			

Table 21: NINA-B3x1 mechanical outline data

5.2 NINA-B3X2 Mechanical specifications

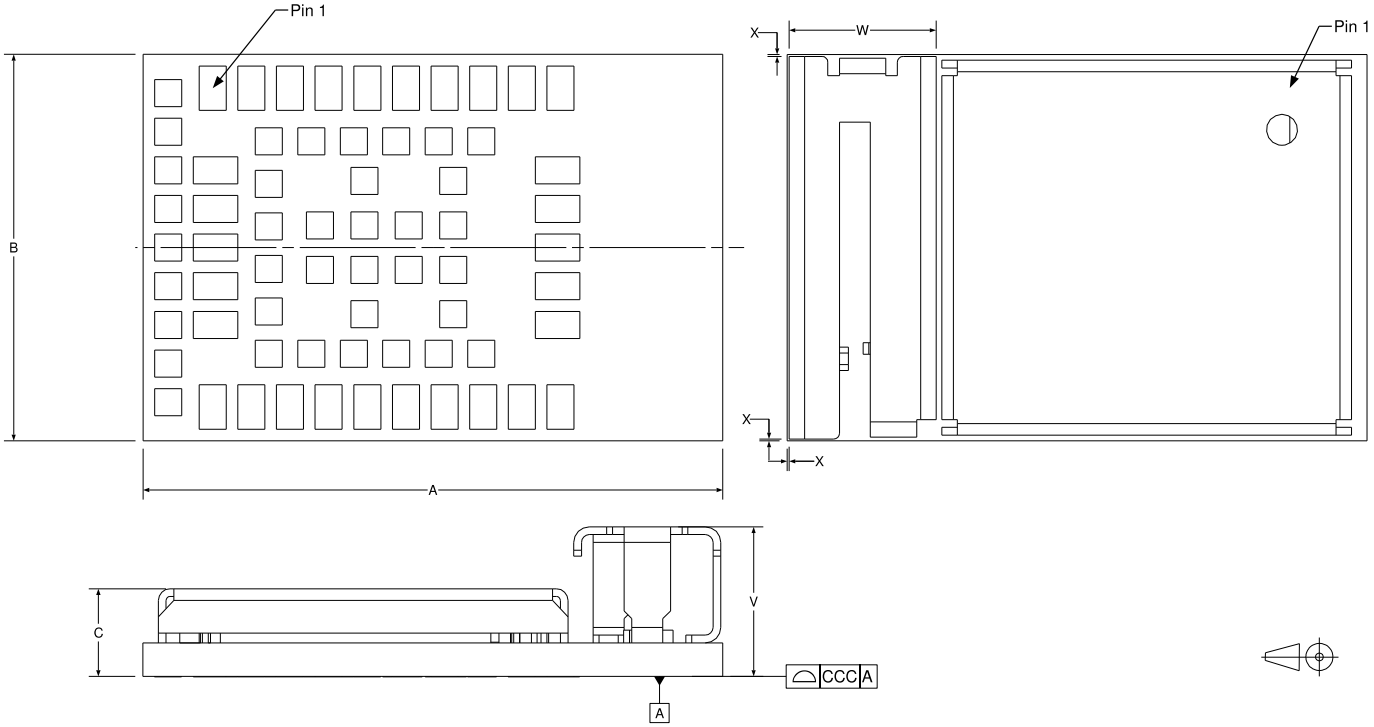


Figure 7: NINA-B3X2 mechanical outline

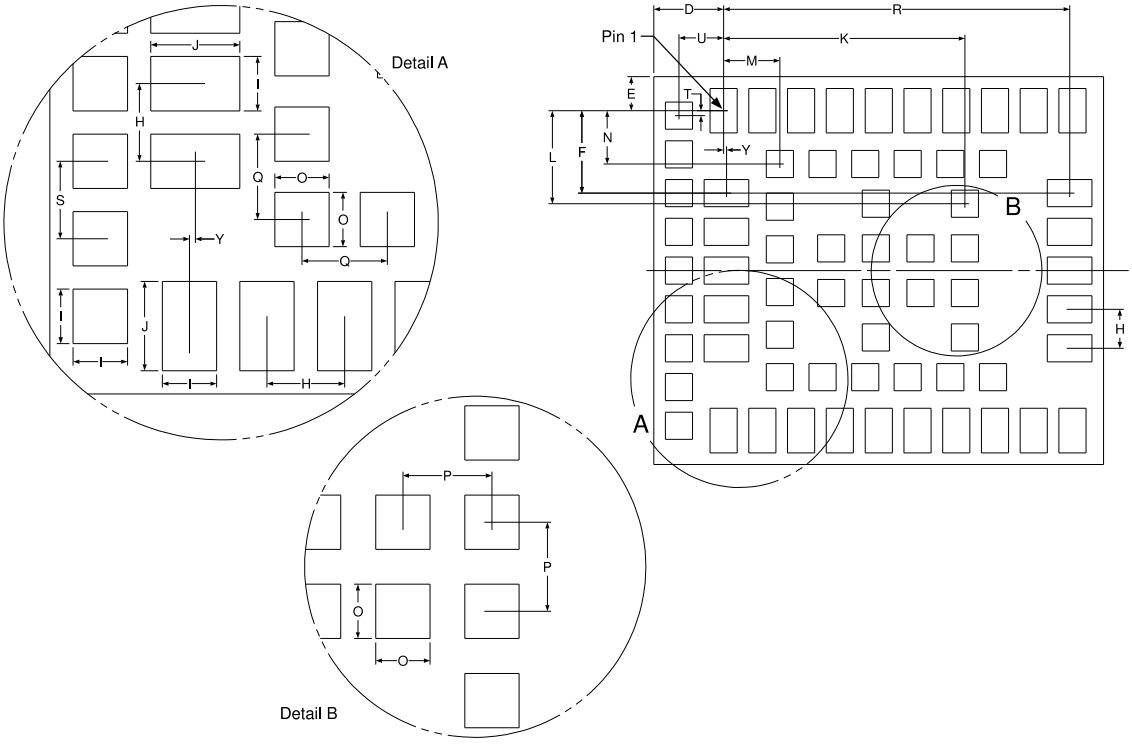


Figure 8: NINA-B3 detailed dimensions

Parameter	Description	Typical [mm]	[mil]	Tolerance [mm]	[mil]
A	Module PCB length	15			
B	Module PCB width	10.0			
C	Module thickness	2.23			
ccc	Seating plane coplanarity	0.10			
D	Horizontal edge to pin no. 1 center	1.80			
E	Vertical edge to pin no. 1 center	0.875			
F	Vertical pin no. 1 center to lateral pin center	2.125			
H	Lateral and antenna row pin to pin pitch	1.00			
I	Lateral, antenna row and outer pin width	0.70			
J	Lateral and antenna row pin length	1.15			
K	Horizontal pin no. 1 center to central pin center	6.225			
L	Vertical pin no. 1 center to central pin center	2.40			
M	Horizontal pin no. 1 center to inner row pin center	1.45			
N	Vertical pin no. 1 center to inner row pin center	1.375			
O	Central, inner and outer row pin width and length	0.70			
P	Central pin to central pin pitch	1.15			
Q	Inner row pin to pin pitch	1.10			
R	Horizontal pin no. 1 center to antenna row pin center	8.925			
S	Outer row pin to pin pitch	1.0			
T	Vertical pin no. 1 center to outer row pin center	0.125			
U	Horizontal pin no. 1 center to outer row pin center	1.15			
V	PCB and antenna thickness	3.83			
W	Module antenna width	3.8			
X	Antenna overhang outside module outline on any side	0.0		+0.60	
Y	Horizontal pin no. 1 center to lateral pin center	0.075			
	Module weight [g]	<1.0			

Table 22: NINA-B3X2 mechanical outline data

6 Qualification and approvals

6.1 Country approvals

The NINA-B3 modules are certified for use in the following countries/regions:

- Europe
- USA
- Canada
- Japan (pending)
- Taiwan (pending)
- South Korea (pending)
- Brazil (pending)
- Australia (pending)
- New Zealand (pending)
- South Africa (pending)

☞ See the NINA-B3 series System Integration Manual [3] for detailed information about the regulatory requirements that must be met when using NINA-B3 modules in an end product.

6.2 Bluetooth qualification

The NINA-B3 module series have been qualified as an end product according to the Bluetooth 5.0 specification.

Product type	QD ID	Listing Date
End product	TBD	TBD

Table 23: NINA-B3 series Bluetooth qualified design ID

7 Antennas

This section is moved to the NINA-B3 series System Integration Manual [3].

8 Product handling

8.1 Packaging

The NINA-B3 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the u-blox Package Information Guide [1].

8.1.1 Reels

The NINA-B3 modules are deliverable in quantities of 500 pieces on a reel. The reel types for the NINA-B3 modules are provided in Table 24 and detailed information about the reel types are described in the u-blox Package Information Guide [1].

Model	Reel Type
NINA-B3x1	B1
NINA-B3x2	A3

Table 24: Reel types for different models of the NINA-B3 series

8.1.2 Tapes

Figure 9 shows the position and orientation of the NINA-B3 modules as they are delivered on tape.

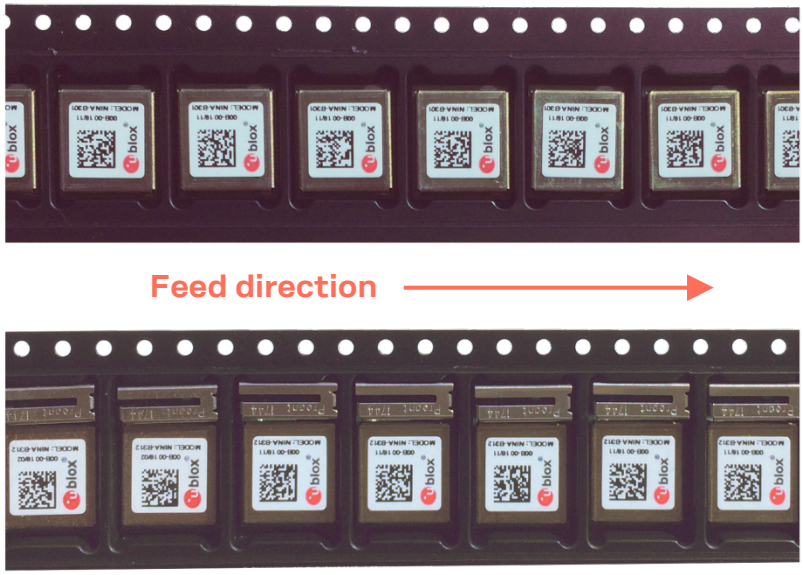


Figure 9: Orientation of NINA-B3 modules on tape

8.2 Moisture sensitivity levels

⚠ The NINA-B3 series modules are Moisture Sensitive Devices (MSD) in accordance with the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the required packaging and handling precautions. The NINA-B3 series modules are rated at MSL level 4. For more information regarding moisture sensitivity levels, labeling and storage, see the u-blox Package Information Guide [1].

☞ For MSL standards, see IPC/JEDEC J-STD-020, which can be downloaded from www.jedec.org.

8.3 Reflow soldering

Reflow profiles are selected according to u-blox recommendations. See NINA-B3 series System Integration Manual [3] for more information.

⚠ Failure to observe these recommendations can result in severe damage to the device.

8.4 ESD precautions

⚠ The NINA-B3 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling the NINA-B3 series modules without proper ESD protection may destroy or damage them permanently.

The NINA-B3 series modules are electrostatic sensitive devices (ESD) and require special ESD precautions typically applied to the ESD sensitive components. Section 4.1.1 provides the maximum ESD ratings of the NINA-B3 series modules.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the NINA-B3 series module.

⚠ Failure to observe these recommendations can result in severe damage to the device.

9 Labeling and ordering information

9.1 Product labeling

The labels of the NINA-B3 series modules include important product information as described in this section.

Figure 14 illustrates the label of the NINA-B3 series modules, which includes the u-blox logo, production lot, product type number, and certification numbers (if applicable).

Figure 14: Location of product type number on the NINA-B3 series module label

Reference	Description
1	Date of unit production (year/week)
2	Product version
3	Product name
4	Data Matrix with unique serial number of 19 alphanumeric symbols. The first 3 symbols represent module type number unique to each module variant, the next 12 symbols represent the unique hexadecimal Bluetooth address of the module AABBCCDDEEFF, and the last 4 symbols represent the hardware and firmware version encoded HHFF.

Table 25: NINA-B3 series label description

9.2 Explanation of codes

Three different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and software versions. Table 26 below details these three different formats:

Format	Structure
Product Name	PPPP-TGVV
Ordering Code	PPPP -TGVV-TTQ
Type Number	PPPP -TGVV-TTQ-XX

Table 26: Product code formats

Table 27 explains the parts of the product code.

Code	Meaning	Example
PPPP	Form factor	NINA
TG	Platform (Technology and Generation) T – Dominant technology, for example, W: Wi-Fi, B: Bluetooth G - Generation	B3: Bluetooth Generation 3
VV	Variant based on the same platform; range [00…99]	11: default configuration, with antenna pin
TT	Major product version	00: first revision
Q	Quality grade A: Automotive B: Professional C: Standard	B: professional grade
XX	Minor product version (not relevant for certification)	Default value is 00

Table 27: Part identification code

9.3 Ordering information

Ordering Code	Product
NINA-B311-00B	NINA-B3 module with antenna pin, pre-flashed and locked for use with u-blox connectivity software
NINA-B312-00B	NINA-B3 module with internal antenna, pre-flashed and locked for use with u-blox connectivity software
NINA-B301-00B	NINA-B3 module with antenna pin, open CPU for custom applications
NINA-B302-00B	NINA-B3 module with internal antenna, open CPU for custom applications

Table 28: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to Digital Converter
BLE	Bluetooth Low Energy
BPF	Band Pass Filter
CTS	Clear To Send
EDM	Extended Data mode
ESD	Electro Static Discharge
FCC	Federal Communications Commission
GATT	Generic ATTribute profile
GPIO	General Purpose Input/Output
IC	Industry Canada
I^2C	Inter-Integrated Circuit
MCU	Micro Controller Unit
MSD	Moisture Sensitive Device
QSPI	Quad Serial Peripheral Interface
RTS	Request To Send
SPI	Serial Peripheral Interface
TBD	To be Defined
UART	Universal Asynchronous Receiver/Transmitter

Table 29: Explanation of the abbreviations and terms used

Related documents

[1] u-blox Package Information Guide, document number UBX-14001652
[2] u-blox Short Range AT Commands Manual, document number UBX-14044127
[3] NINA-B3 Series System Integration Manual, document number UBX-15026175
[4] NINA-B31 Getting Started, document number UBX-18022394

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Comments
R01	10-Nov-2017	ajoh, apet, kgom	Initial release.
R02	8-Jun-2018	ajoh, kgom	Removed Arm Mbed software option. Updated the mechanical specification (Section 5). Updated RF parameters such as output power and receiver sensitivity (Table 3). Added current consumption data when running the u-blox connectivity software (Table 14).
R03	13-Sep-2018	ajoh, kgom	Changed the product status to Initial Production. Updated Table 1 and Table 2. In Table 22, modified the module PCB length to 15. Included information about Drive strength in GPIO (section 2.7.1) and limitations of the radio sensitive pins in section 3.1. Added some digital pin characteristics in section 4.2.6. Moved certification, qualification and antenna information (previously sections 6 and 7) to the NINA-B3 System Integration Manual.

Contact

For complete contact information, visit us at www.u-blox.com.

u-blox Offices

North, Central and South America

u-blox America, Inc.

Phone: +1 703 483 3180
E-mail: info_us@u-blox.com

Regional Office West Coast:

Phone: +1 408 573 3640
E-mail: info_us@u-blox.com

Technical Support:

Phone: +1 703 483 3185
E-mail: support@u-blox.com

Headquarters
Europe, Middle East, Africa

u-blox AG

Phone: +41 44 722 74 44
E-mail: info@u-blox.com
Support: support@u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.

Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office Australia:

Phone: +61 2 8448 2016
E-mail: info_anz@u-blox.com
Support: support_ap@u-blox.com

Regional Office China (Beijing):

Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Chongqing):

Phone: +86 23 6815 1588
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shanghai):

Phone: +86 21 6090 4832
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shenzhen):

Phone: +86 755 8627 1083
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office India:

Phone: +91 80 405 092 00
E-mail: info_in@u-blox.com
Support: support_in@u-blox.com

Regional Office Japan (Osaka):

Phone: +81 6 6941 3660
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Japan (Tokyo):

Phone: +81 3 5775 3850
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Korea:

Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:

Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com