LM74700-Q1 Low I_Q Reverse Polarity Protection Ideal Diode Controller

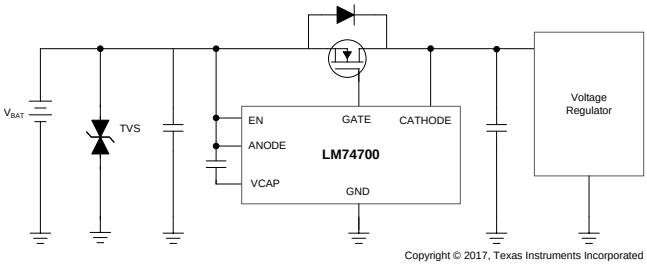
1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- 3 V to 65 V Input Range
- –65 V Reverse Voltage Rating
- Charge Pump for External N-Channel MOSFET
- 20 mV ANODE to CATHODE Forward Voltage Drop Regulation
- Enable Pin Feature
- 3 µA Shutdown Current (EN=Low)
- 60 µA Operating Quiescent Current (EN=High)
- 1.5-A Peak Gate Turnoff Current
- Fast Response to Reverse Current Blocking: < 1 µs
- Meets Automotive ISO7637 Transient Requirements With a Suitable TVS Diode
- 6-Pin SOT-23 Package 2.90 mm × 1.60 mm

2 Applications

- Automotive Battery Regulation
- Industrial Power Supplies
- Telecom and Datacom Systems
- Battery Powered System
- Active ORing for Redundant Power

Typical Application Schematic



3 Description

The LM74700-Q1 ideal diode controller operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low loss reverse polarity protection. The wide supply input range of 3 to 65 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from negative supply voltages down to –65 V. With a low $R_{DS(ON)}$ external N-channel MOSFET, a very low forward voltage drop can be achieved while minimizing the amount of power dissipated in the MOSFET. For low load currents, the forward voltage is regulated to 20-mV to enable graceful shutdown of the MOSFET. External MOSFETs with 5 V or lower threshold voltage are recommended. With the enable pin low, the controller is off and draws approximately 3-µA of current.

The LM74700-Q1 controller provides a charge pump gate drive for an external N-channel MOSFET. The high voltage rating of LM74700-Q1 helps to simplify the system designs for automotive ISO7637 protection. Fast response to Reverse Current Blocking makes the device suitable for systems with output voltage holdup requirements during ISO7637 pulse testing as well as power fail and brownout conditions. The LM74700-Q1 is also suitable for ORing applications or AC rectification.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM74700-Q1	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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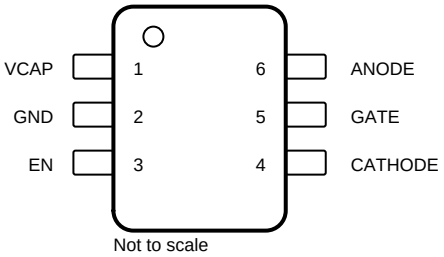
4 Revision History

Changes from Original (October 2017) to Revision A	Page
• Multiple changes made throughout Data Sheet	1

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Not to scale

Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	VCAP	O	Charge pump output. Connect to external charge pump capacitor
2	GND	G	Ground pin
3	EN	I	Enable pin. Can be connected to ANODE.
4	CATHODE	I	Cathode of the diode. Connect to the drain of the external N-channel MOSFET
5	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET
6	ANODE	I	Anode of the diode and input power. Connect to the source of the external N-channel MOSFET.

(1) I = Input, O = Output, G = GND

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	ANODE to GND	–65	65	V
Input Pins	EN to GND, $V_{(ANODE)}$ > 0 V	–0.3	65	V
Input Pins	EN to GND, $V_{(ANODE)}$ ≤ 0 V	$V_{(ANODE)}$	(65 + $V_{(ANODE)}$)	V
Output Pins	GATE to ANODE	–0.3	20	V
Output Pins	VCAP to ANODE	–0.3	16.5	V
Input to Output Pins	ANODE to CATHODE	–75	0.6	V
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (VCAP, EN, ANODE, CATHODE)	±750	
			Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input Pins	ANODE to GND	–60		60	V
	CATHODE to GND			60	
	EN to GND	–60		60	
Input to Output pins	ANODE to CATHODE	–70			V
T_J	Operating junction temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM74700-Q1 DBV (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	103.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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6.5 Electrical Characteristics

V_{ANODE} =12V, V_{CAP} – V_{ANODE} =10V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ANDODE} SUPPLY VOLTAGE						
V_{ANODE}	Operating input voltage		4		60	V
V_{ANODE} POR	Supply Voltage Charge pump enabled	V_{EN} = 3.3V			4	V
V_{ANODE} POR	Minimum operating supply voltage	V_{EN} = 3.3V	2.8	3	3.2	V
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V		3	15	µA
I_Q	Operating Quiescent Current	V_{EN} = 3.3V		60		µA
ENABLE INPUT						
V_{IL}	Enable input low threshold		0.5	1	1.1	V
V_{IH}	Enable input high threshold		1.2	2	2.5	
I_{IH}	Enable sink current	V_{EN} = 12V		5	8	µA
V_{ANODE} to $V_{CATHODE}$						
$V_{AK(REG)}$	Regulated Forward V_{AK} Threshold		12	20	34	mV
V_{AK}	V_{AK} threshold for full conduction mode		37	50	55	mV
V_{AK}	V_{AK} threshold for revere current blocking		–15	–12	–5	mV
Gm	Regulation Error AMP Transconductance		1600	2300	2900	µA/V
GATE DRIVE						
I_{GATE}	Peak source current	V_{ANODE} – $V_{CATHODE}$ = 100mV, V_{GATE} – V_{ANODE} = 5V	5	7		mA
I_{GATE}	Peak sink current	V_{ANODE} – $V_{CATHODE}$ = –20mV, V_{GATE} – V_{ANODE} = 5V		1500		mA
RDS_{ON}	discharge switch RDS_{ON}	V_{ANODE} – $V_{CATHODE}$ = –20mV, V_{GATE} – V_{ANODE} = 100mV	0.8		2.8	Ω
V_{GATE}	Gate drive Voltage (V_{GATE} – V_{ANODE})				15	V
CHARGE PUMP						
I_{CAP}	Charge Pump source current (Charge pump on)	V_{CAP} – V_{ANODE} = 7V	180	370	600	µA
	Charge Pump sink current (Charge pump off)	V_{CAP} – V_{ANODE} = 12.5V		5	10	µA
V_{CAP} – V_{ANODE}	Charge pump turn on voltage		11.5	11.8	12.1	V
V_{CAP} – V_{ANODE}	Charge pump turn off voltage		12.7	13.1	13.5	V
V_{CAP} – V_{ANODE}	V_{CAP} – V_{ANODE} UV release at rising edge	V_{ANODE} – $V_{CATHODE}$ = 100mV	5.8	6.6	7.7	V
V_{CAP} – V_{ANODE}	V_{CAP} – V_{ANODE} UV threshold at falling edge	V_{ANODE} – $V_{CATHODE}$ = 100mV	5.4	5.5	5.7	V
CATHODE						
$I_{CATHODE}$	CATHODE sink current	V_{ANODE} =12V, V_{ANODE} – $V_{CATHODE}$=100mV		1.5	2	µA
		V_{ANODE} =12V, V_{ANODE} – $V_{CATHODE}$= –100mV		1.5	2	µA
		V_{ANODE} = –12V, $V_{CATHODE}$ =12V		0	1	µA

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	EN (low to high) to I_{GATE} delay				100	µs
$T_{reverse\ reconvery}$	Time from reverse voltage detection to I_{GATE} sink	V_{ANODE} – $V_{CATHODE}$ = 100mV to –100mV		0.5	0.75	µs

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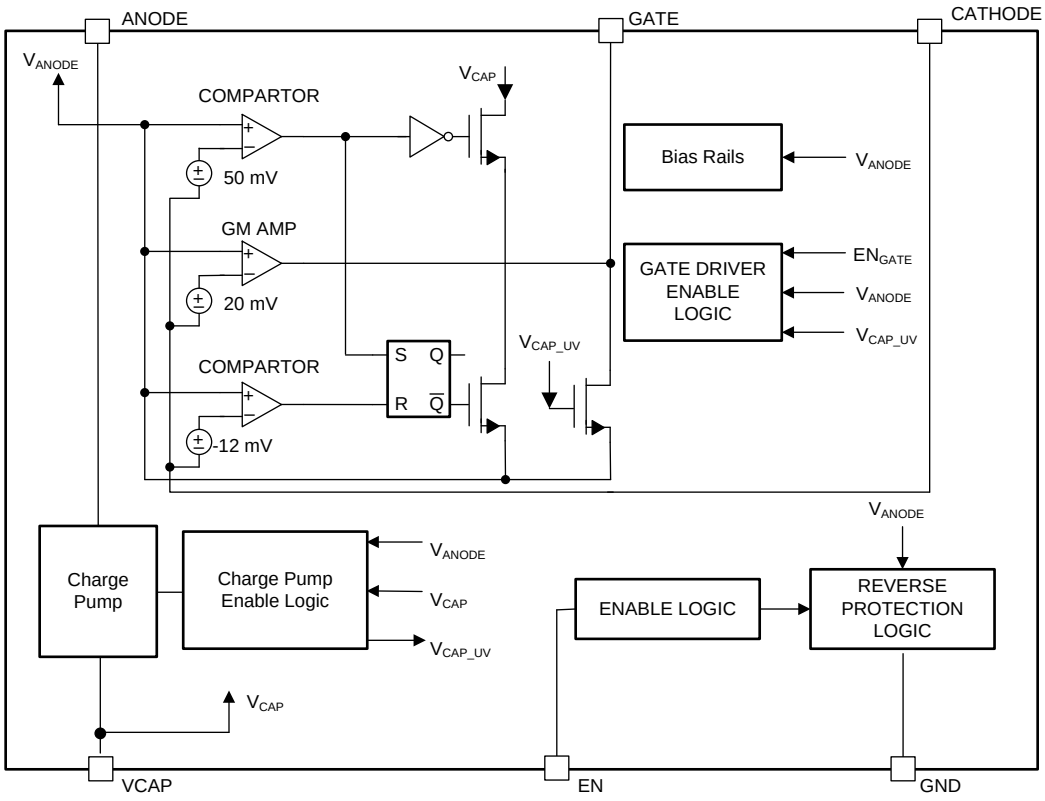
7 Detailed Description

7.1 Overview

The LM74700-Q1 ideal diode controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit or be used in an ORing configuration while minimizing the number of external components. This easy to use ideal diode controller is paired with an external N-channel MOSFET to replace other reverse polarity schemes such as a P-channel MOSFET or a Schottky diode. An internal charge pump is used to drive the external N-Channel MOSFET to a maximum gate drive voltage of approximately 15 V. The voltage drop across the MOSFET is continuously monitored between the ANODE and CATHODE pins, and the GATE to ANODE voltage is adjusted as needed to drive the N-channel MOSFET. During light load currents, the forward voltage drop of the N-channel MOSFET is regulated to 20 mV. At heavier load conditions, the MOSFET is fully enhanced and the voltage drop is proportional to the load current and $R_{DS(ON)}$ of the selected MOSFET. A reverse current condition is detected when there is –12 mV between the ANODE and CATHODE pin, resulting in the GATE pin being internally connected to the ANODE pin turning off the external N-channel MOSFET, and using the body diode to block any of the reverse current. An enable pin (EN) is available to place the LM74700-Q1 in shutdown mode disabling the N-Channel MOSFET and minimizing the quiescent current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage

The ANODE pin is used to power the LM74700-Q1's internal circuitry, typically drawing 60 µA when enabled and 3 µA when disabled. If the ANODE pin voltage is greater then specified minimum operating voltage, the LM74700-Q1 operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from ANODE to GND is designed to vary from 65 V to –65 V, allowing the LM74700-Q1 to withstand negative voltage transients or inputs from an AC source.

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Feature Description (continued)

7.3.2 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external capacitor is placed between VCAP and ANODE to provide energy allowing the external MOSFET to be turned on quickly. In order for the charge pump to supply current to the external capacitor, the ANODE to GND voltage must be greater than the specified minimum operating voltage, and the EN pin must be above the specified input high threshold. If both of these conditions are not achieved, the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP to ANODE voltage must be above the undervoltage lockout threshold, typically 6.6 V, before the internal gate driver is enabled. To remove any chatter on the gate drive approximately 600 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to ANODE voltage reaches 13.1 V, typically, at which point the charge pump is disabled decreasing the current draw on the ANODE pin. The charge pump remains disabled until the VCAP to ANODE voltage is below to 11.8 V typically at which point the charge pump is enabled. The voltage between VCAP and ANODE continue to charge and discharge between 11.8 V and 13.1 V as shown in Figure 1. By enabling and disabling the charge pump, the operating quiescent current of the LM74700-Q1 is reduced. When the charge pump is enabled it sources a charging current of 370µA typical and when disabled it sinks 5µA typical.

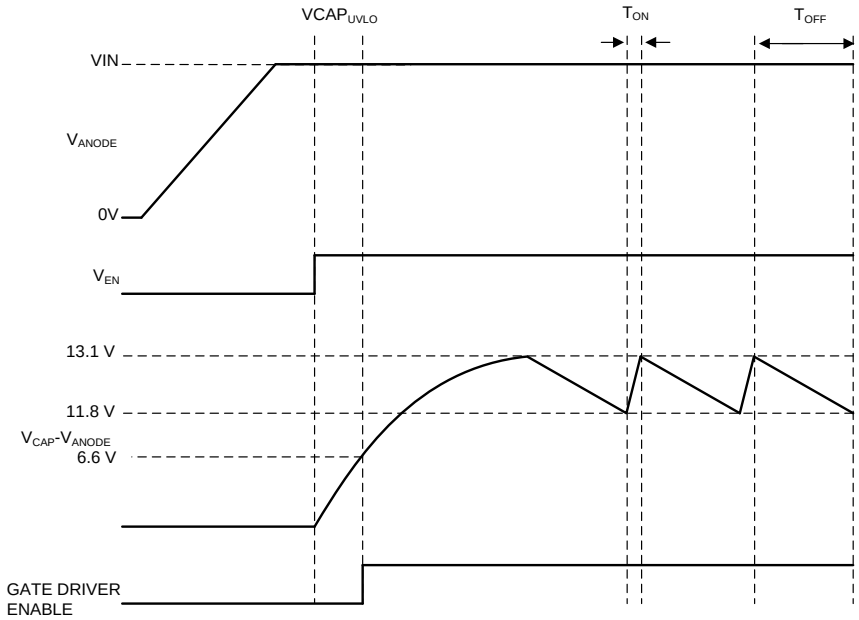

Figure 1. Charge Pump Operation

7.3.3 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the GATE to ANODE voltage to the corresponding mode of operation. There are three defined modes of operation that the gate driver operates under forward regulation, full conduction mode and reverse current protection, according to the ANODE to CATHODE voltage. Forward regulation mode, full conduction mode and reverse current protection mode are described in more detail in the *Regulated Conduction Mode*, *Full Conduction Mode* and *Reverse Current Protection Mode* sections. Figure 2 depicts how the modes of operation vary according to the ANODE to CATHODE voltage of the LM74700-Q1. The threshold between forward regulation mode and conduction mode is when the ANODE to CATHODE voltage is 50 mV. The threshold between forward regulation mode and reverse current protection mode is when the ANODE to CATHODE voltage is –12 mV.

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Feature Description (continued)

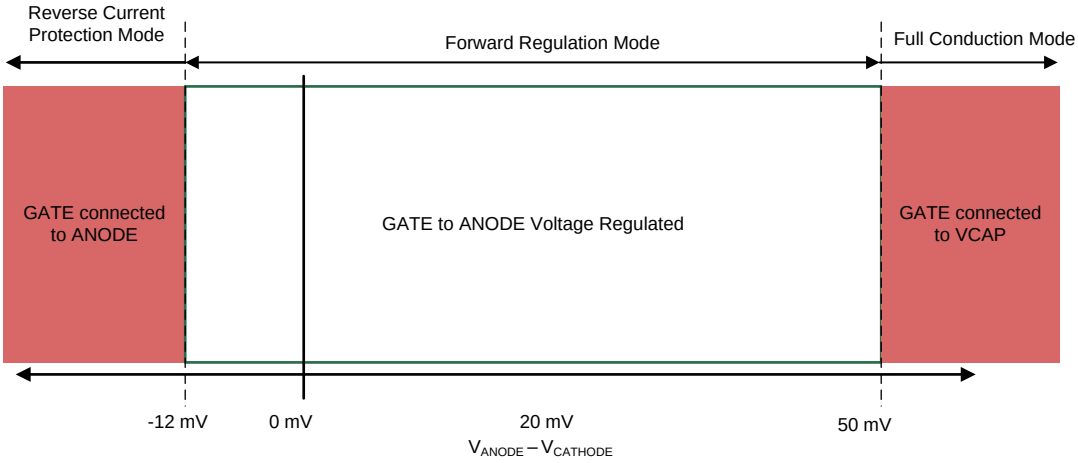

Figure 2. Gate Driver Mode Transitions

Before the gate driver is enabled the three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP to ANODE voltage must be greater than the undervoltage lockout voltage.
- The ANODE voltage must be greater than the specified minimum operating voltage.

If all three conditions are not achieved, the GATE pin is internally connected to the ANODE pin, assuring that the external MOSFET is disabled. Once these conditions are achieved the gate driver operates in the correct mode depending on the ANODE to CATHODE voltage.

7.3.4 Enable

The LM74700-Q1 has an available enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in *Gate Driver* and *Charge Pump* sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74700-Q1 in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as little at –65 V. This allows for the EN pin to be connected directly to the ANODE pin if enable functionality is not needed. It is not recommended to leave the EN pin floating.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The LM74700-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold or the ANODE to GND voltage is below the minimum operating voltage. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the LM74700-Q1 enters low I_Q operation with the ANODE pin only sinking 3 µA and the CATHODE pin sinking less than 1 µA. When the LM74700-Q1 is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the MOSFET's body diode.

7.4.2 Conduction Mode

Conduction mode occurs when the gate driver is enabled. There are three regions of operating during conduction mode based on the ANODE to CATHODE voltage of the LM74700-Q1. Each of the three modes is described in the *Regulated Conduction Mode*, *Full Conduction Mode* and *Reverse Current Protection Mode* sections.

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Device Functional Modes (continued)

7.4.2.1 Regulated Conduction Mode

For the LM74700-Q1 to operate in regulated conduction mode, the gate driver must be enabled as described in the *Gate Driver* section and the current from source to drain of the external MOSFET must be within the range to result in an ANODE to CATHODE voltage drop of –12 mV to 50 mV. During forward regulation mode the ANODE to CATHODE voltage is regulated to 20 mV by adjusting the GATE to ANODE voltage. By regulation this voltage the power loss of the external MOSFET can be minimized while resulting in fast turnoff in result of any reverse current.

7.4.2.2 Full Conduction Mode

For the LM74700-Q1 to operate in full conduction mode the gate driver must be enabled as described in the *Gate Driver* section and the current from source to drain of the external MOSFET must be large enough to result in an ANODE to CATHODE voltage drop of greater than 50 mV typical. If these conditions are achieved the GATE pin is internally connected to the VCAP pin resulting in the GATE to ANODE voltage being approximately the same as the VCAP to ANODE voltage. By connecting VCAP to GATE the external MOSFET's $R_{DS(ON)}$ is minimized reducing the power loss of the external MOSFET when forward currents are large.

7.4.2.3 Reverse Current Protection Mode

For the LM74700-Q1 to operate in reverse current protection mode, the gate driver must be enabled as described in the *Gate Driver* section and the current of the external MOSFET must be flowing from the drain to the source. When the ANODE to CATHODE voltage is typically less than –12 mV reverse current protection mode is entered and the GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM74700-Q1 is used with N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the typical application is shown in Figure 3 where the LM74700-Q1 is used in series with a battery to drive the MOSFET Q1. The TVS is not required for the LM74700-Q1. However, they are used to clamp the positive and negative voltage surges. The output capacitor C_{OUT} is recommended to protect the immediate output voltage collapse as a result of line disturbance.

8.1.1 Typical Application

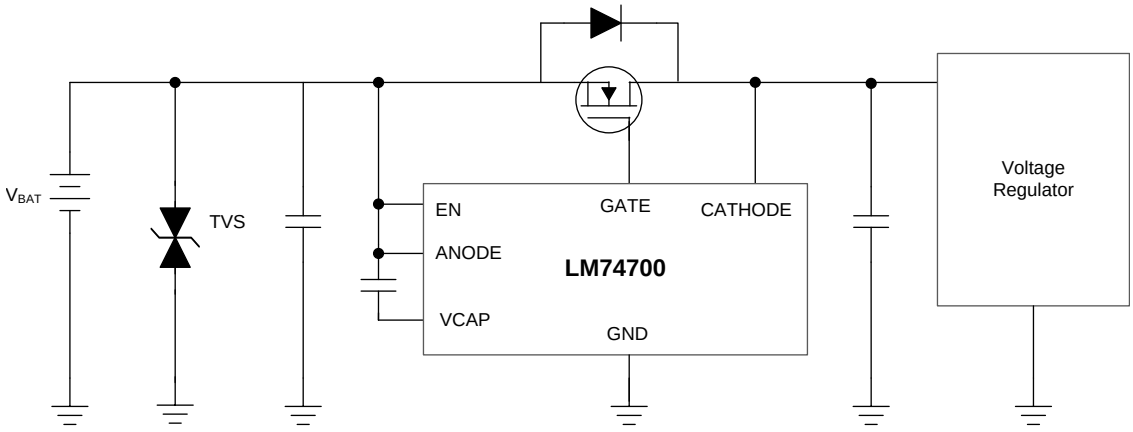

Figure 3. Typical Application Circuit

8.1.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	Max V_{DS} of the MOSFET
Output voltage	Max V_{DS} of the MOSFET
Output current range	Maximum drain current
Output capacitance	47 µF

8.1.1.2 Detailed Design Procedure

To begin the design process, determine the following:

8.1.1.2.1 Design Considerations

- Input voltage range
- Output current range
- MOSFET Gate threshold voltage

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8.1.1.2.2 MOSFET Selection

The LM74700-Q1 can provide up to 15 V of gate to source voltage (V_{GS}). The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, and the drain-to-source On resistance R_{DSON}. The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. It is recommended to use MOSFETs with voltage rating up to 60 V with the LM74700-Q1.

8.1.1.3 Application Curves

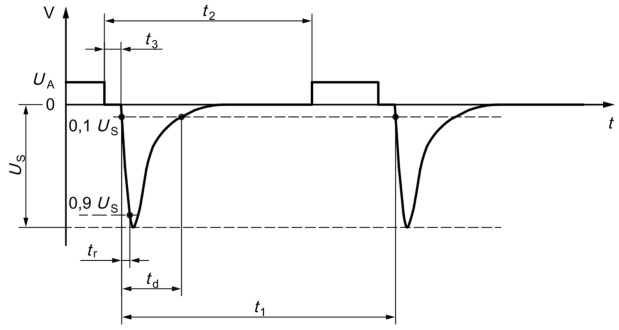

Figure 4. ISO Pulse 1 Test Setup

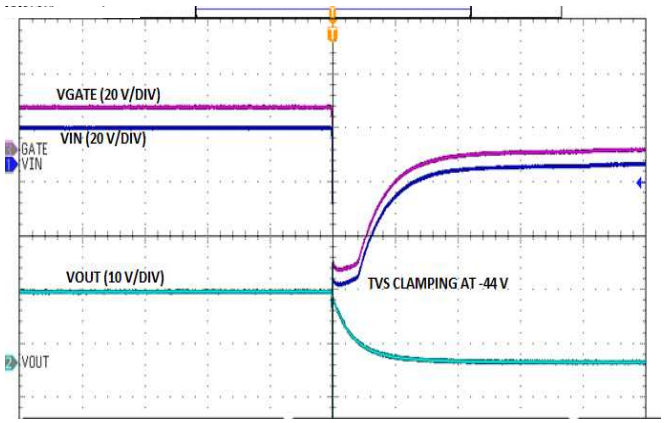

Figure 5. Response to ISO 1

8.1.2 Selection of TVS Diodes in Automotive Reverse Polarity Applications

TVS diodes can be used in automotive systems for protection against transients. In the application circuit show in Figure 6, a bi-directional TVS diode is used to clamp for positive pulses as seen in load dump and clamp for negative pulses such as seen in the ISO specs.

There are two important specs: breakdown voltage and clamping voltage. Breakdown voltage is the voltage at which the TVS diode goes into avalanche similar to a zener diode and is specified at a low current value typical 1 mA. Clamping voltage is the voltage the TVS diode clamps to in high current pulse situations.

In the case of an ISO 7637-2 pulse 1, the voltages go to –150 V with a generator impedance of 10 Ω. This translates to 15 A flowing through the TVS - and the voltage across the TVS would be close to its clamping voltage. A rule of thumb with TVS diode voltage selection is that the breakdown voltage should be higher than worst case steady state voltages seen in the system. TVS diodes are meant to clamp pulses and not meant for steady state voltages.

The value of breakdown voltage of the TVS should be higher than 24 V which is a commonly used battery for jump start and the clamping voltage of the TVS should be upto ± 60 V.

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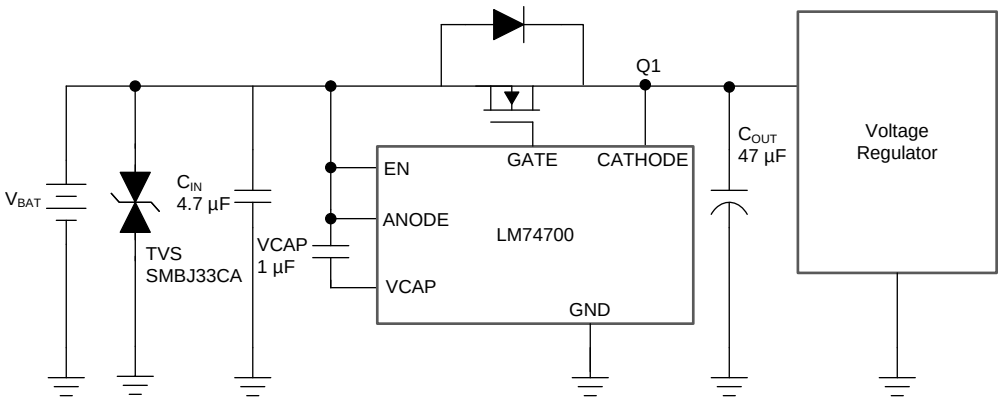

Figure 6. Typical Application with input Voltage Clamping

The second criterion is that the abs max rating for reverse voltage of the LM74700 is not exceeded (–75 V).

In case of reverse voltage pulses such as in ISO specs, the LM74700 turns the MOSFET off. When the MOSFET turns off the voltage seen by the LM74700, Anode to Cathode is - (clamping voltage of TVS (plus) the output capacitor voltage). If the max voltage on output capacitors is 16 V, then the clamping voltage of the TVS- should not exceed, 75 V – 16 V = 59 V.

SMBJ33CA TVS diode can be used for TVS. The breakdown voltage and clamping voltage of TVS 36.7 V and 53.3 V meets criteria one and two.

As far as power levels for TVS diodes the 'B' in the SMBJ stands for 600 W peak power levels. This is sufficient for ISO 7637-2 pulses and suppressed load dump case (ISO-16750-2 pulse B). For unsuppressed load dumps (ISO-16750-2 pulse A) higher power TVS diodes such as SMCJ or SMDJ may be required.

8.2 Application Limitations

This section highlights some limitations in the application which were identified during bench evaluation of the existing LM74700-Q1 silicon on the evaluation module (EVM).

8.2.1 ISO7637-2:2011(E) Pulse 1 Performance

Due to very fast input voltage slew rate during the ISO7637-2:2011 Pulse 1 test, level 4 (–150 V) the device gets stressed and loses the reverse current blocking feature and forward regulation scheme.

TI recommends to use at least 4.7 µF capacitor across ANODE to GND in the designs that undergo this test. Testing has shown that 4.7 µF input capacitor fixes the issue in this test.

A design fix will be included in the final release of the IC.

9 Power Supply Recommendations

The LM74700-Q1 Ideal Diode Controller designed for the supply voltage range of 3 V ≤ V_{ANODE} ≤ 65 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 0.1 µF is recommended. To prevent LM74700-Q1 and surrounding components from damage under the conditions of a direct output short circuit, it is necessary to use a power supply having over load and short circuit protection.

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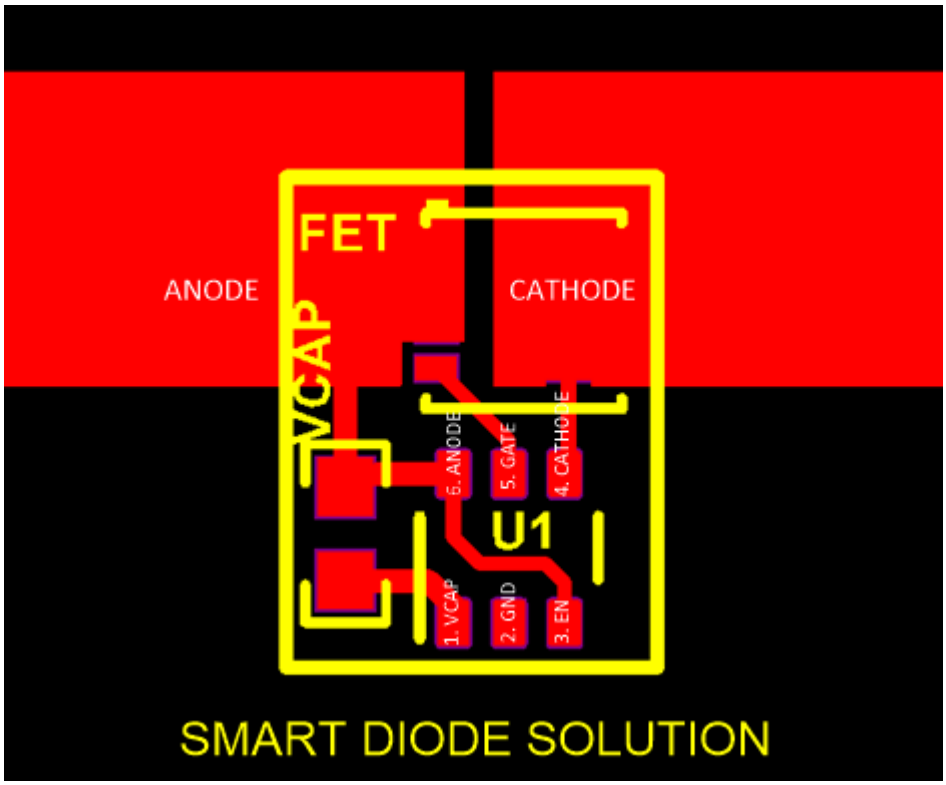
10 Layout

10.1 Layout Guidelines

- Connect ANODE, GATE and CATHODE pins of LM74700-Q1 close to the MOSFET's SOURCE, GATE and DRAIN pins.
- The high current path of for this solution is through the MOSFET, therefore it is important to use thick traces for source and drain of the MOSFET to minimize resistive losses.
- The charge pump capacitor V_{CAP} must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The Gate Drive and Gate pull down pins of the LM74700-Q1 must be connected to the MOSFET gate without using vias. Avoid excessively thin traces to the Gate Drive.
- Obtaining acceptable performance with alternate layout schemes is possible, however the layout shown in the *Layout Example* is intended as a guideline and to produce good results.
- Keep the GATE Drive pin close to the MOSFET to avoid further reduce MOSFET turn-off delay.

10.2 Layout Example



ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74700QDBVRQ1	PREVIEW	SOT-23	DBV	6	2500	TBD	Call TI	Call TI	-40 to 125		
LM74700QDBVTQ1	PREVIEW	SOT-23	DBV	6	250	TBD	Call TI	Call TI	-40 to 125		
PLM74700QDBVTQ1	ACTIVE	SOT-23	DBV	6	250	TBD	Call TI	Call TI	-40 to 125	XB0R	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

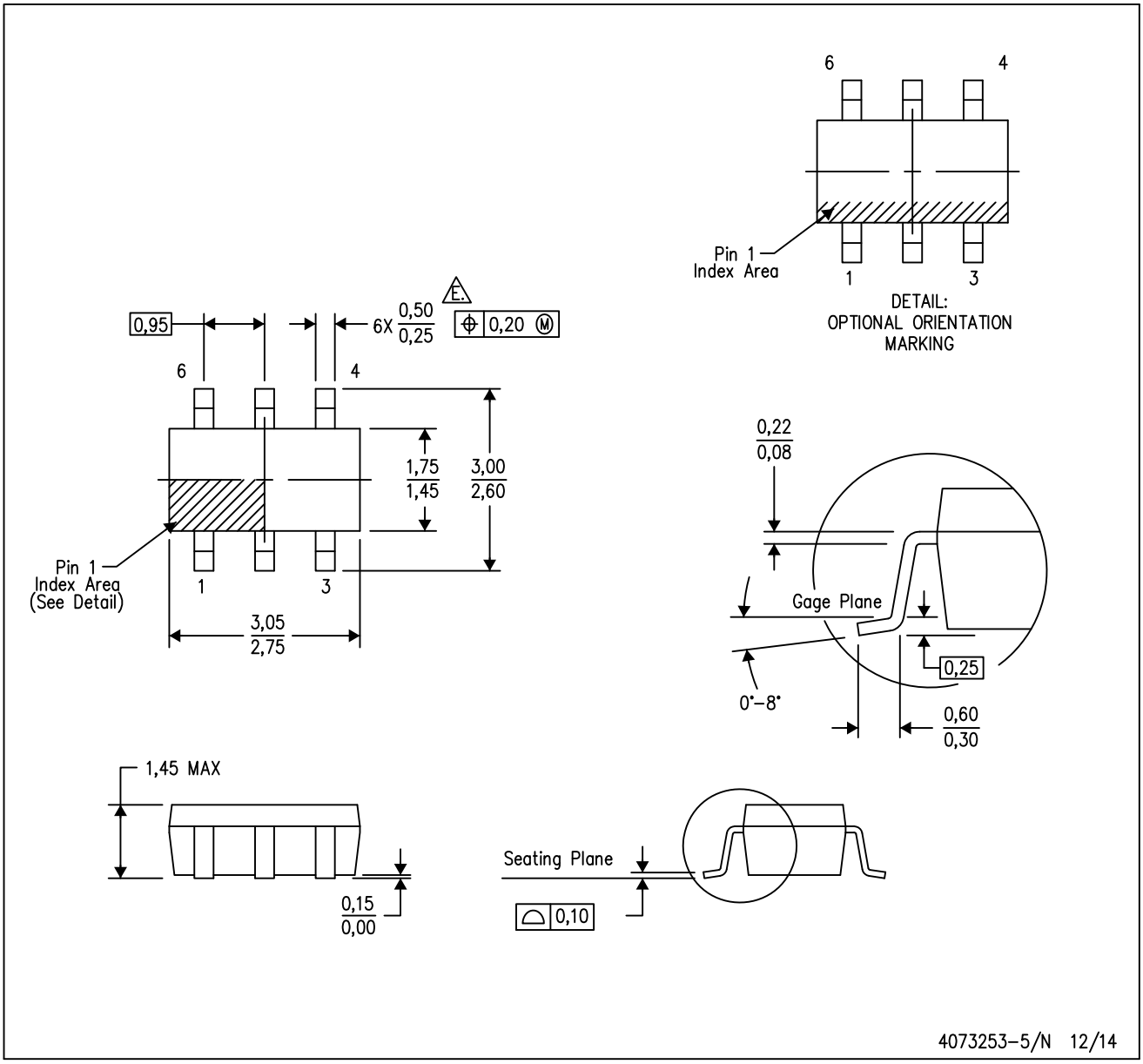
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

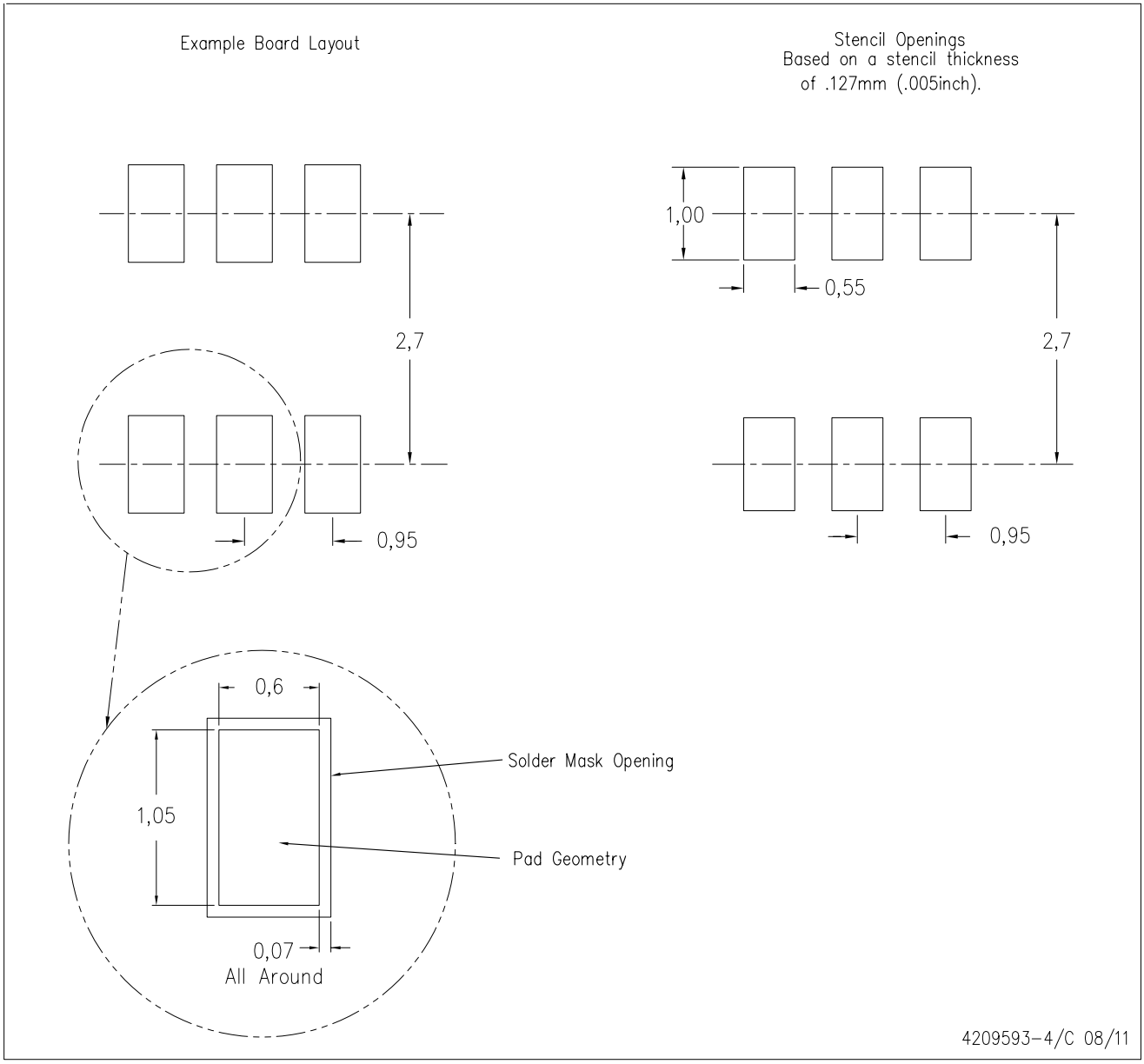
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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