



Dual P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^d	Q_g (Typ.)
- 40	0.027 at $V_{GS} = - 10$ V	- 8	21.7 nC
	0.034 at $V_{GS} = - 4.5$ V	- 7.2	

FEATURES

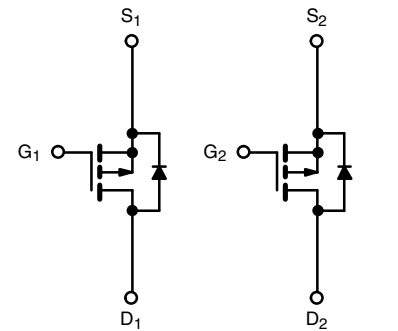
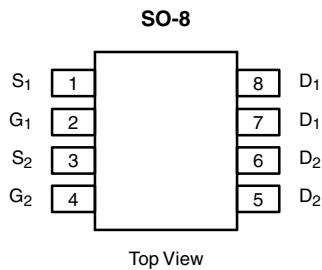
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switches
- Notebook PCs
- Desktop PCs



P-Channel MOSFET P-Channel MOSFET

Ordering Information: Si4909DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	- 8.0	A
	$T_C = 70^\circ\text{C}$	- 6.5	
	$T_A = 25^\circ\text{C}$	- 6.4 ^{a, b}	
	$T_A = 70^\circ\text{C}$	- 5.1 ^{a, b}	
Pulsed Drain Current	I_{DM}	- 30 ^e	
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	- 2.6	
	$T_A = 25^\circ\text{C}$	- 1.6 ^{a, b}	
Avalanche Current	I_{AS}	- 20	
Single-Pulse Avalanche Energy	E_{AS}	20	mJ
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	3.2	W
	$T_C = 70^\circ\text{C}$	2.1	
	$T_A = 25^\circ\text{C}$	2.0 ^{a, b}	
	$T_A = 70^\circ\text{C}$	1.28 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R_{thJA}	47	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Foot	R_{thJF}	29	38	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under steady state conditions is 110°C/W .
- Based on $T_C = 25^\circ\text{C}$.
- Limited by package.

Si4909DY

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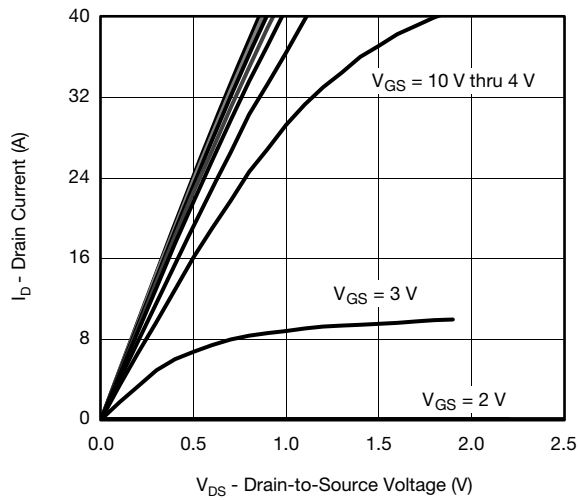
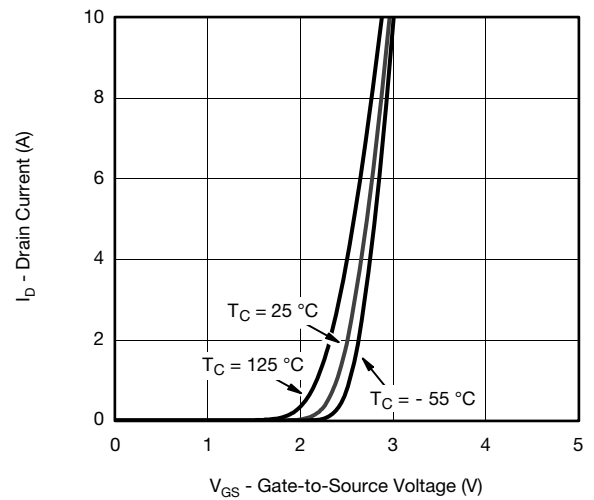
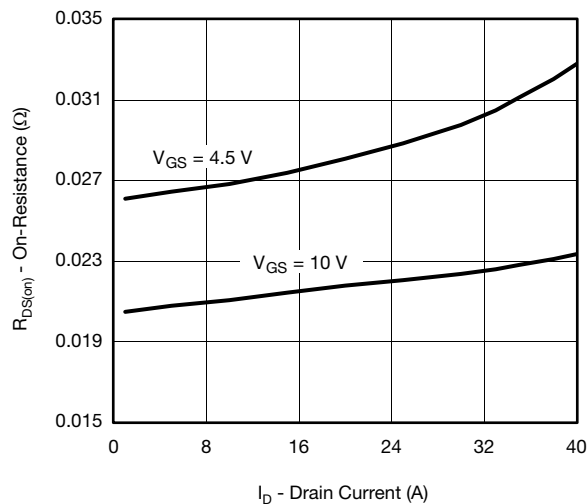
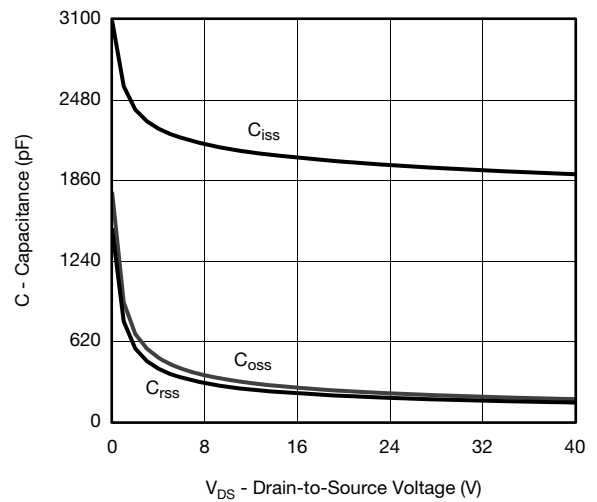
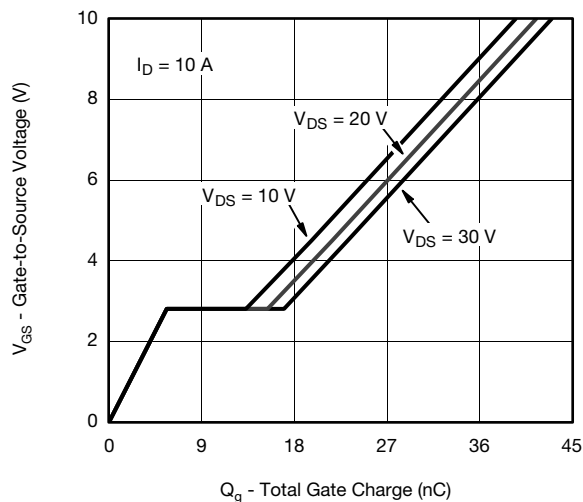
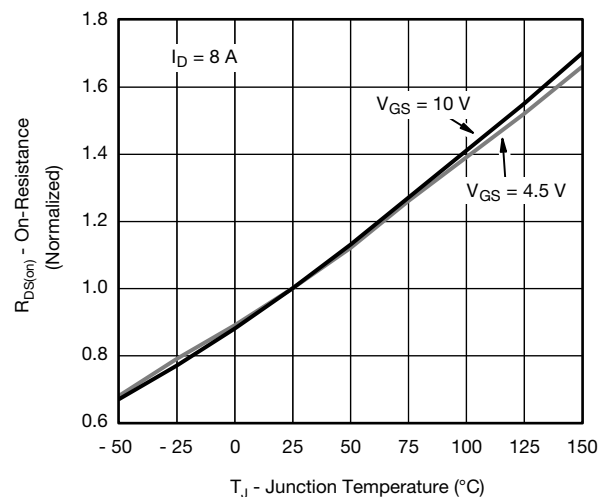
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 40			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 34		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			4.8		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1.2		- 2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 40 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 40 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ - 10 V, V _{GS} = - 10 V	- 20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 8 A		0.021	0.027	Ω
		V _{GS} = - 4.5 V, I _D = - 5 A		0.027	0.034	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 8 A		22		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 20 V, V _{GS} = 0 V, f = 1 MHz		2000		pF
Output Capacitance	C _{oss}			240		
Reverse Transfer Capacitance	C _{rss}			202		
Total Gate Charge	Q _g	V _{DS} = - 20 V, V _{GS} = - 10 V, I _D = - 10 A		41.5	63	nC
		V _{DS} = - 20 V, V _{GS} = - 4.5 V, I _D = - 10 A		21.7	33	
Gate-Source Charge	Q _{gs}			5.6		
Gate-Drain Charge	Q _{gd}			9.8		
Gate Resistance	R _g	f = 1 MHz	1.5	6	12	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 20 V, R _L = 2 Ω I _D ≡ - 10 A, V _{GEN} = - 10 V, R _g = 1 Ω		10	20	ns
Rise Time	t _r			9	18	
Turn-Off DelayTime	t _{d(off)}			50	90	
Fall Time	t _f			13	26	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 20 V, R _L = 2 Ω I _D ≡ - 10 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		42	75	
Rise Time	t _r			40	70	
Turn-Off DelayTime	t _{d(off)}			40	70	
Fall Time	t _f			18	35	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			- 2.6	A
Pulse Diode Forward Current	I _{SM}				- 30	
Body Diode Voltage	V _{SD}	I _S = - 2 A, V _{GS} = 0 V		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 2 A, dl/dt = 100 A/μs, T _J = 25 °C		41	80	ns
Body Diode Reverse Recovery Charge	Q _{rr}			32	65	nC
Reverse Recovery Fall Time	t _a			15		ns
Reverse Recovery Rise Time	t _b			26		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

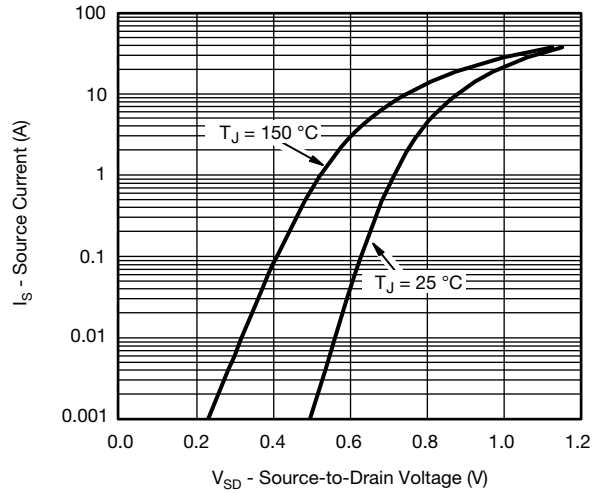
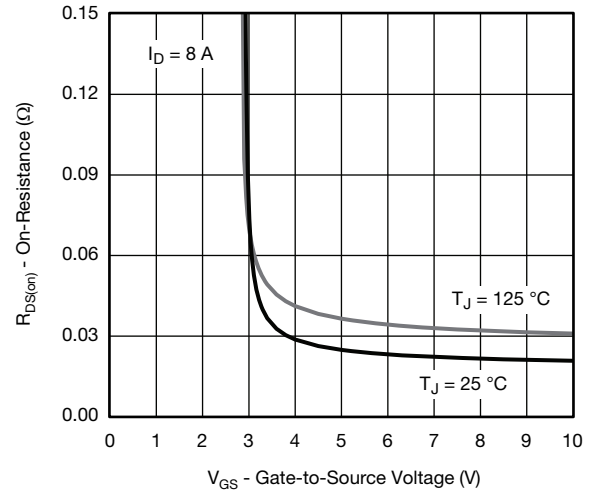
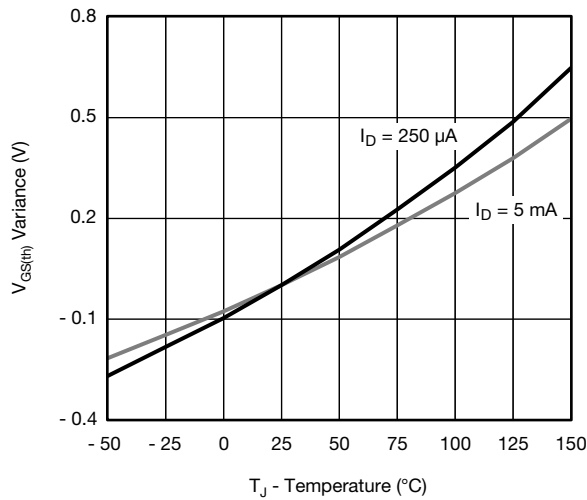
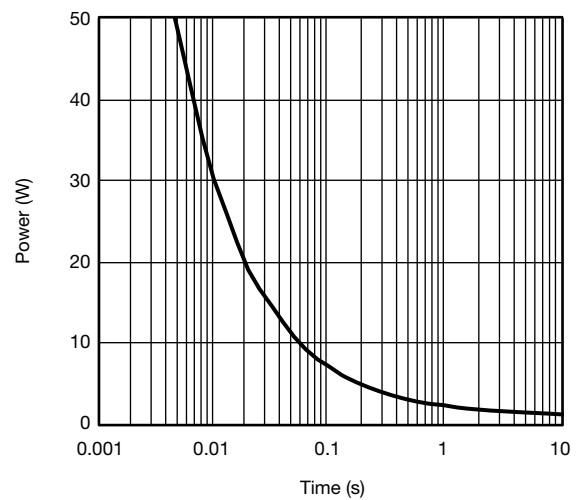
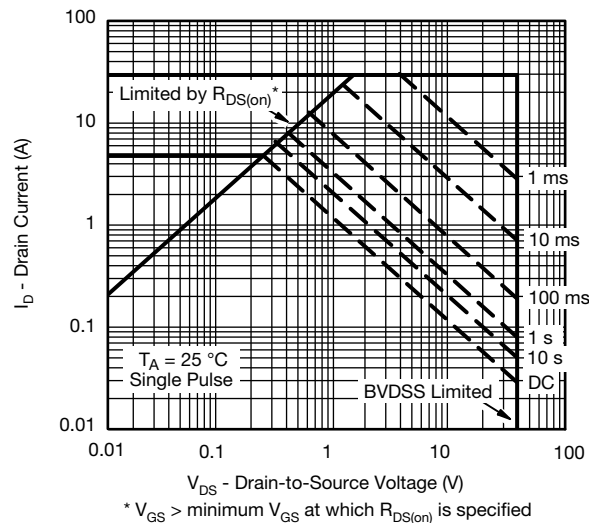
b. Guaranteed by design, not subject to production testing.

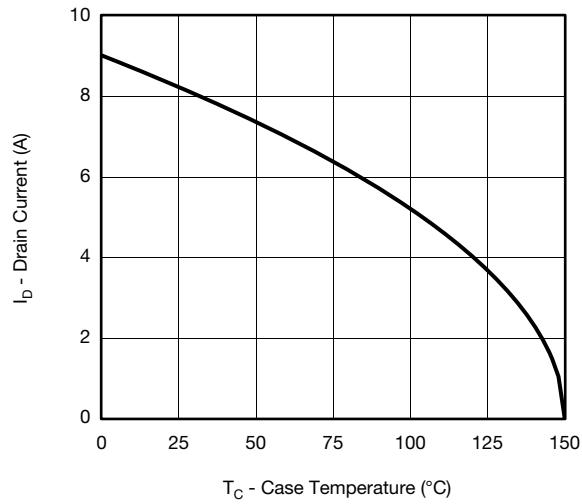
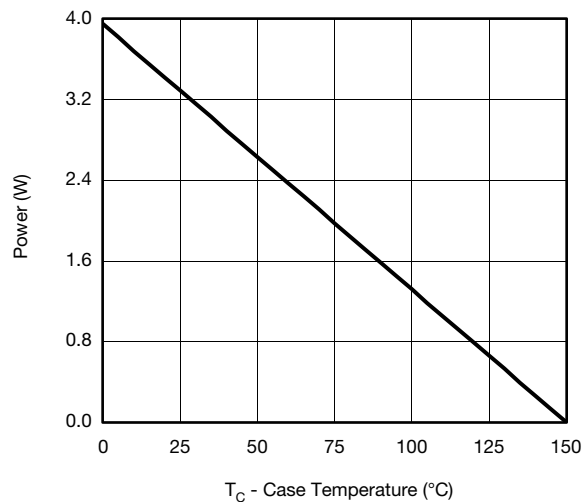
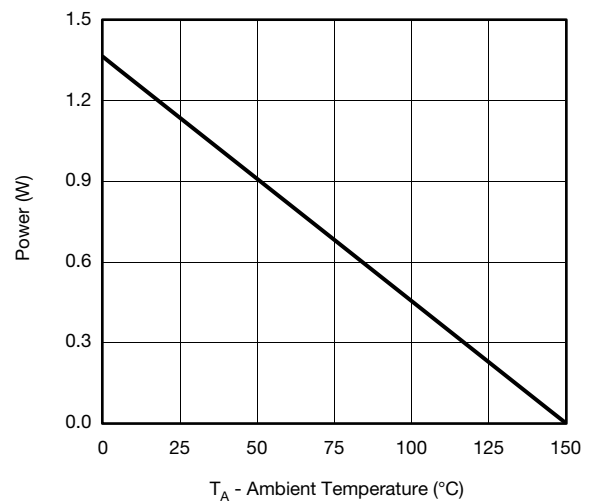
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

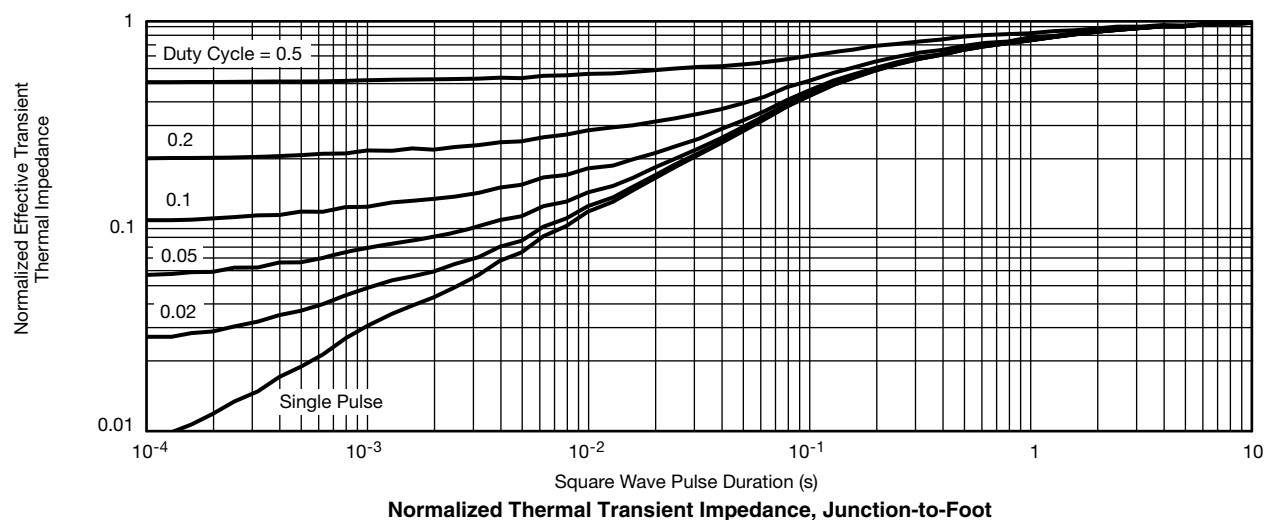
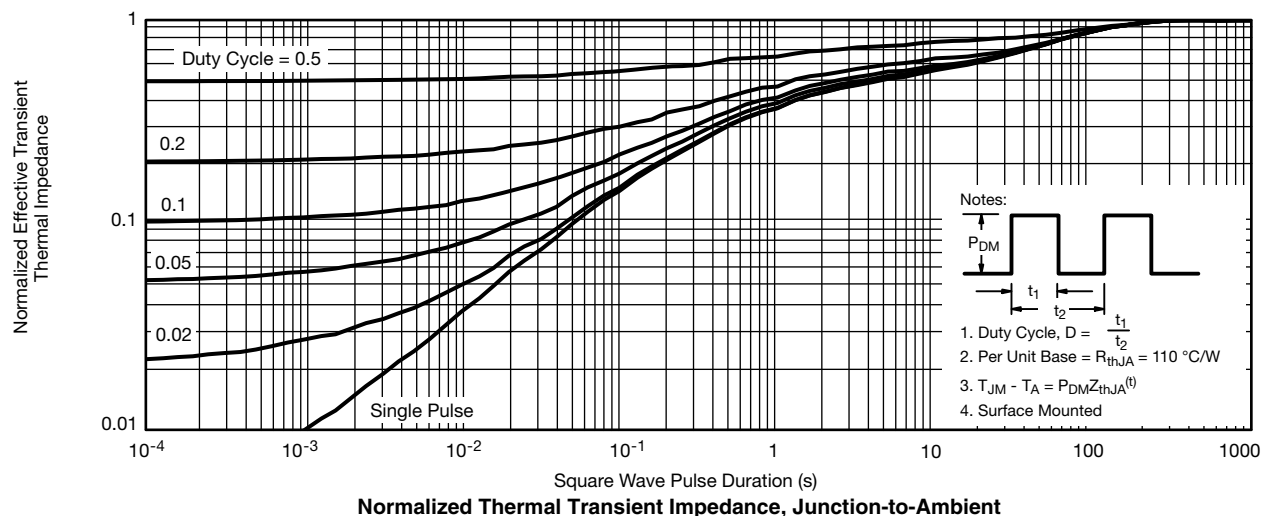
Si4909DY

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**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient****Safe Operating Area*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power, Junction-to-Foot

Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67077.

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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