

Does LTC4314 remain bus-friendly when...



Ed Mellinger 1 posts since Jun 28, 2018

Does LTC4314 remain bus-friendly when powered down? Jun 28, 2018 8:38 PM

I am evaluating the LTC4314 mux for a multi-master I2C system, where to save power (system runs on batteries for a year), I need to power down one of the masters, including its mux, when it is not in use. Other devices will continue to use the I2C bus while this mux is powered down.

My reading of the spec sheet ILEAK (Input Leakage Current) value is that all SDA and SCL pins are high impedance ($<10\mu\text{A}$) at all times, pretty much regardless of whether VCC and/or VCC2 are present or are zero. However there are no words in the Operation or Applications section that would give a warm fuzzy feeling that such a mixed-power situation is supported.

Can anyone comment on whether this is an approved mode of operation for this part, or offer any warnings of gotchas that might apply in this situation?

Additional info: VCC = VCC2 = I2C bus VDD = 5V when operating; bus speeds are $<10\text{kHz}$, and I do not anticipate using the Rise Time Accelerators. I just want to save microamps during the 98% of the time the system is idle.

Thanks!

Tags: ltc4314



jnaso 55 posts since Apr 21, 2016

Re: Does LTC4314 remain bus-friendly when powered down? Jun 30, 2018 10:50 AM

Hi eddykilowatt,

Your understanding is correct. The LTC4314 I2C bus pins will not interfere with the bus while the device is unpowered. The control pins are also high impedance, so if there happens to be a high signal on one of those pins, it won't parasitically power up the LTC4314.

One thing to note: If VCC=0V, the equivalent input resistance of the ACC(bar) pin is 125k to ground for ACC(bar) greater than 1.5V. So if VCC=0V and ACC(bar) is 5V, it will sink about $40\mu\text{A}$. It won't power up the LTC4314, but something to be aware of.

Hopefully that leaves you with that warm and fuzzy feeling you were looking for!

Regards,
Jason

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