Design Notes
Lower Half Elex Board, *Primary* Battery System, Coastal Profiling Float

2021-07-26 ECM adapt from HD Battery req'ts doc

1. Requirements

1.1. Manage 8S4P pack of Electrochem 3B0036 Li primary cells. Pack wired in two groups of two parallel strings each, independently fused at 8A, and brought out on four heavy wires.

1.2 Typical discharge profile is 10 min pumping at 8 A, 1 hr profiling at 0.3 A, and 1-23 hr sleeping at 0.004 A. Float system max current draw is TBD A. Wiring and fusing should support this load.

1.3 Expected pack operating voltage range is 31.4 V max (beginning of life, open circuit), 16 V min (end of life, full load, 0 degC). Expected capacity at 0 degC and 8 A load is approx 2.55 V/cell x 8 cells x 26 A-hr/string x 4 strings = 2100 W-hr. (C.f. Inspired Energy @ 28V x 3.2 A-hr x 6 sticks = 540 W-hr.)

1.4 LHE should provide pack overcurrent and undervoltage cutoff, CPU-controlled sleep function, endcap power switch support, discharge current coulomb counting, and power switching and overcurrent protection for the pump motor drive.

1.5 LHE overcurrent should shut down input from battery pack, after 15 msec at pack max rated current of 12 A (TBD)

1.6 LHE undervoltage should shut down input from battery pack, after ~100 msec at pack voltage of 16.0 (TBD) V falling. Undervoltage warning should be at 18.0 (TBD) V falling

1.7 LHE sleep function should switch the system outputs off for programmable periods from 1 to 64 minutes (+/- 5%). The sleep function should be armed and triggered over the I2C connection to the Mobo/Micro. Standby power in the sleep state should be less than 2.5 mW (100 uA at 25 V).

1.8 LHE should accept input from two endcap momentary contact reed switches and should switch system outputs on or off respectively. Standby power in the off state should be less than 2.5 mW.

1.9 LHE should integrate battery current with TBD time resolution, TBD coulomb resolution, and TBD coulomb full-scale capacity. Coulomb counter contents and controls should be accessible over the I2C connection to the Mobo/Micro

1.10 LHE interface to Mobo/Micro should present I2C on two signal lines at 100 kbit/s, 24 V battery power output at TBD A max, and should receive I2C 5 V logic power input at 100 mA max (for Mobo-related interface circuits in the battery pack). The I2C signals should be buffered by and NXP PCA9512 Buffer device.

1.11 LHE should include power switching, fault reporting, and energy monitoring for the Pump Drive power output. The power, fault, and monitor functions should be controlled over the I2C connection to the Mobo/Micro. The Pump Drive power switch should include soft start inrush control with a current limit of 10A and be able to charge 1000 uF of downstream capacitance. The Pump Drive power switch should include Electronic Circuit Breaker function with a trip rating of 10A and trip time of 15 msec. The Pump Drive power feed should use a large TVS diode(s) for pump regen control. An active regen control circuit is not required. The Pump Drive power feed should include an energy monitor circuit. The energy data should be accessible to the Mobo/Micro over the I2C bus.

1.12 LHE available board area is ~8.6" x ~2.2" with ~6 standoff screw mounting holes. Vertical clearance is TBD.

2. Description

2.1 Input overcurrent and undervoltage: An LTC4380 is present to provide power switching for the Sleep and Endcap Power functions. Its overcurrent function is used to protect the battery pack from downstream shorts or overcurrent demands. An LTC2934 supervisor monitors pack discharge voltage via divider network, and generates an Undervoltage Warning which can be read via the PIO interface by the Mobo/Micro, followed by Undervoltage Shutdown at a lower voltage, which disables the On input to the 4380. The auxilliary n_MR input to the supervisor allows the PwrOn signal from the sleep timer to control the power switch as well.

2.2 Sleep Timer and On/Off Control: Flip-Flop 741G74 is the manual power control for the Float. It is set or reset by momentary closure of the endcap Pwr_On and Pwr_off reed switches, respectively, and its output becomes the PwrOn enable signal to the input power switch.

The sleep timer is an MC14536 oscillator/timer set for 2.185 kHz, with inputs ABC that can be configured for delays from 1 to 64 minutes. The sleep time is set by Mobo PIO outputs SleepTime0-2, which are clocked into a 74HC174 latch by raising Mobo PIO signal SleepTrig high.

During normal (non-sleep) float operation, SleepTime0-2 is held to 000, which when latched is applied to AND gate 741G27 to produce the SleepDis signal. SleepDis resets the sleep timer, stops its oscillator, and forces its output high, which allows AND gate 741G00 to be controlled by the reedswitch power flip-flop to set MasterPwrOn to either the on or off state.

Sleep is enabled by writing a non-zero value to SleepTime0-2, and triggered by raising

SleepTrig high to latch the value into the 74HC174. The SleepTime value n is applied to the timer's ABC inputs, selecting decoder stages corresponding to delays of 2^(n-1) minutes at the timer output. At the same time, the non-zero value applied to the 741G27 gate allows SleepDis to go low and the timer to begin counting.

The timer output goes low after one timer clock cycle (~0.5 msec), which forces the AND gate to
override the manual power flip-flop and set MasterPwrOn to the off state. The timer output remains low for the commanded sleep time and then goes high, gating MasterPwrOn back to the on state and waking up the Mobo and rest of the float.

The sleep cycle will repeat after another 2^(n-1) minutes, so upon awaking from sleep the Mobo controller should write 000 to SleepTime0-2, and latch it by cycling SleepTrig high and then low. (This should be part of normal power-on initialization as well.)

After initialization the SleepTime and SleepTrig port bits can be re-configured as inputs, for some additional insurance against inadvertent writes, as they are held in inactive states by pulldowns.

The Float can be powered on or off from any state, asleep or awake, via the endcap reed switches. If the Float is in sleep mode, the endcap Pwr_On reed switch will set the power control flip-flop and also reset the SleepTime latch to 000, setting SleepDis, disabling the sleep timer, and gating MasterPwrOn to the the on state.

2.3 Coulomb Counter: An LTC2946 Energy Monitor in the input section 'borrows' the current-sense signal used by the input overcurrent circuit. The monitor's Charge accumulator provides a 32-bit reading of current demand over time. The monitor is powered from the always-on Batt5V bus in order to retain accumulator data throughout a deployment; it should be placed in its Shutdown Mode before the Float is put to sleep or powered down, in order to reduce current demand to quiescent values.

2.4 Mobo PIO Port: The Mobo controls the LHE board via two TCA6408 8-bit I2C/PIO ports. The ports can be bitwise configured as either inputs or outputs. The first port, I2C address 0x21, is largely an output port, and generates the pump power and sleep trigger signals. The second port, I2C address 0x20, has the Undervoltage Warn and pump power fault (circuit breaker tripped) inputs. The second port also has the sleep timer control bit outputs SleepTime0-2.

2.5 Power Supplies: The LHE board generates the always-on 5V logic supply Batt5V from the pack input, via a TPS7A16 LDO regulator. An additional 5V logic supply Mobo5V is derived from the 5 V logic power provided by the Mobo interface when the Mobo is on. Batt5V powers the sleep timer and coulomb counter, while Mobo5V is used for the Mobo-facing portions of the PIO port and I2C interface.

3. Design Notes

3.1 Undervoltage Supervisor Desired trip voltages are 18V UV Warn, 16V UV Shutdown (2.0 V/cell). Allow 10 uA for divider to keep impedances low, 16V/10uA = 1.6 Mohm total divider impedance. (Supervisor input current 1 nA so no worreis.) PFI (warn) threshold is 0.400 V, bottom R value is 0.4V/18V x 1.6M = 35.5k use 35.7k. ADJ (shutdown) threshold is 0.400, R value is, 0.4/16V x 1.6M = 40.0k, subtract bottom R to get middle R: 40.0 - 35.7 = 4.30k, use 4.32k. Top R should be 1.6M - 35.5k - 4.32k = 1.56M use 1.58M to wind up a bit low.

3.2 Power Switch Current limit threshold 50 mV. 12.5A limit needs 4mohm... non-stock. Use 7.5 and 9 mohm in parallel for 4.1mohm and 12.2 A limit? 12 A x 15 msec x 30V is right at SOA limit for PSMN1R7-60BS pass FET.

3.3 Pack Coulomb Counter Full scale Vsense input 102.4 mV, LSB is 25 uV. With 4 mohm shunt, full scale is 25.6 A and LSB is 6.25 mA. Set CLK_DIV divider to 4 (default) to divide 4 MHz clock to target 250 kHz for A/D, 16.4 msec conversion/accumulate time, 2.23 year time counter overflow.

Charge accumulator is 36 bits with top 32 bits read back, so 16 actual counts for 1 LSB read back. So 1 LSB = 6.25mA x 16 x 16.4msec/LSB = 1.64 mC/LSB charge resolution. 1.64mC x 2**32 = 7.04 E6 C (A-sec). 7.04 E6 C / 3600 sec/hr = 1957 A-hr full scale capacity. (C.f. 104 A-hr pack size.)

3.4 Sleep Timer

3.5 Pump CB/Inrush/Load Switch

3.6 Pump Energy Monitor

3.7 Overcurrent Coordination

3.8 Power Supplies Batt5V loads are

Timer MC14536 dynamic	6 uA
Reed switch pullups	1000
Energy monitor 4 MHz 2@950uA	1900

3.X Standby Power Budget: Focus on sleep/shutdown power since Float power should dominate when power is on. 4 strings x 26 A-hr/string = 104 A-hr for pack. Allow 1% for sleep, gives 1.04 A-hr. 1 A-hr / 24 hr / 365 d = 114 uA sleep budget.

UV divider	10 uA
LTC4380 shutdown	8

TPS7A16 LDO	10
MC14536 dynamic	6
TCA6408 ports, static, 2 @ 7uA	14

Questions/Comments for Review

1. ~~Reed/Sleep interaction logic looks backwards, Reed_On can't override Sleep -- reverse reed labelling and use n_Q output?~~
2. Pack overcurrent is latch-off. OK? (Retry available but req. different 4380 chip)
3. Need: Final numbers for Float 5V and 12V loads, and/or Mobo max VBatt current draw.
4. Need: LHE and DC-DC board vertical clearance dimension(s).
5. Ed check sequencing of PIO power and need for Joint4V7 power rail.
6. Energy Monitors on Batt pwr (requires shutdown) or Mobo pwr (requires saving data)?
7. UV Warning to Mobo interrupt (as was planned for Alert signal)?

Questions for Electrochem/BattSpecialties

What is 3B0036 internal fuse?
Recc fuse to coordinate (blow first) for 2 parallel strings
Suggested UV Cutoff for 8 series 3B0036

Programming Notes

1. Batt pack energy monitor (LTC2946) must be put into shutdown mode (40uA) before float is put to sleep or turned off; when active it draws ~1 mA.