

STM32H7B3I-EVAL

MB1331

Table of contents

Sheet 1 : Project overview
Sheet 2 : MB1331 TOP page
Sheet 3 : MCU STM32H7B3LIH6Q
Sheet 4 : MCU Clocks & Reset
Sheet 5 : USB_OTG_FS
Sheet 6 : USB OTG HS with external PHY
Sheet 7 : Memories (NOR, SRAM, SDRAM)
Sheet 8 : OCSPI 1 & 2
Sheet 9 : SD Card 1 & 2
Sheet 10 : Audio Codec
Sheet 11 : Audio & Motor DFSDM
Sheet 12 : Camera
Sheet 13 : LCD
Sheet 14 : Peripherals (WIFI, buttons, LEDs)
Sheet 15 : FDCAN & RS232
Sheet 16 : STMP52 & PT100
Sheet 17 : Motor Control
Sheet 18 : MFX I/O Expander
Sheet 19 : Extension Connectors
Sheet 20 : Board Power
Sheet 21 : MCU Power
Sheet 22 : JTAG & Trace
Sheet 23 : ST-LINK V3 SWD

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the board layout.

Open Platform License Agreement

The Open Platform License Agreement (“Agreement”) is a binding legal contract between you (“You”) and STMicroelectronics International N.V. (“ST”), a company incorporated under the laws of the Netherlands acting for the purpose of this Agreement through its Swiss branch 39, Chemin du Champ des Filles, 1228 Plan-les-Ouates, Geneva, Switzerland.

By using the enclosed reference designs, schematics, PC board layouts, and documentation, in hardcopy or CAD tool file format (collectively, the “Reference Material”), You are agreeing to be bound by the terms and conditions of this Agreement. Do not use the Reference Material until You have read and agreed to this Agreement terms and conditions. The use of the Reference Material automatically implies the acceptance of the Agreement terms and conditions.

The complete Open Platform License Agreement can be found on www.st.com/opla.

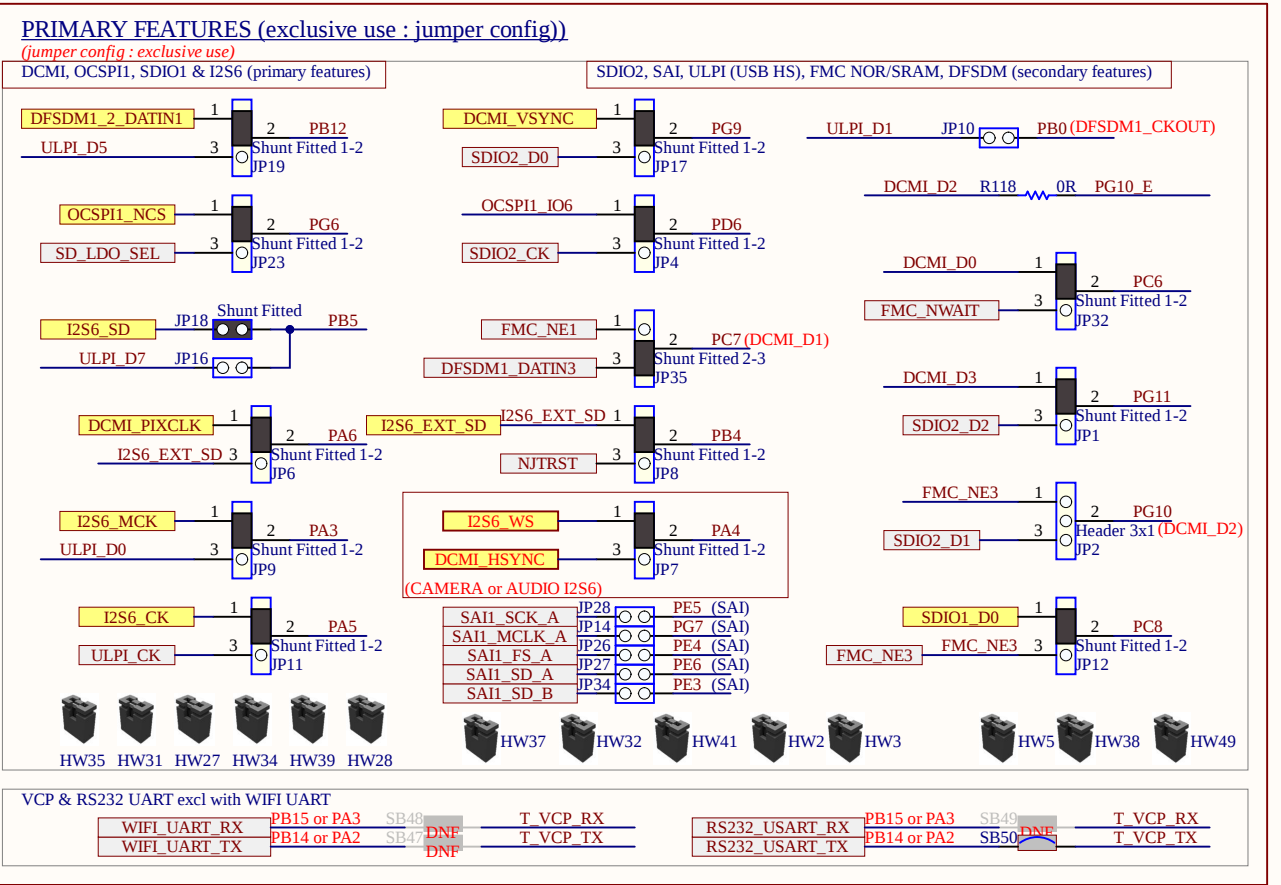
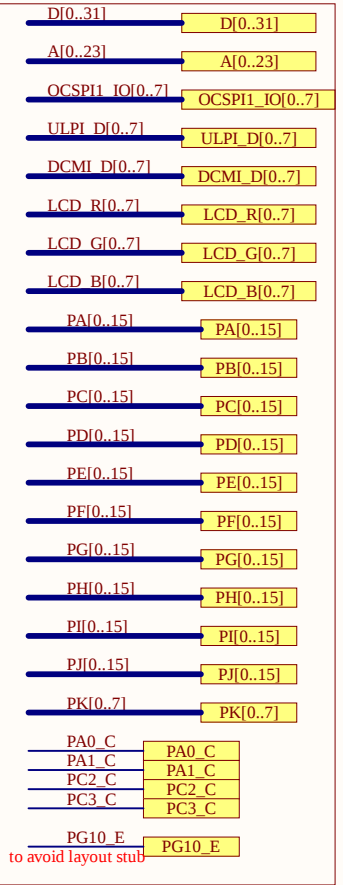
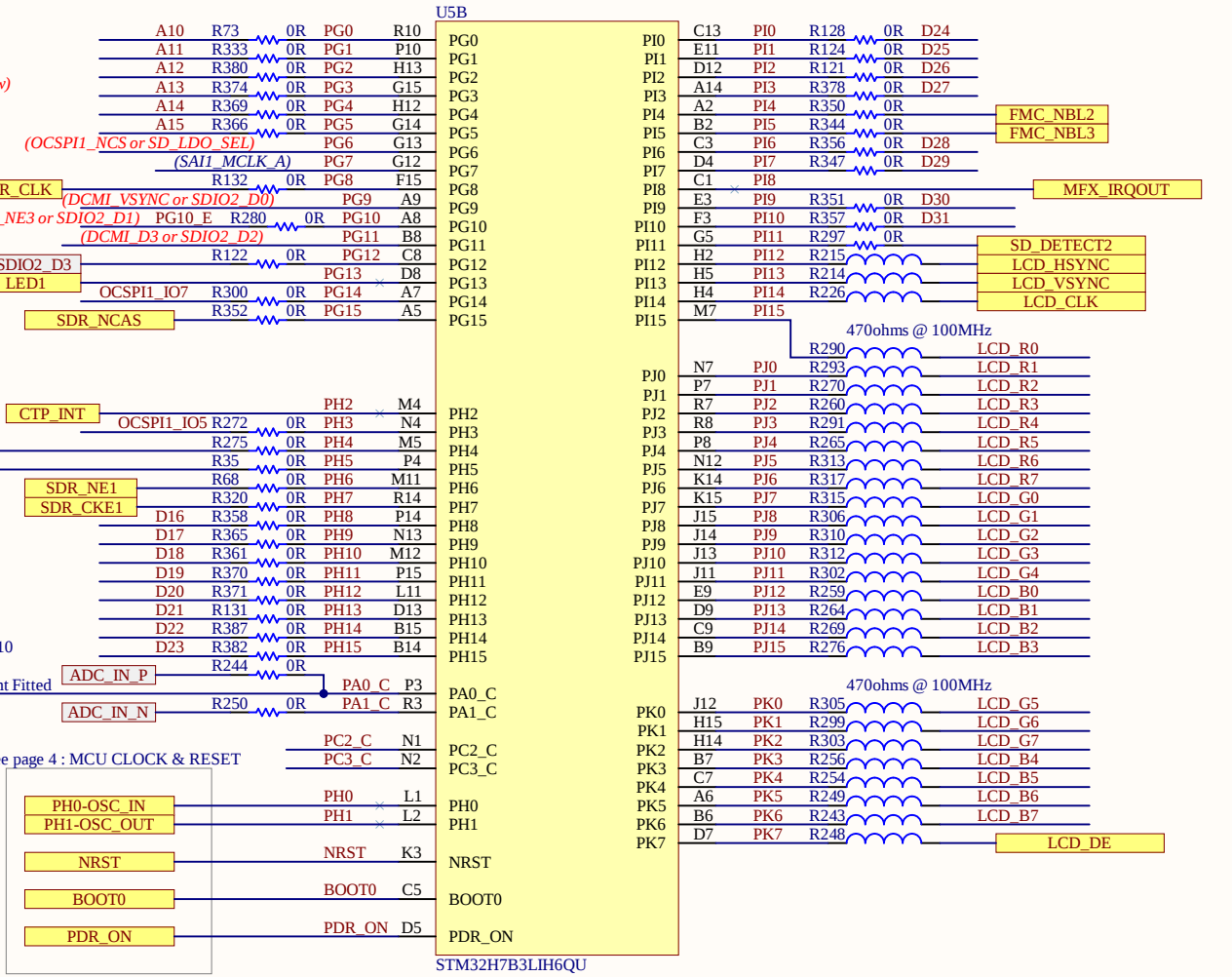
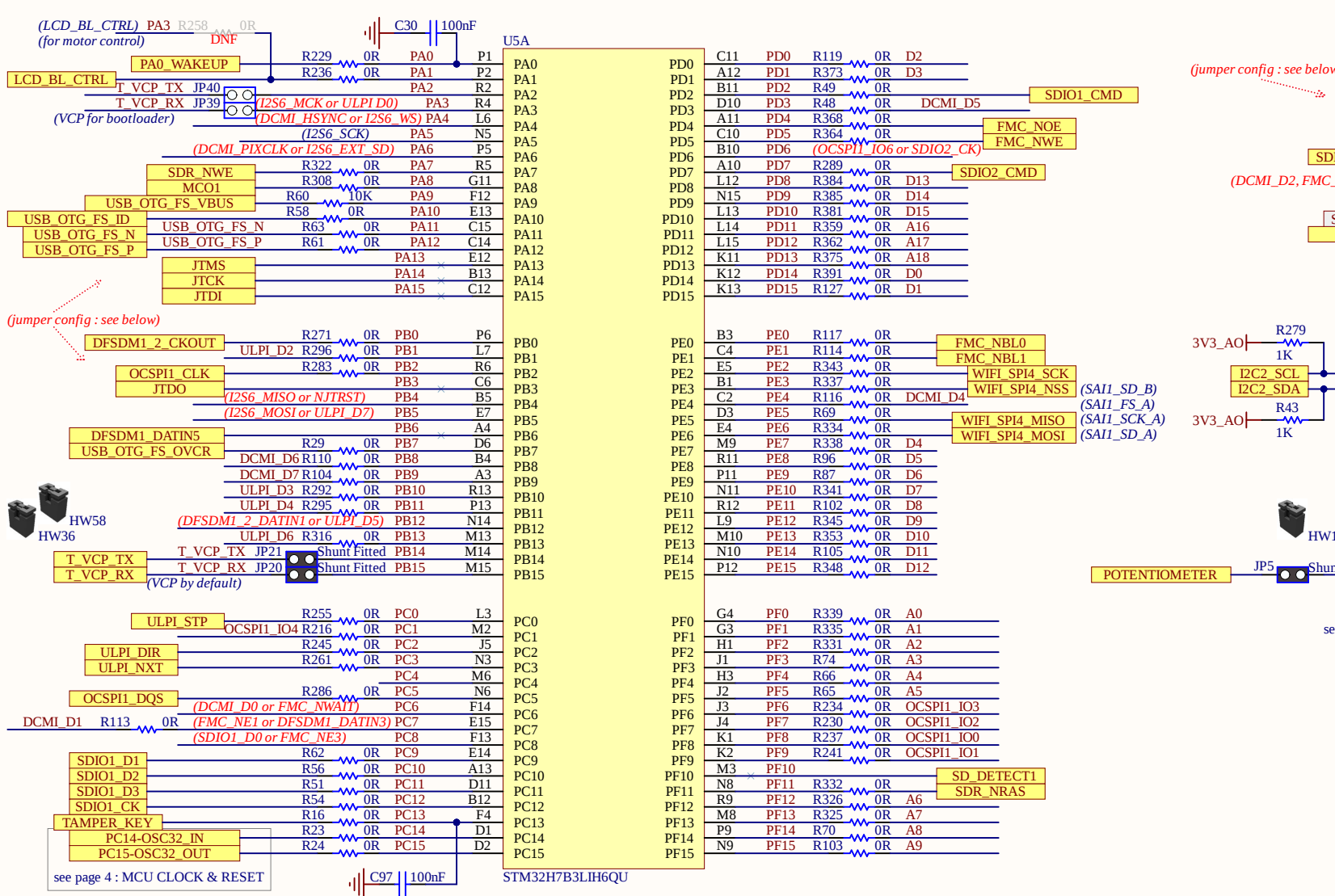
U_Top
MB1331_TOP.SchDoc

Title: Project overview		
Project: STM32H7B3I-EVAL		
Variant: H7B3LIQ		
Revision: D-03	Reference: MB1331	
Size: A4	Date: 25-MAR-20	Sheet: 1 of 23

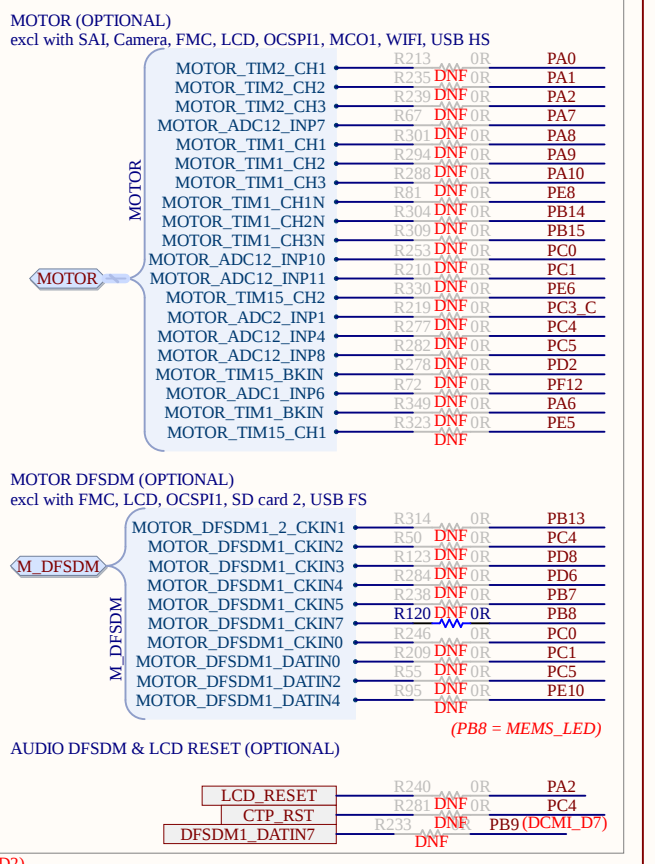
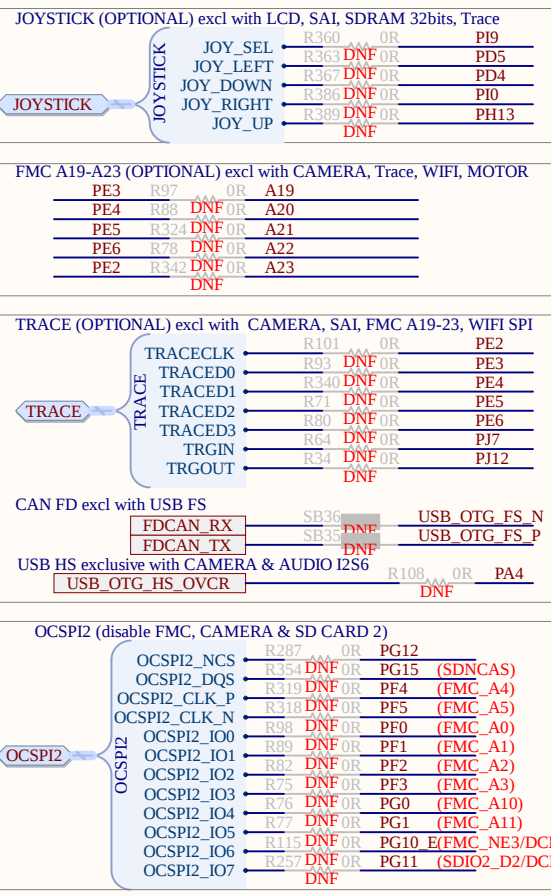


STM32H7B3LIH6Q MCU I/Os

PRIMARY FEATURES (fitted by default)

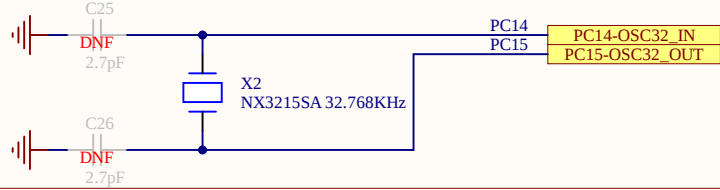


SECONDARY FEATURES (not fitted by default)

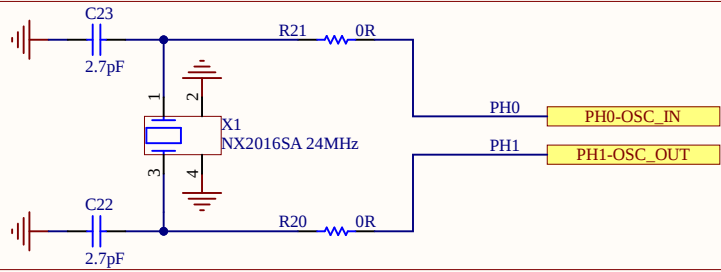


STM32H7B3LIH6Q MCU CLOCK, RESET & BOOT

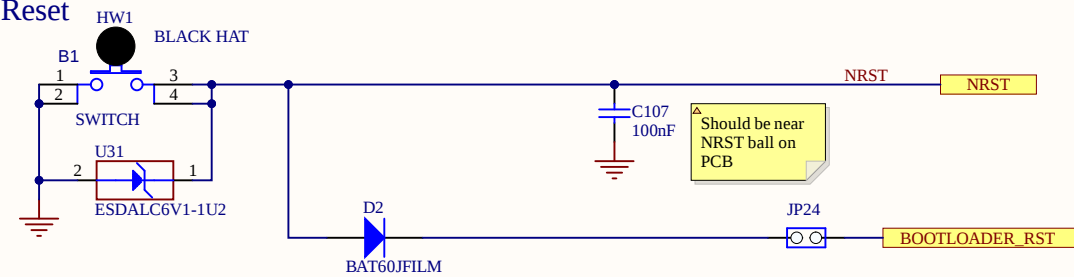
32kHz Clock



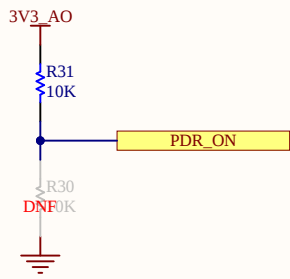
24MHz Clock



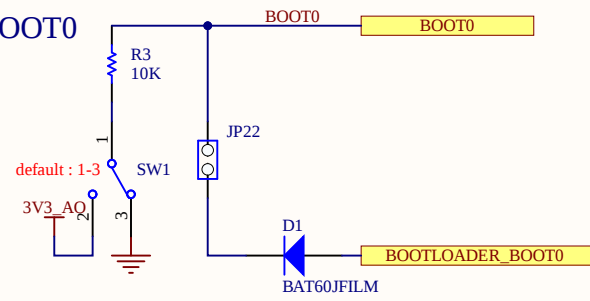
Reset



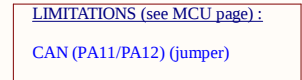
PDR ON



BOOT0



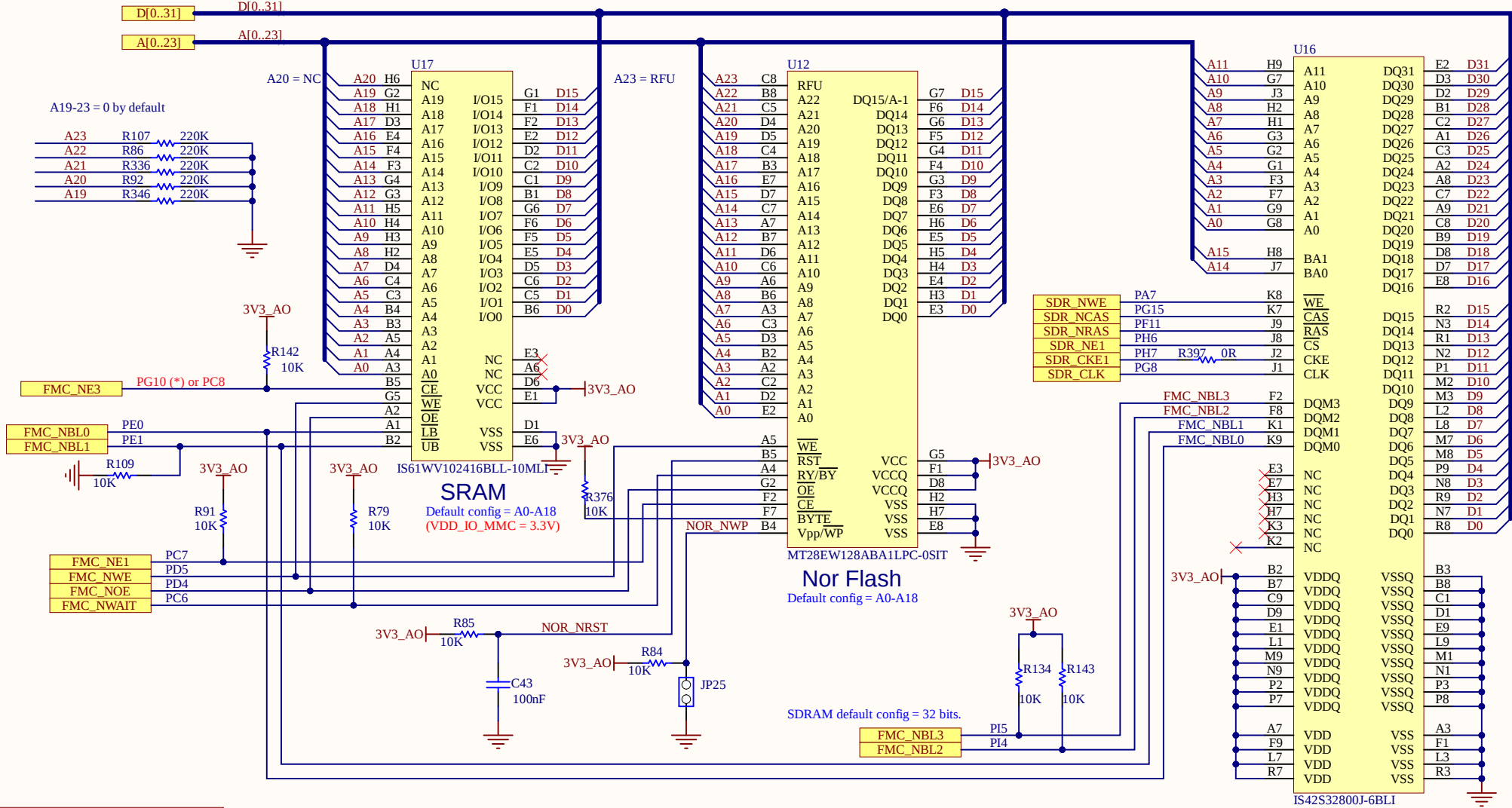
(Always $\overline{ON}$)



MEMORIES

(Always ON)

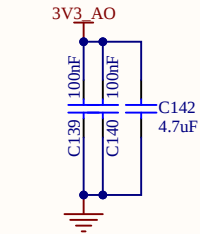
(*) Some SRAM I/Os are supplied by VDD_IO_MMC
(make sure to control MFX0 & PG6)
(see Power_Board page)



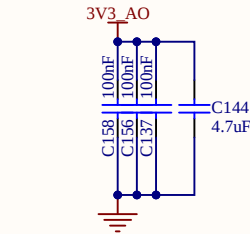
LIMITATIONS (SDRAM):
OCSPi2

LIMITATIONS (NOR):
CAMERA
OCSPi2, DFSDM DATIN3

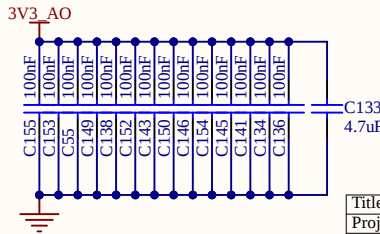
LIMITATIONS & BACK-UP (SRAM):
CAMERA
SD CARD : NE3 = PG10 (if SD CARD 1 is used) / PC8 (if SD CARD 2 is used)
OCSPi2
(*) Make sure to set VDD_IO_MMC = 3.3V



Place close to SRAM



Place close to Nor Flash



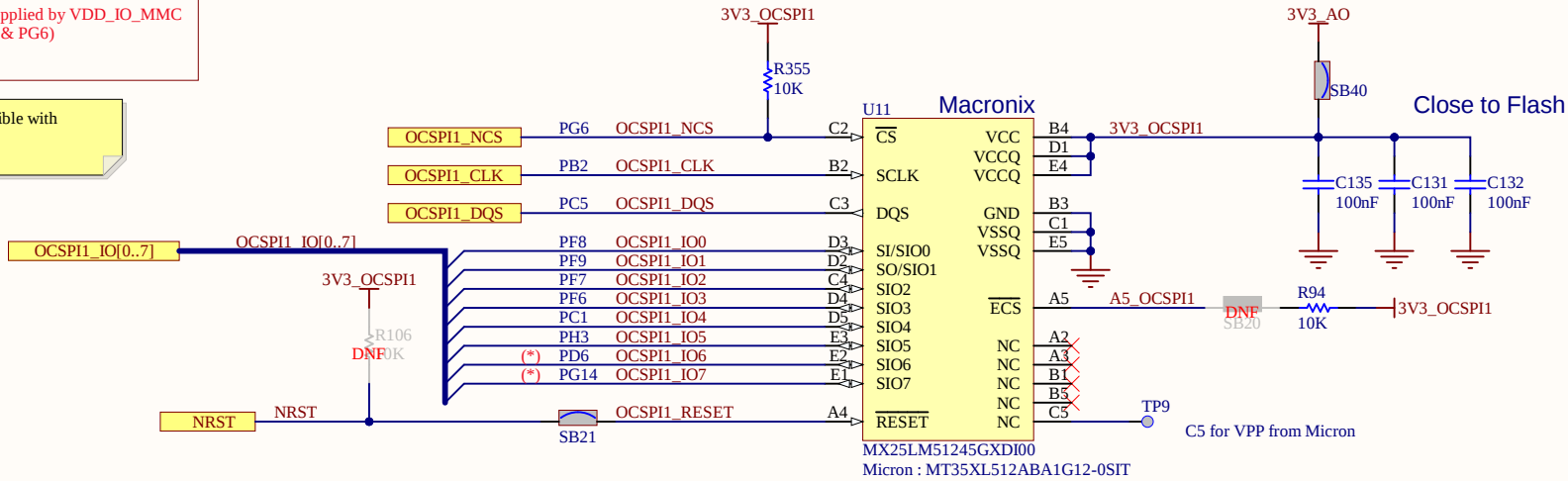
Place close to SDRAM



OCSPI 1

(*) Some OCSPI1 I/Os are supplied by VDD_IO_MMC
(make sure to control MFX0 & PG6)
(see Power_Board page)

Double footprint to be compatible with
Macronix and Micron
MT35XL512ABA1G12-0SIT

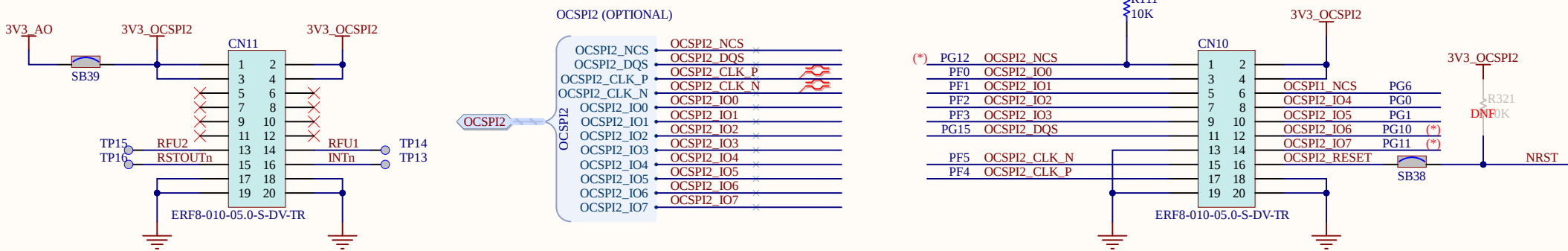


LIMITATIONS (see MCU page):
SD CARD 2 (jumper)
(*) Make sure to set VDD_IO_MMC = 3.3V

(RESET pins of Flash have internal pull-up (both) by default
and VPP connection is tbc on Micron)

OCSPI 2 (MB1242 Module connector)

(*) Some OCSPI2 I/Os are supplied by VDD_IO_MMC
(make sure to control MFX0 & PG6)
(see Power_Board page)

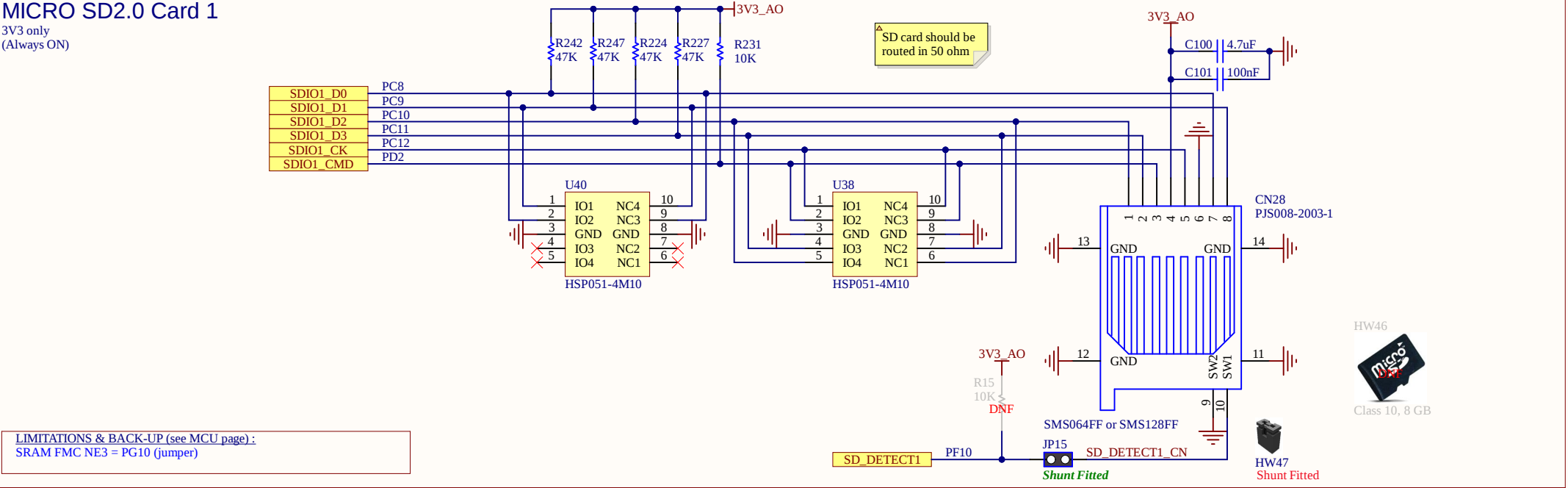


LIMITATIONS & BACK-UP (see MCU page):
FMC (NOR, SRAM & SDRAM)
SD CARD 2 (jumper)
(*) Make sure to set VDD_IO_MMC = 3.3V



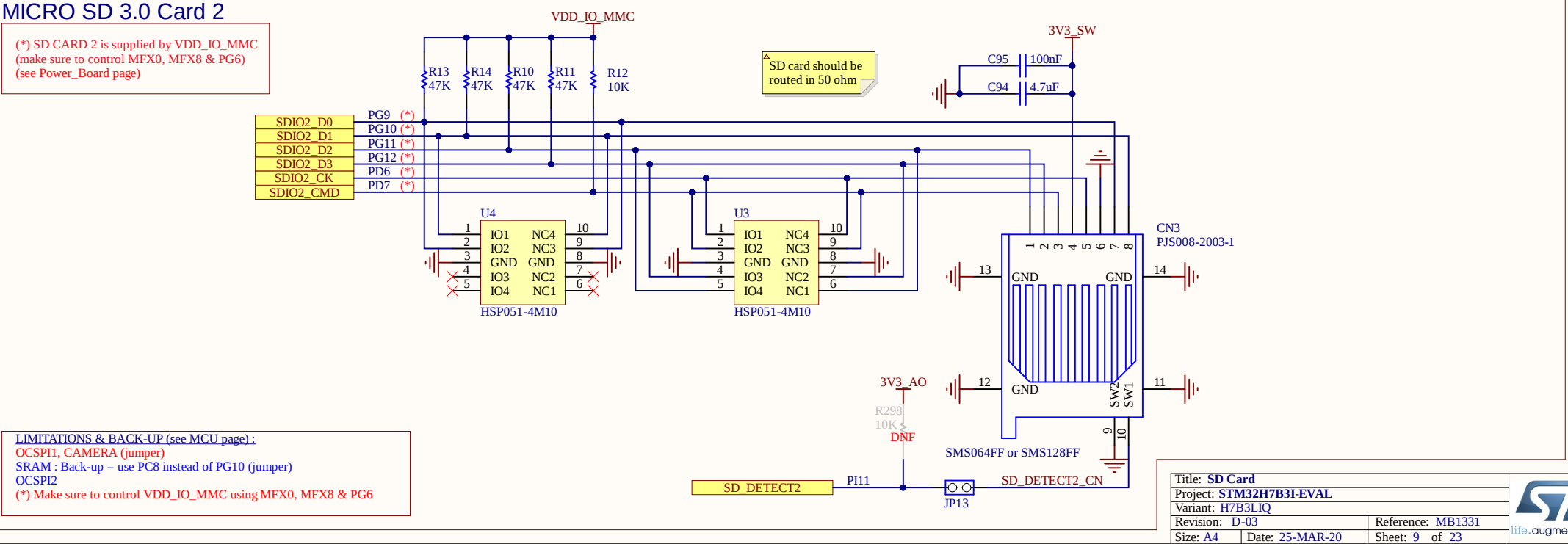
MICRO SD2.0 Card 1

3V3 only
(Always ON)



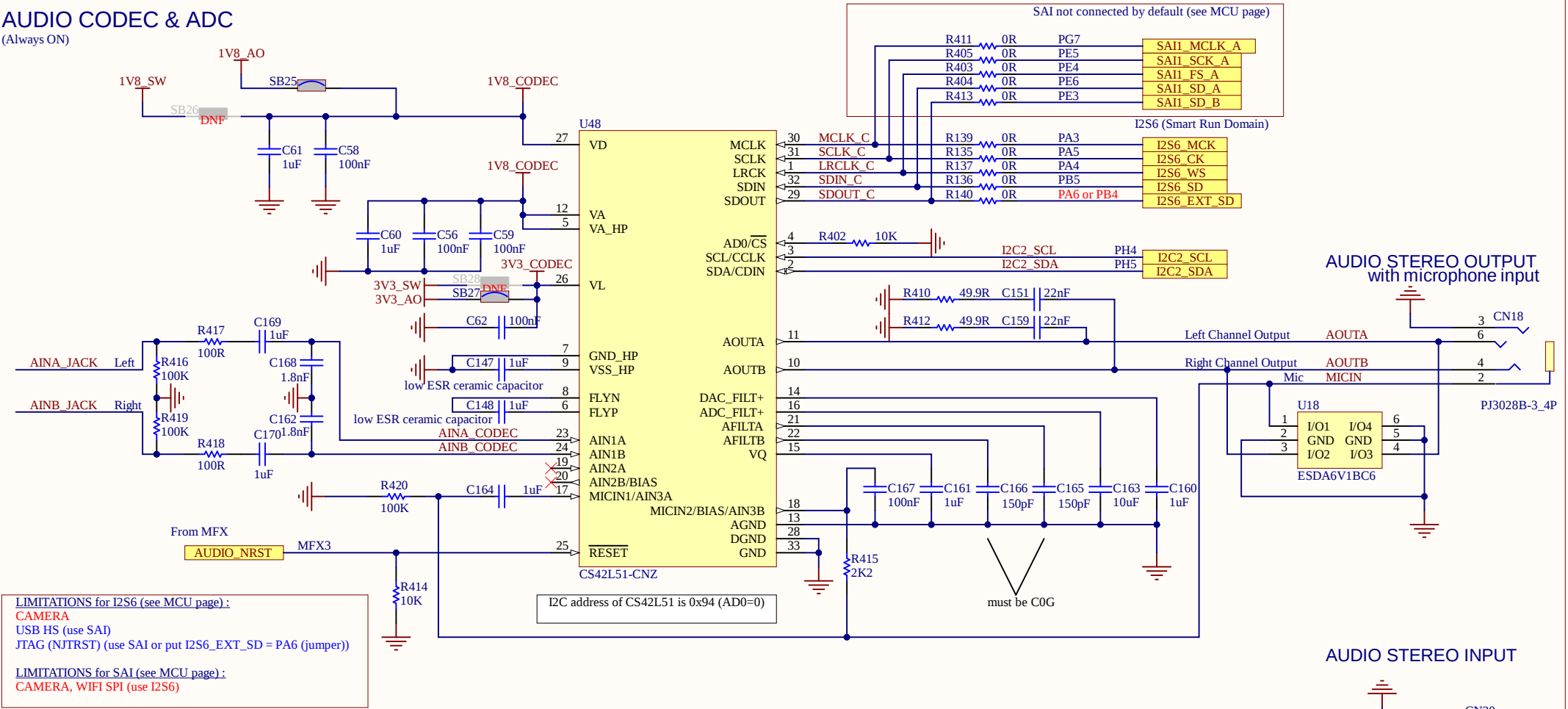
MICRO SD 3.0 Card 2

(*) SD CARD 2 is supplied by VDD_IO_MMC
(make sure to control MFX0, MFX8 & PG6)
(see Power_Board page)



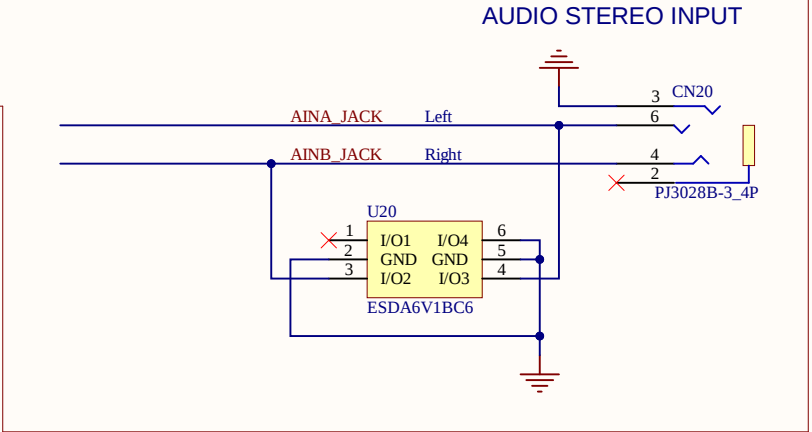
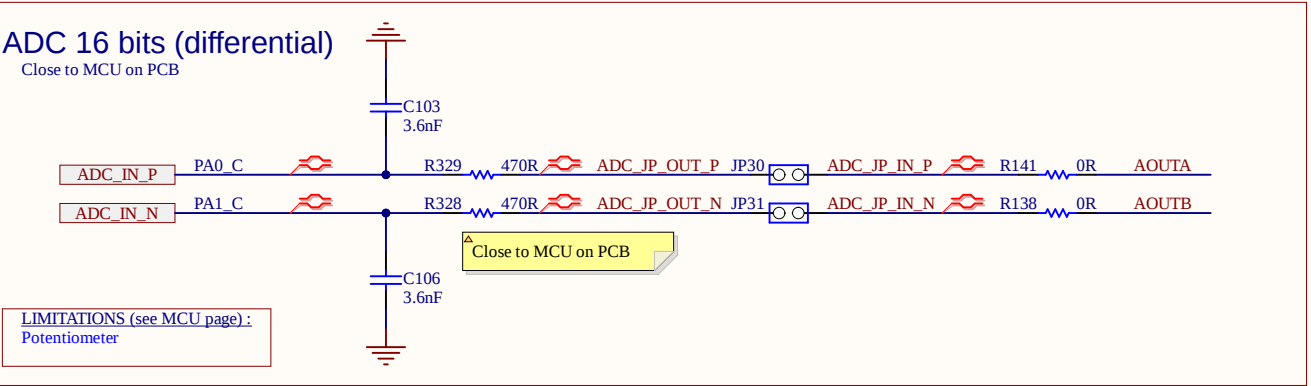
AUDIO CODEC & ADC

(Always ON)



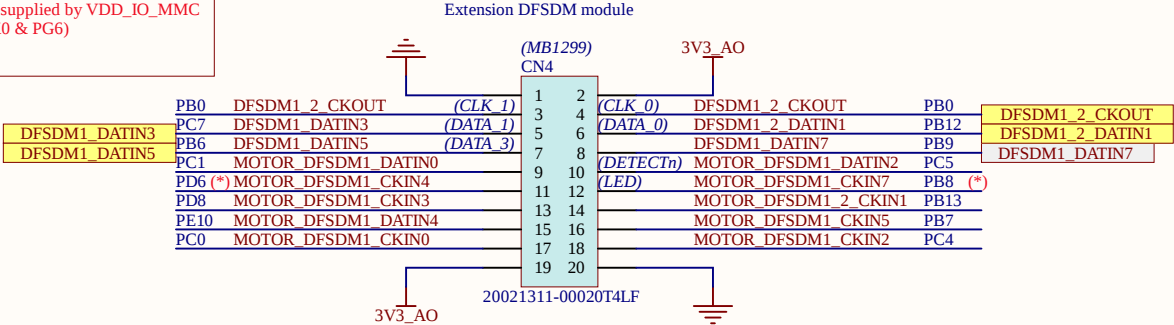
ADC 16 bits (differential)

Close to MCU on PCB

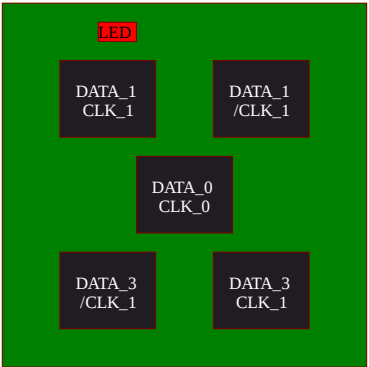


DFSDM AUDIO & MOTOR

(*) Some DFSDM I/Os are supplied by VDD_IO_MMC
(make sure to control MFX0 & PG6)
(see Power_Board page)



HW30
DNF
MB1299-5_MEMS_Microphone_Expansion_Board



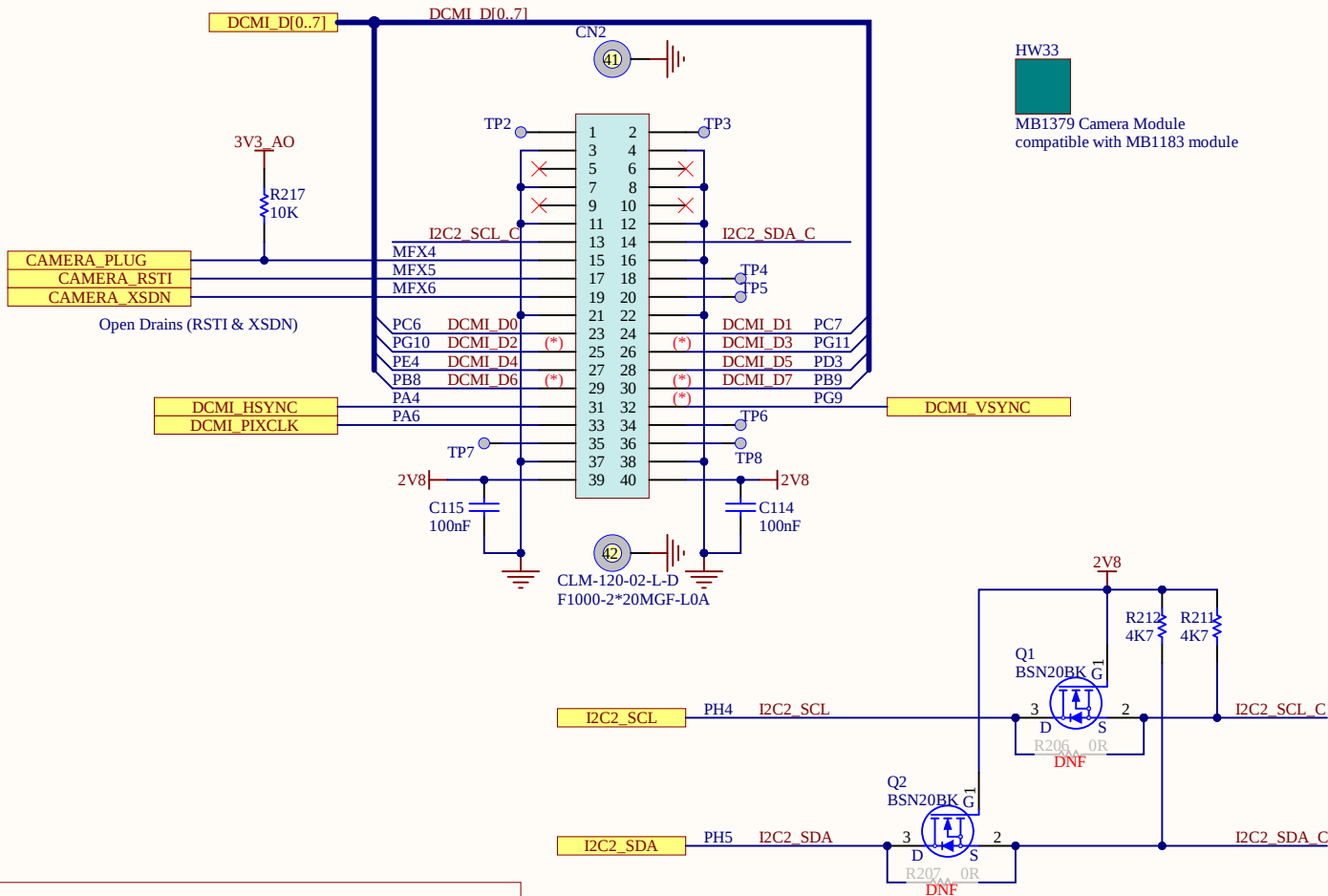
(MB1299)
CLK0 & CLK1 = data valid when clk is high
/CLK1 = data valid when clk is low

LIMITATIONS AUDIO DFSDMx4 (see MCU page):

(*) Make sure to set VDD_IO_MMC = 3.3V
CAMERA
USB HS, FMC NOR (jumper)

CAMERA MODULE CONNECTOR

(*) Some DCM1 I/O are supplied by VDD_IO_MMC
(make sure to control MFX0 & PG6)
(see Power_Board page)

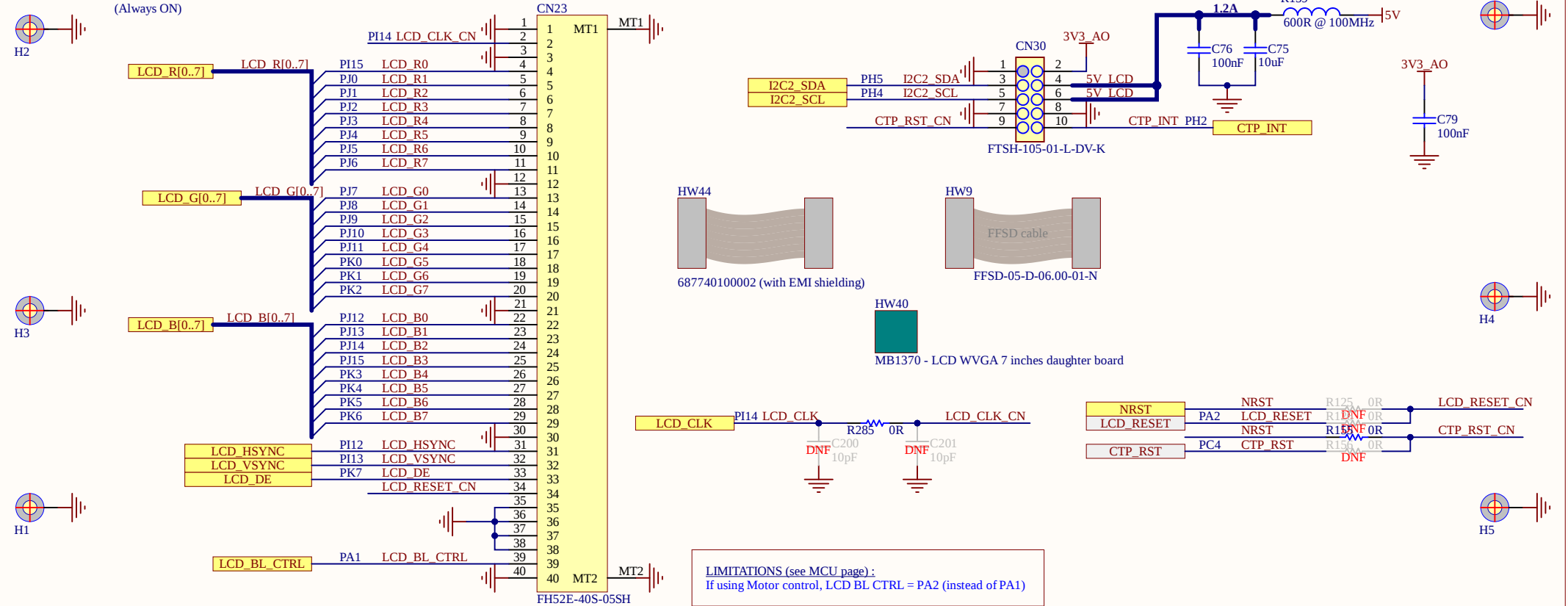


HW33
MB1379 Camera Module
compatible with MB1183 module

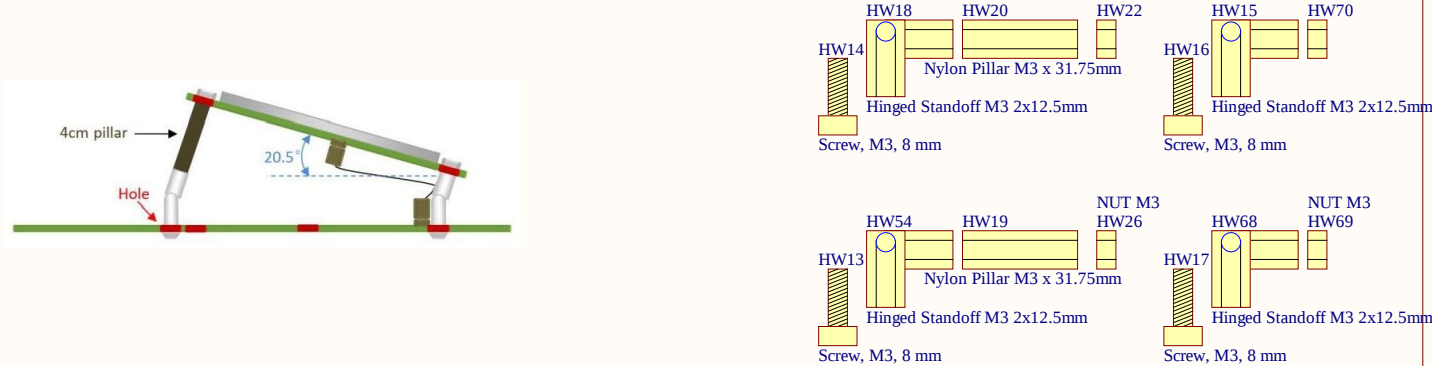
LIMITATIONS (see MCU page) :
AUDIO (I2S6), DFSDM
AUDIO (SAI), SRAM, NOR, SD CARD 2, OCSPI2
(*) Make sure to set VDD_IO_MMC = 3.3V



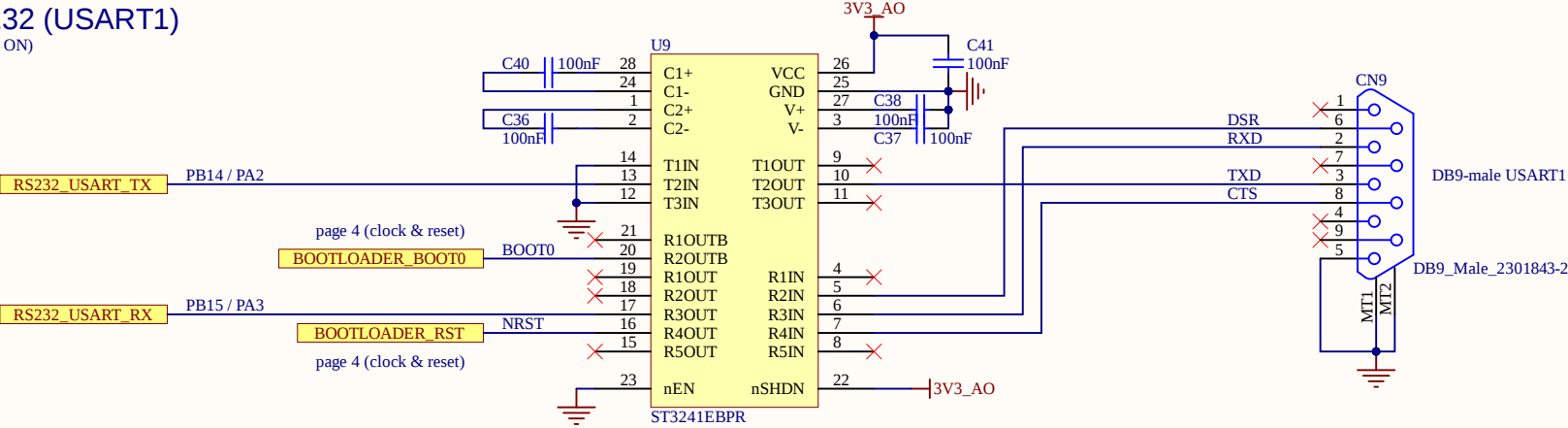
RGB LCD MODULE CONNECTORS



LCD MODULE MECHANICAL ASSEMBLY



RS232 (USART1)
(Always ON)

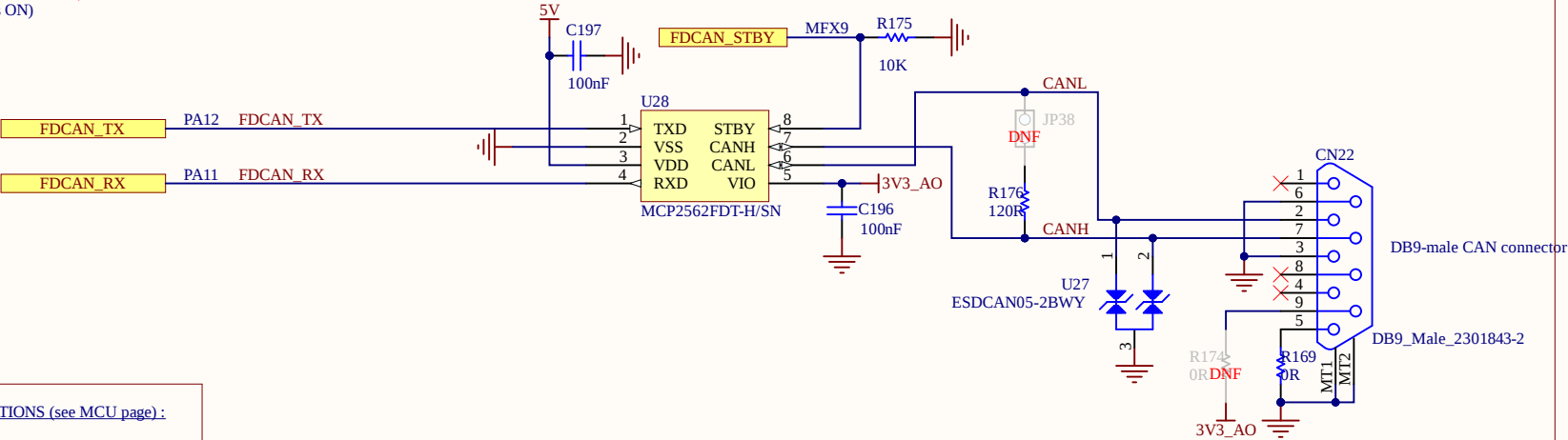


LIMITATIONS (see MCU page) :

PB14/PB15 : not a bootloader compatible UART

PA2/PA3 : AUDIO I2S6, USB HS, MOTOR CONTROL

CAN FD
(optional ; not fitted)
(Always ON)



LIMITATIONS (see MCU page) :

USB FS

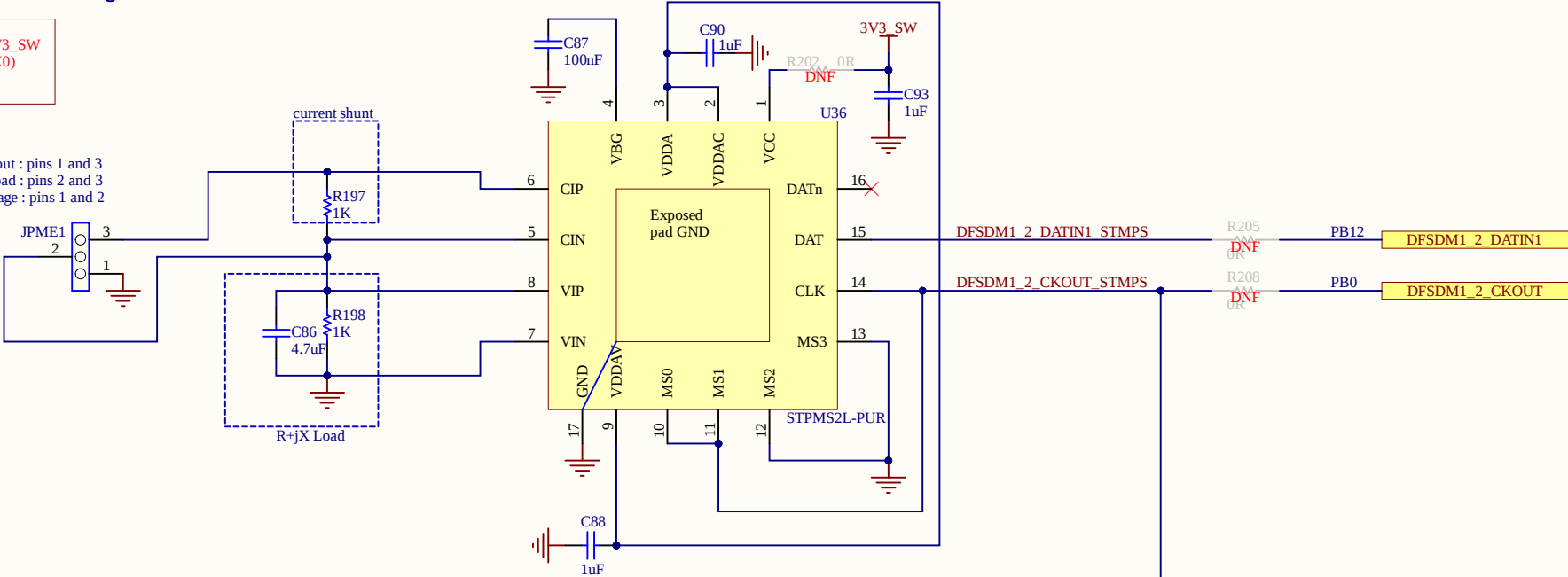


STPMS2 power metering

(optional : not fitted)

STPMS2 is supplied by 3V3_SW
(make sure to control MFX0)
(see Power_Board page)

external generator input : pins 1 and 3
voltage of complex load : pins 2 and 3
shunt voltage : pins 1 and 2



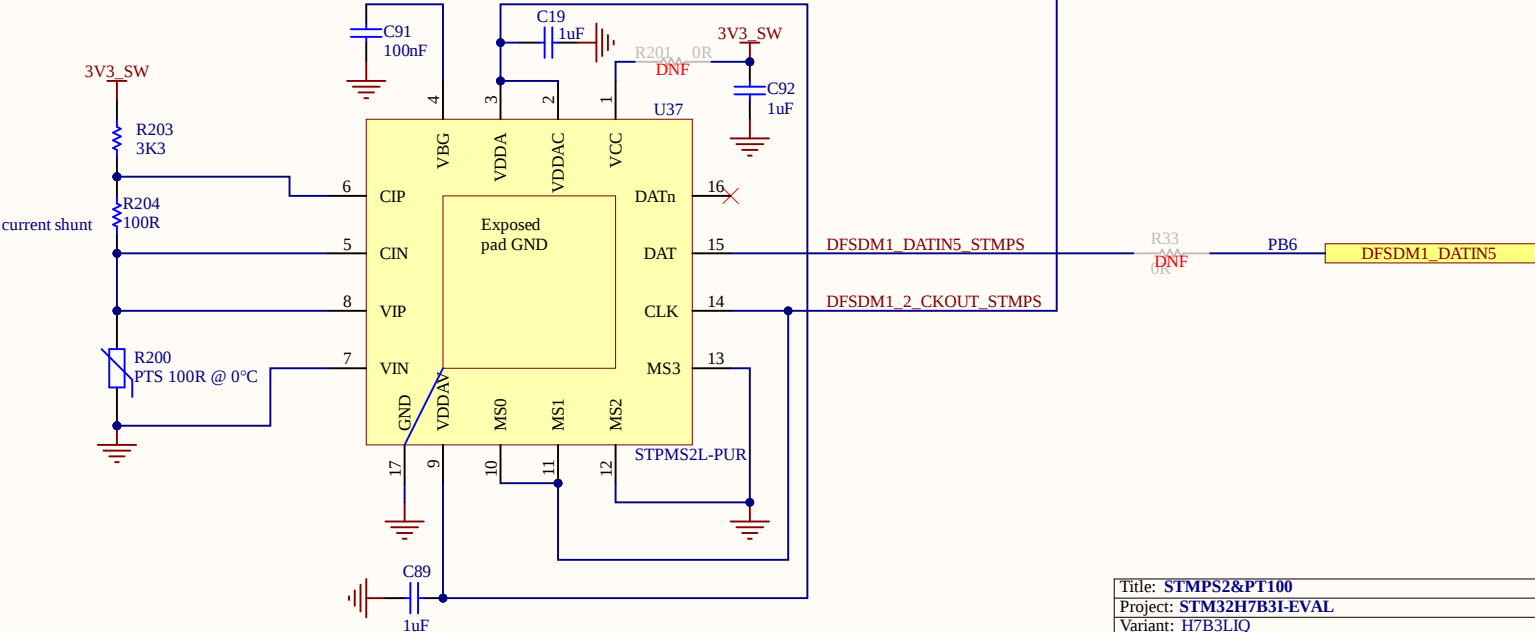
LIMITATIONS :

See user manual

PT100 measurement using SigmaDelta STPMS2

(optional : not fitted)

STPMS2 is supplied by 3V3_SW
(make sure to control MFX0)
(see Power_Board page)



LIMITATIONS :

See user manual

Title: STPMS2&PT100		
Project: STM32H7B3I-EVAL		
Variant: H7B3LIQ		
Revision: D-03	Reference: MB1331	
Size: A4	Date: 25-MAR-20	Sheet: 16 of 23



MOTOR CONTROL
(optional : not fitted)

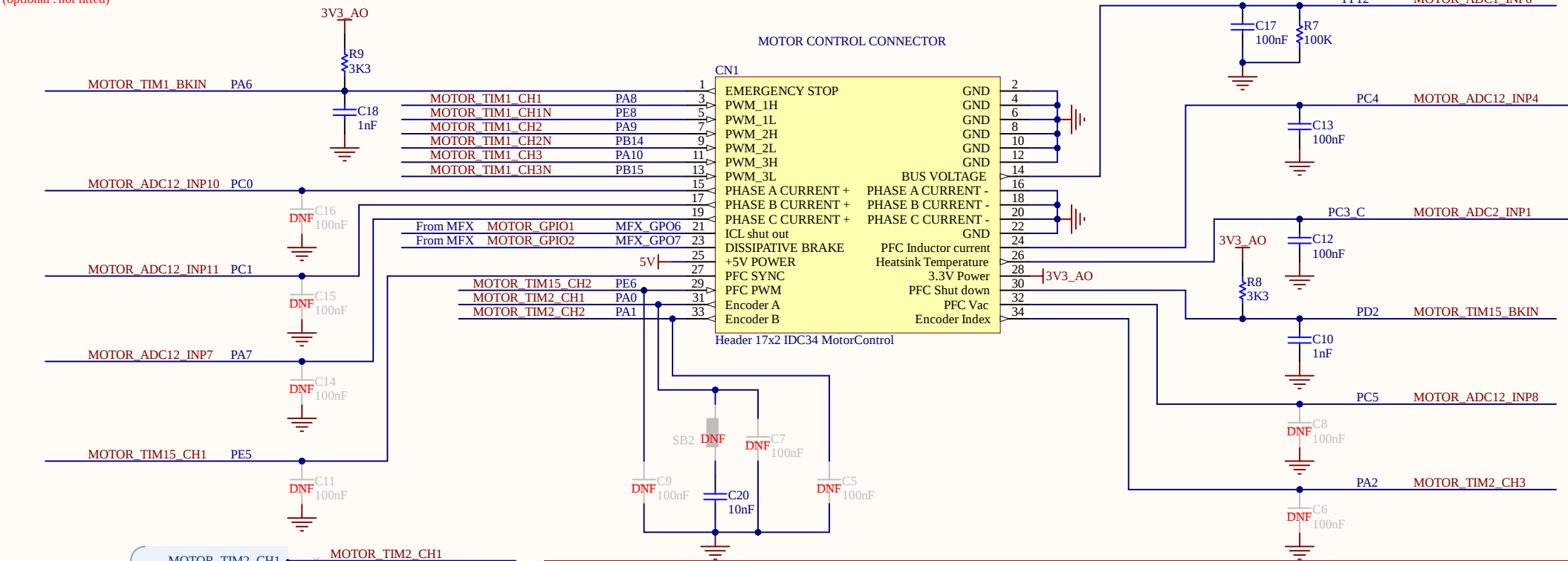
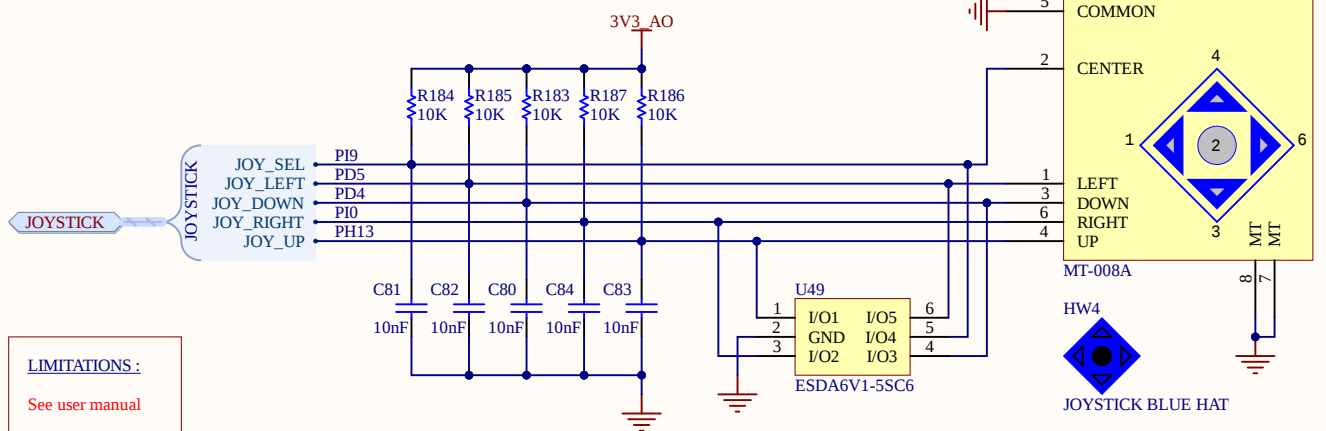


Table mapping motor control signals to specific pins and components. Includes columns for MOTOR, MOTOR_TIM, MOTOR_ADC, and MOTOR_GPIO.

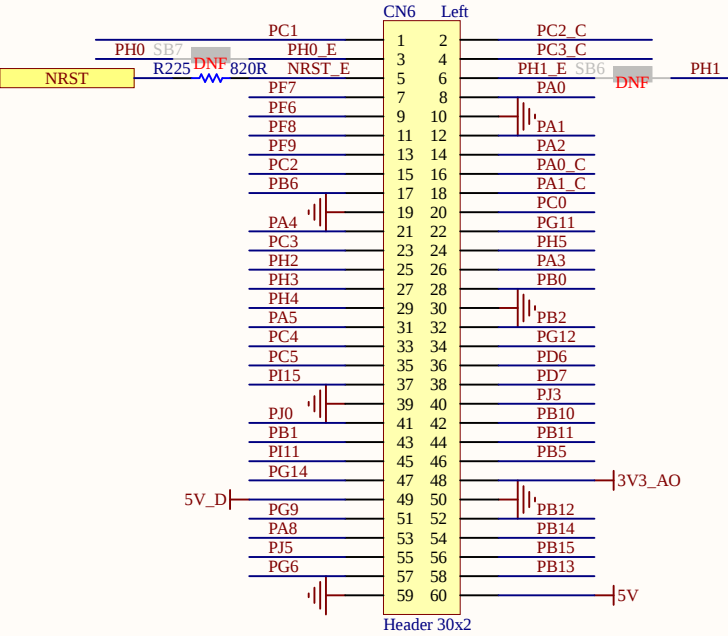
LIMITATIONS :
See user manual

MOTOR CONTROL JOYSTICK (OPTIONAL : not fitted)

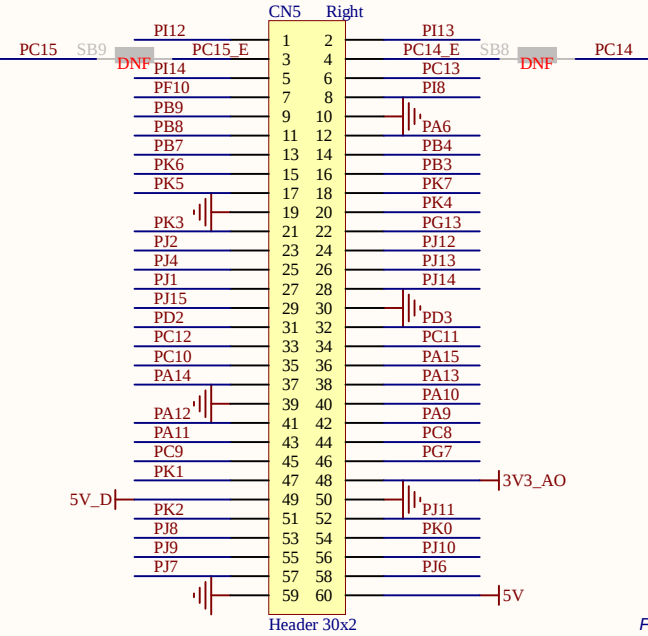


LIMITATIONS :
See user manual

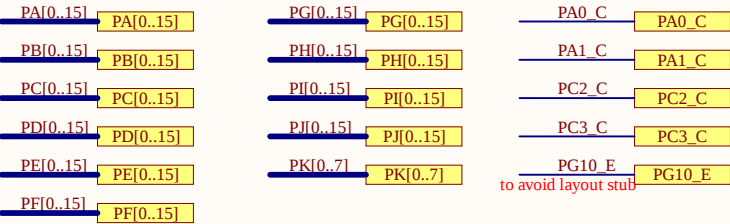
MCU EXTENSION CONNECTORS



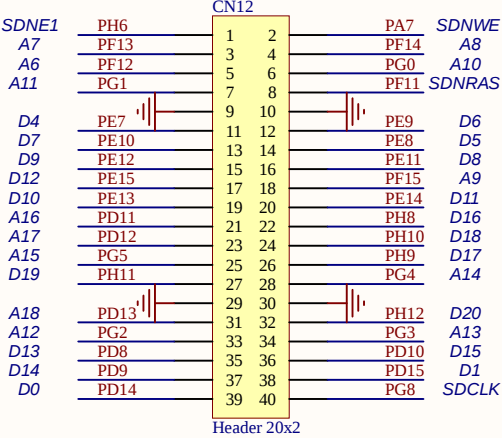
FTR-130-03-L-D-LC (Samtec)
or FTR-130-53-L-D-LC (Samtec) ?



FTR-130-03-L-D-LC (Samtec)
or FTR-130-53-L-D-LC (Samtec) ?

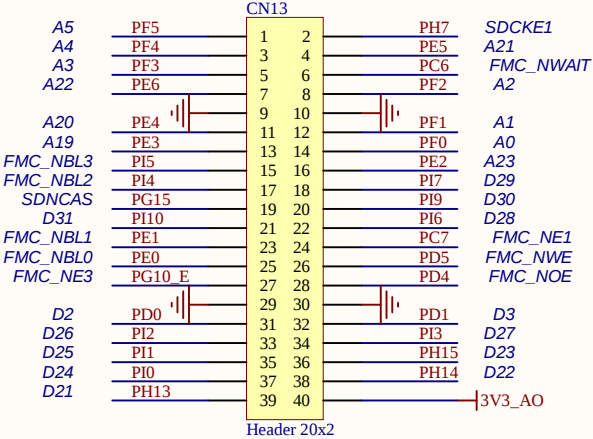


Place close Memory



FTR-120-03-L-D-LC (Samtec)
or FTR-120-53-L-D-LC (Samtec) ?

Place close Memory

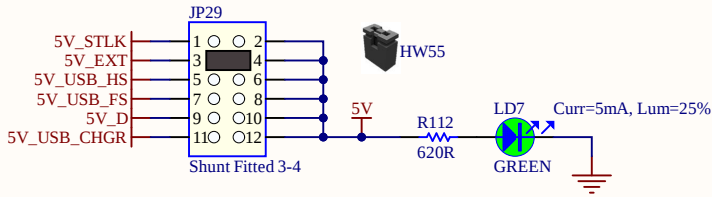


FTR-120-03-L-D-LC (Samtec)
or FTR-120-53-L-D-LC (Samtec) ?

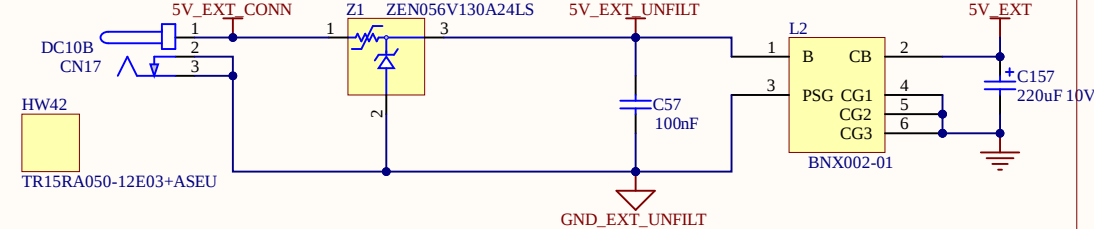


BOARD POWER

5V Power Supply options

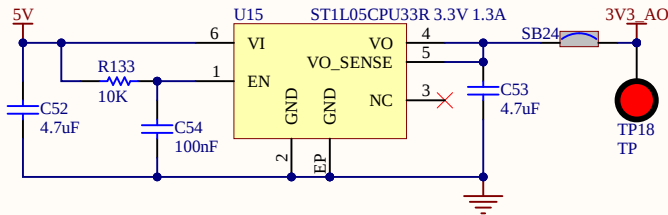


5V External supply (Always ON)

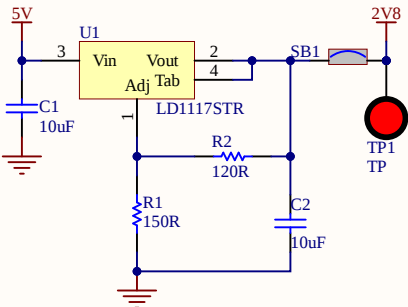


3V3 Supply (Always ON)

See Power MCU page
(also provides power to MCU VDD)

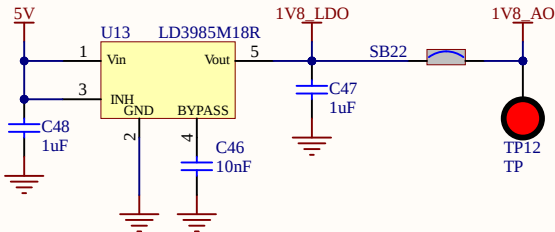


2V8 supply (Always ON)

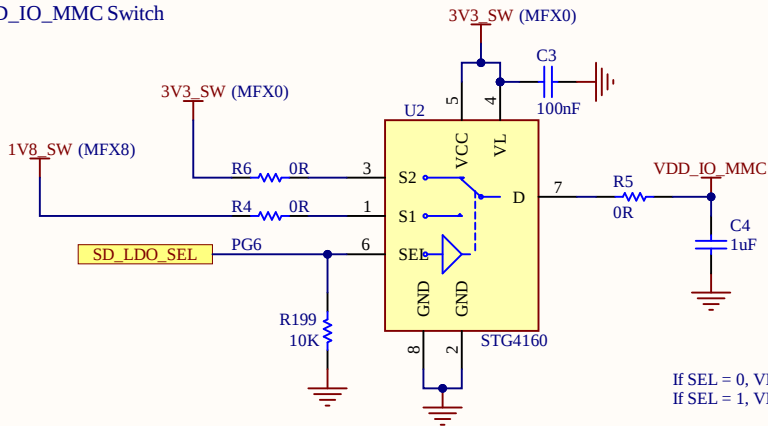


1V8 (Always ON)

See Power MCU page : can be replaced by MCU internal SMPS



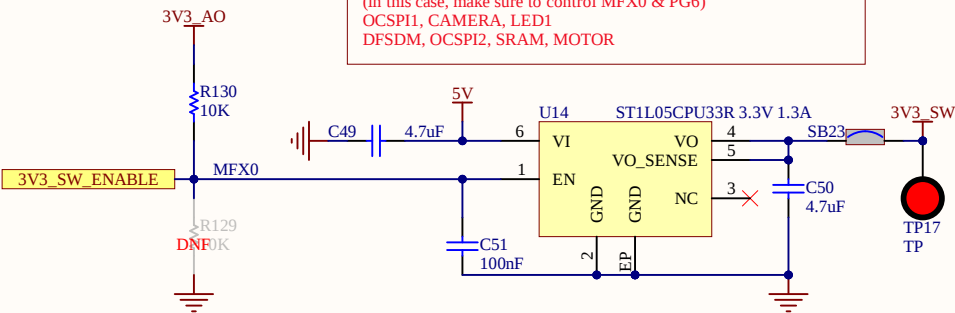
VDD_IO_MMC Switch



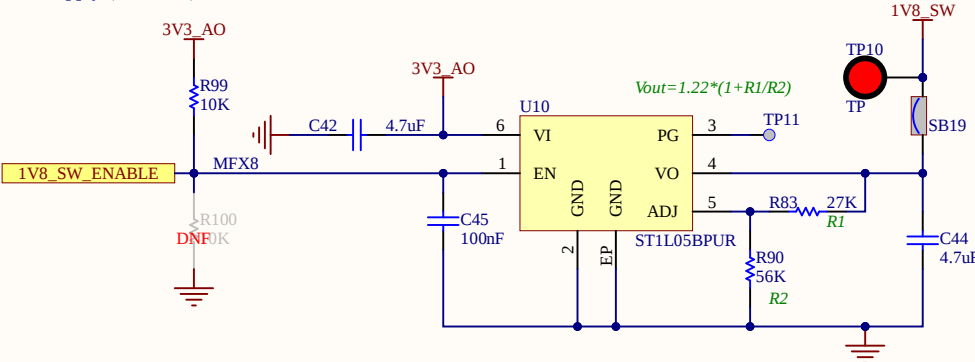
If SEL = 0, VDD_MMC = 3V3 (default)
If SEL = 1, VDD_MMC = 1V8

3V3 Supply (Switched)

SD CARD 2 is supplied by VDD_IO_MMC
(in this case, make sure to control MFX0, MFX8 & PG6)
Following interfaces are supplied by VDD_IO_MMC = 3.3V only
(in this case, make sure to control MFX0 & PG6)
OCSP11, CAMERA, LED1
DFSMD, OCSP12, SRAM, MOTOR

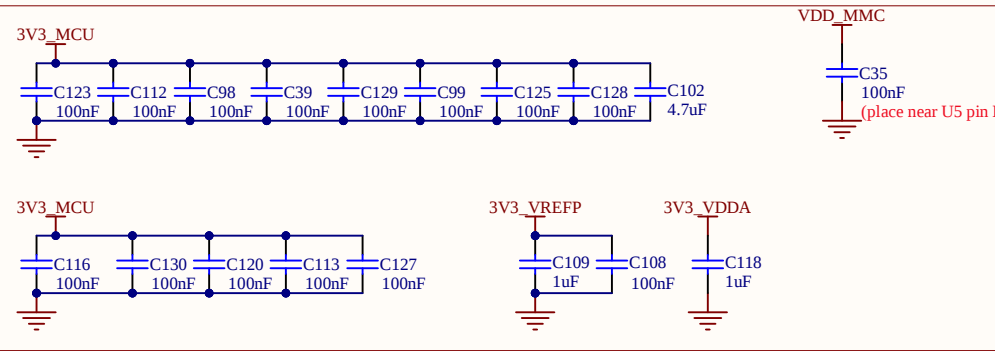
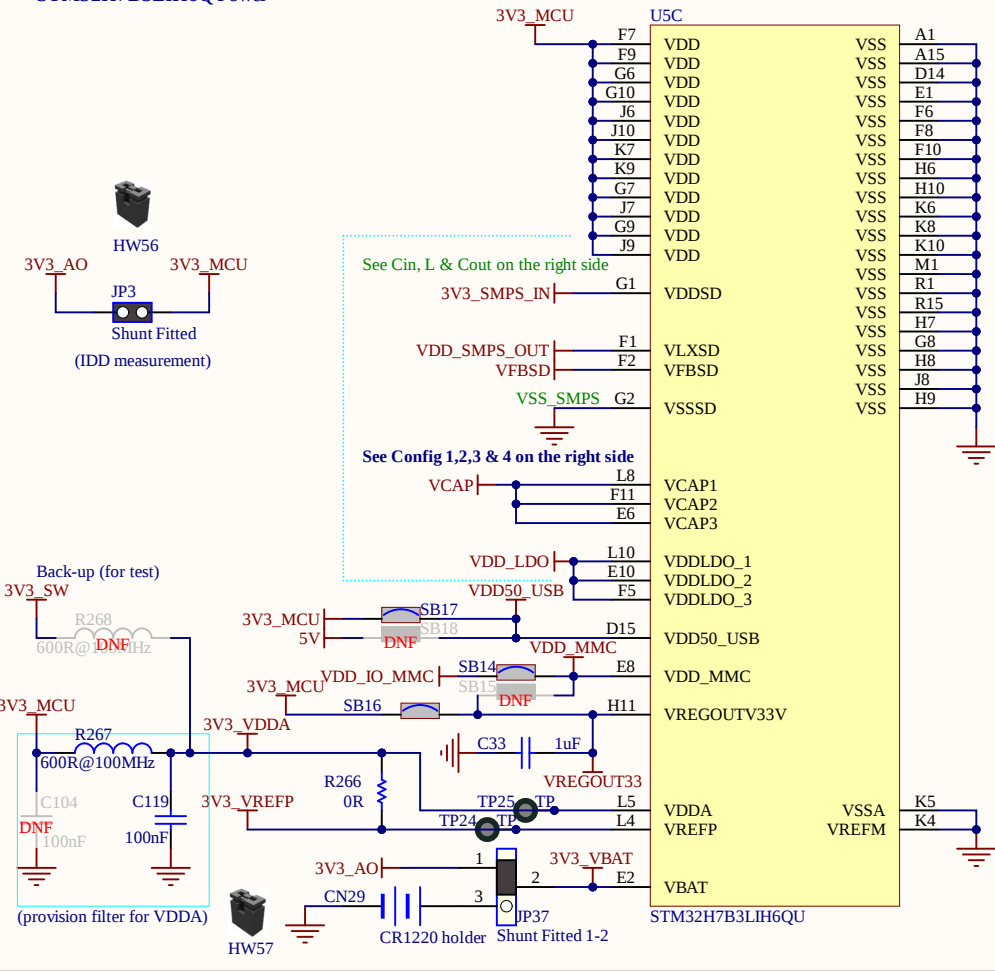


1V8 Supply (Switched)



MCU POWER

STM32H7B3LIH6Q Power



Internal LDO/SMPS Supply Configuration

For further details, please see UM2662 User Manual and RM0455 STM32H7A3 Reference Manual

Supply Config 1 : LDO only (SMPS OFF, LDO ON)

3V3_MCU, VDD_LDO, VFBS, R251, 2x2.2uF instead of 2x100nF near VCAP pins / plan

Disconnect 3V3_SMPS_IN from 3V3_MCU
Connect 3V3_SMPS_IN to GND
Connect VDD_SMPS_IND_OUT to GND
Connect VDD_LDO to 3V3_MCU
2 x 2.2uF near VCAP plans/pins

Supply Config 2 : SMPS only (SMPS ON, LDO OFF)

Default config

3V3_MCU, 3V3_SMPS_IN, VDD_SMPS_OUT, VDD_SMPS_IND_OUT, VCAP, R22, 0R, Cin near VDDSD pin, C27, 10uF, C28, 10uF, L1, 2.2uH, 1.2A, C29, 100pF, Cfit, L near VLX pin, C24, 10uF, Cout near L, C121, 100nF, C126, 100nF, VSS_SMPS, VDD_LDO, SB3, SB5, SB17, SB18, SB14, SB15, SB16, SB19, SB20, SB21, SB22, SB23, SB24, SB25, SB26, SB27, SB28, SB29, SB30, SB31, SB32, SB33, SB34, SB35, SB36, SB37, SB38, SB39, SB40, SB41, SB42, SB43, SB44, SB45, SB46, SB47, SB48, SB49, SB50, SB51, SB52, SB53, SB54, SB55, SB56, SB57, SB58, SB59, SB60, SB61, SB62, SB63, SB64, SB65, SB66, SB67, SB68, SB69, SB70, SB71, SB72, SB73, SB74, SB75, SB76, SB77, SB78, SB79, SB80, SB81, SB82, SB83, SB84, SB85, SB86, SB87, SB88, SB89, SB90, SB91, SB92, SB93, SB94, SB95, SB96, SB97, SB98, SB99, SB100

Connect 3V3_SMPS_IN to 3V3_MCU
Connect VDD_SMPS_IND_OUT to VCAP1/2/3
2x100nF near VCAP plans/pins

Supply Config 3 : SMPS & LDO cascaded (SMPS & LDO ON)

VDD_LDO, VFBS, R262, 2x100nF near VDDLDO pins / plan, C124, 100nF, C122, 100nF

Compared to config 2 :
Disconnect VDD_SMPS_IND_OUT from VCAP1/2/3
Connect VDD_SMPS_IND_OUT to VDD_LDO
Add 2x100nF near VDDLDO pins/plans
Add 2x2.2uF near VCAP pins/plans (see config 1)

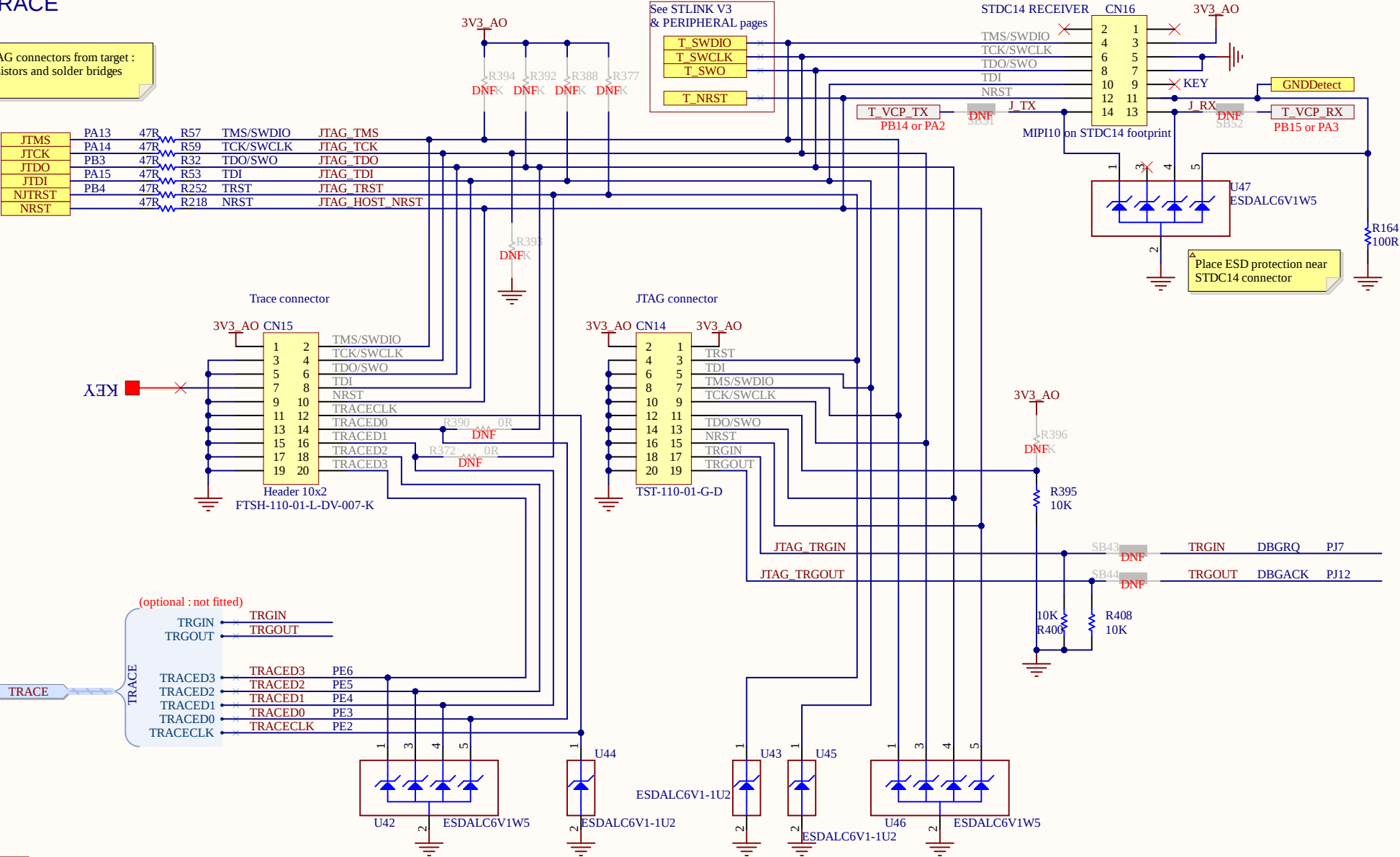
Supply Config 4 : same as config 3, but SMPS supplies also 1V8 to board

VDD_SMPS_IND_OUT, 1V8_AO, SB4, DNF, C21, 4.7uF

Compared to config 3
Connect VDD_SMPS_IND_OUT to 1V8 board supply
Add a 10uF close to the 1.8V board supply
Add a 10uF close to one VDD_LDO pin

JTAG & TRACE
(Always ON)

To disconnect JTAG connectors from target :
- Remove 47R resistors and solder bridges



LIMITATIONS :
see User Manual



(Always ON)

Must be on a border or the PCB.

Header 4x1

Silkscreen = Reserved

3V3_STLK

X4

VDD OUT 3

EN GND 2

NZ2520SH 25MHz

R145 100R

G1

H1

OSC_IN/PH0

OSC_OUT/PH1

J1

NRST

D6

BOOT0

C6

PDR_ON

C68 100nF

3V3_STLK

Header 2x1

Silkscreen = NRST

C77 2.2uF

R165 3K

J14

J15

V12_OTGPHY

REXT_OTGPHY

U21A

STLK_SWDIR/PA7

STLK_SWCLK/PA14

USB_DEV_HS_N/R14

USB_DEV_HS_P/R15

USB_DEV_HS_N/PB14

USB_DEV_HS_P/PB15

T_SW_DIR/PA7

T_SWDIR_IN/PH7

T_SWDIR_OUT/PH9

T_SWCLK/PH6

T_SWO/PD2

STLK_VCP_RX/PG9

STLK_VCP_TX/PG14

GNDDetect/PG5

T_VCC_AIN/PA0

T_PWR_EXT/PB1

T_PWR_EN/PB0

STLK_LED/PA10

STLK_MCO/PA8

T_NRST/PA6

HW_TYP_0/PI4

HW_TYP_1/PI5

ST-LinkV3E SWD

R3

N12

L2

M11

D12

T SWDIR IN

T SWDIRa

T SWCLKa

T SWOa

R157 100R

R409 0R

R401 0R

R399 0R

T SWCLK PA13

T SWCLK PA14

T SWO PB3

See JTAG page

T SWDIR

T SWCLK

T SWO

C10

A7

STLK VCP RX

STLK VCP TX

SB42

SB41

T VCP TX

T VCP RX

PB14 or PA2

PB15 or PA3

3V3 AO

K13

N3

R4

R5

GNDDetect

T_PWR_EXT

T_PWR_EN

R146 4K7

R147 4K7

5V

R153 2K7

R154 4K7

See JTAG page

D15

F15

P3

D4

C4

LED_STLK

STLK_MCO

T_NRSTa

R398 0R

T_NRST

TP22

0R must be close to STDC14 connector
To disconnect STLINK V3 from target :
- Remove 0R resistors and solder bridges

LIMITATIONS (see MCU page):

Back up : if SD CARD 2, use UART VCOM back-up (PB14/PB15)

[illegible]

The diagram shows the electrical connections for the USB-to-UART bridge and the 5V ST-LINK power section.

USB-to-UART Bridge:

- USB Micro-Breceptacle (CN21):**
 - Pin 1: VBUS
 - Pin 2: DM
 - Pin 3: DP
 - Pin 4: ID
 - Pin 5: GND
 - Pin 6: Shield
 - Pin 7: Shield
 - Pin 8: Shield
 - Pin 9: Shield
 - Pin 10: EXP
 - Pin 11: EXP
- 5V_USB_CHGR:**
 - Pin 1: Connected to VBUS (Pin 1 of CN21) through capacitor C72 (4.7uF).
 - Pin 2: Connected to DM (Pin 2 of CN21).
 - Pin 3: Connected to DP (Pin 3 of CN21).
 - Pin 4: Connected to ID (Pin 4 of CN21).
 - Pin 5: Connected to GND (Pin 5 of CN21).
- ESDA7P60-1U1M (U23):**
 - Pin 1: Connected to 5V_USB_CHGR Pin 1.
 - Pin 2: Connected to DM (Pin 2 of CN21).
- ECMF02-2AMX6 (U26):**
 - Pin 1: NC
 - Pin 2: GND
 - Pin 3: D-
 - Pin 4: D+
 - Pin 5: D-
 - Pin 6: D+
- USB_DEV_HS_CN_N (U27):**
 - Pin 1: Connected to DM (Pin 2 of CN21).
 - Pin 2: Connected to DP (Pin 3 of CN21).
 - Pin 3: Connected to ID (Pin 4 of CN21).
 - Pin 4: Connected to GND (Pin 5 of CN21).
- USB_DEV_HS_CN_P (U28):**
 - Pin 1: Connected to DP (Pin 3 of CN21).
 - Pin 2: Connected to ID (Pin 4 of CN21).
 - Pin 3: Connected to GND (Pin 5 of CN21).

5V ST-LINK Power Section:

- 5V_USB_CHGR:**
 - Pin 1: Connected to VBUS (Pin 1 of CN21) through capacitor C70 (1uF).
 - Pin 2: Connected to DM (Pin 2 of CN21).
 - Pin 3: Connected to DP (Pin 3 of CN21).
 - Pin 4: Connected to ID (Pin 4 of CN21).
 - Pin 5: Connected to GND (Pin 5 of CN21).
- TP20 (TP):**
 - Pin 1: Connected to VBUS (Pin 1 of CN21) through capacitor C70 (1uF).
 - Pin 2: Connected to DM (Pin 2 of CN21).
 - Pin 3: Connected to DP (Pin 3 of CN21).
 - Pin 4: Connected to ID (Pin 4 of CN21).
 - Pin 5: Connected to GND (Pin 5 of CN21).
- R152 (DNF):**
 - Pin 1: Connected to VBUS (Pin 1 of CN21) through capacitor C70 (1uF).
 - Pin 2: Connected to DM (Pin 2 of CN21).
 - Pin 3: Connected to DP (Pin 3 of CN21).
 - Pin 4: Connected to ID (Pin 4 of CN21).
 - Pin 5: Connected to GND (Pin 5 of CN21).
- R148 (10K):**
 - Pin 1: Connected to VBUS (Pin 1 of CN21) through capacitor C70 (1uF).
 - Pin 2: Connected to DM (Pin 2 of CN21).
 - Pin 3: Connected to DP (Pin 3 of CN21).
 - Pin 4: Connected to ID (Pin 4 of CN21).
 - Pin 5: Connected to GND (Pin 5 of CN21).

LD9

Red

1 2

3V3_STLK

4 3

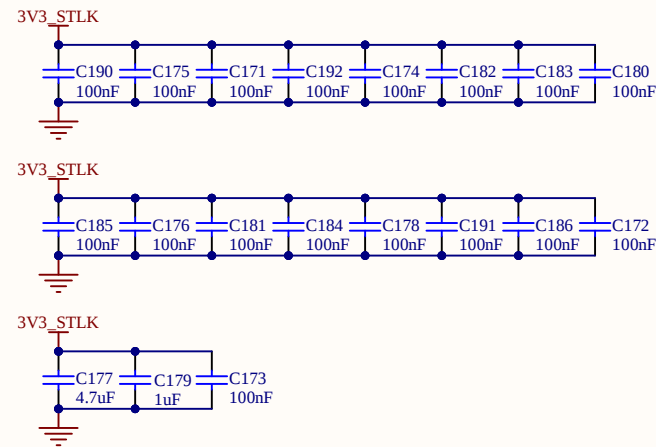
Green

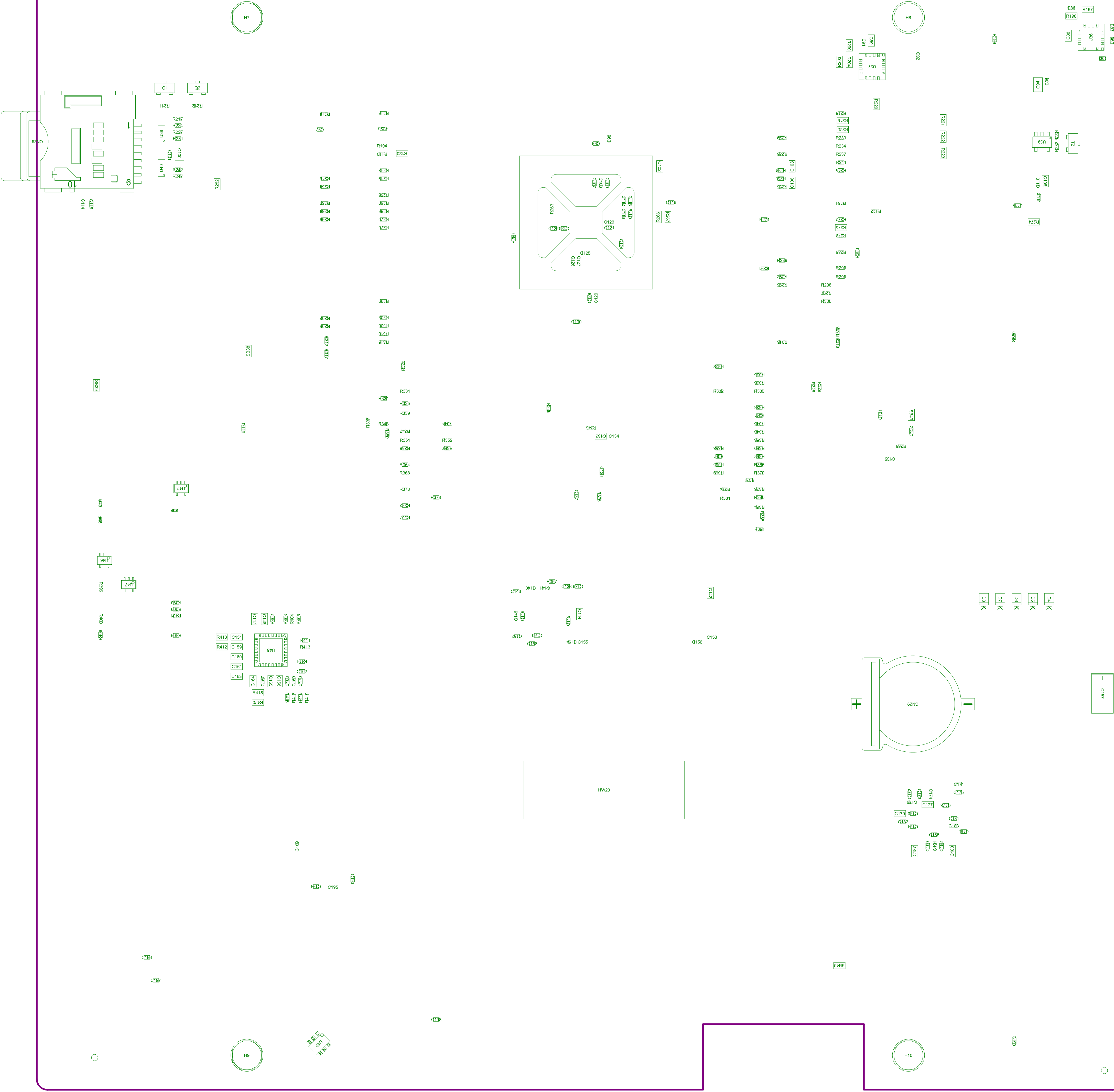
LD_BICOLOR_CMS

R190 330R

R192 330R

LED_STLK





Project: STM32H7B3I-EVAL		
Layer: M15-Bottom Assembly	Gerber:.GM15	
Variant: H7B3LIQ	Ref: MB1331	
Date: 25-MAR-20	Rev: D	