PCB Layout Recommendations for BGA Packages

Technical Note

FPGA-TN-02024-4.8

October 2021

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Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BGA	Ball Grid Array
caBGA	Chip Array BGA
csBGA	Chip-Scale BGA
csfBGA	Chip-Scale Flip-Chip BGA
fcBGA	Flip Chip BGA
FOWLCSP	Fan Out Wafer Level Chip Scale Package
fpBGA	Fine Pitch BGA
ftBGA	Thin BGA
IPC	Association Connecting Electronics Industries
JEDEC	JEDEC Solid State Technology Association
NSMD	Non-Solder Mask Defined
PBGA	Plastic BGA
PCB	Printed circuit board
QFNS	Quad Flat Pack Saw-Singulated
SBGA	Super BGA
SMD	Solder Mask Defined
TQFP	Thin Quad Flat Pack
ucBGA	Ultra Chip-Scale BGA
WLCSP	Wafer Level Chip Scale Package

1. Introduction

As Ball Grid Array (BGA) packages become increasingly popular and become more populated across the array with higher pin count and smaller pitch, it is important to understand how they are affected by various board layout techniques. This document provides a brief overview of PCB layout considerations when working with BGA packages. It outlines some of the most common problems and provides tips for avoiding them at the design stage. A key challenge of adopting fine-pitch (0.8 mm or less) BGA packages is the design of a route fanout pattern that maximizes I/O utilization while minimizing fabrication cost. This technical note provides an overview of PCB design examples provided by Lattice Semiconductor.

For more information and design examples, go to the Solutions page (Development Boards and Kits) of the Lattice Semiconductor web site (http://www.latticesemi.com/en/Products/DevelopmentBoardsAndKits).

2. Lattice BGA Package Types

Table 2.1. Lattice BGA Package Types

Package Type	Description
PBGA	**Plastic BGA** with 1.27 mm solder ball pitch. Die up configuration.
fpBGA	**Fine Pitch BGA** – Plastic BGA with 1.0 mm solder ball pitch. Die up configuration.
ftBGA	**Fine Pitch Thin BGA** – Thin plastic BGA with 1.0 mm solder ball pitch. Die up configuration.
caBGA	**Chip Array BGA** – Plastic BGA with 0.8 mm solder ball pitch. Die up configuration.
csBGA	**Chip Scale BGA** – Plastic BGA with 0.5 mm solder ball pitch. Die up configuration.
csfBGA	**Chip Scale Flip-Chip BGA** – Plastic chip scale BGA with 0.5 mm solder ball pitch.
fcBGA	**Flip-Chip BGA** with 1.0 mm solder ball pitch. Die down configuration.
FOWLCSP	**Fan Out Wafer Level Chip Scale Package -** Saw-singulated package with 0.5 mm ball pitch built onto a silicon device with a redistribution layer. Die down configuration.
SBGA	**Super BGA** – Similar to PBGA, but with an integrated heatsink plate. This package has 1.27 mm solder ball pitch and die down configuration. SBGA packages offer enhanced thermal dissipation capability.
ucBGA	**Ultra Chip BGA** – Saw-singulated plastic ball grid array package with 0.4 mm ball pitch.
WLCSP	**Wafer-Level Chip Scale Package** – Saw-singulated package with 0.35 mm and 0.4 mm ball pitch built onto a silicon device. Die down configuration.

3. BGA Board Layout Recommendations

To evenly balance the stress in the solder joints, Lattice recommends that PCB solder pads match the corresponding package solder pad type.

Table 3.1. Lattice BGA Package SMD/NSMD Pad Opening

	Package Solder Pad Type	Package BGA Solder Mask Opening – Diameter (mm)	Package BGA Pad Opening (mm)
0.35 mm Ball Pitch			
16, 25 WLCSP	NSMD (Figure 3.1)		0.200
36 WLCSP (Option 1[3])	NSMD (Figure 3.1)		0.200
0.4 mm Ball Pitch			
25 WLCSP	NSMD (Figure 3.1)		0.250
30 WLCSP	NSMD (Figure 3.1)		0.260
36 WLCSP (Option 3[5])	NSMD (Figure 3.1)		0.200
36 WLCSP (Option 2[4]), 81 WLCSP	NSMD (Figure 3.1)		0.230
49 WLCSP	NSMD (Figure 3.1)		0.235
72 WLCSP	NSMD (Figure 3.1)		0.240
36, 49 ucBGA	SMD (Figure 3.2)	0.200	
64, 81, 121, 132, 225 ucBGA	SMD (Figure 3.2)	0.220	
0.5 mm Ball Pitch			
56, 132, 328 csBGA	SMD (Figure 3.2)	0.300	
64, 81, 100, 121, 144, 196, 284 csBGA	SMD (Figure 3.2)	0.250	
132 csBGA (Option2[3])	SMD (Figure 3.2)	0.300	
184 csBGA	SMD (Figure 3.2)	0.275	
289 csBGA	SMD (Figure 3.2)	0.275	
121, 285 csfBGA	SMD (Figure 3.2)	0.250	
256, 324 csfBGA	SMD (Figure 3.2)	0.300	
256 FOWLCSP[6]	SMD (Figure 3.2	0.280	
0.65 mm Ball Pitch			
80 ckfBGA	SMD (Figure 3.2)	0.300	
80 ctfBGA	SMD (Figure 3.2)	0.250	
0.80 mm Ball Pitch			
100, 196, 256, 324, 332, 400, 484 caBGA	SMD (Figure 3.2)	0.400	
121 caBGA	SMD (Figure 3.2	0.350	
381, 554, 756 caBGA	SMD (Figure 3.2)	0.300	
1.00 mm Ball Pitch			
256 ftBGA (Option 1[1]), 256 ftBGA (Option 2[1]), 256 ftBGA (Option3[4])	SMD (Figure 3.2)	0.450	
237, 324 ftBGA	SMD (Figure 3.2)	0.450	
100, 144, 208, 256, 388, 484, 672, 676, 900, 1152, 1156 fpBGA	SMD (Figure 3.2)	0.450	
672 fcBGA[6]	SMD (Figure 3.2	0.480	
1020, 1152, 1704 Organic fcBGA	SMD (Figure 3.2)	0.450	

	Package Solder Pad Type	Package BGA Solder Mask Opening – Diameter (mm)	Package BGA Pad Opening (mm)
1.27 mm Ball Pitch			
272 PBGA	SMD (Figure 3.2)	0.600	
388 PBGA	SMD (Figure 3.2)	0.630	
256, 352 SBGA	SMD (Figure 3.2)	0.580	

Notes:

1. ispMACH® 4000, MachXO™ and LatticeXP2™
2. LatticeECP3™ and MachXO2™
3. iCE40™
4. MachXO, MachXO2 and MachXO3™
5. CrossLink™
6. CertusPro™-NX

Table 3.2. PCB SMD/NSMD Pad Recommendations[1]

	Optimum PCB SMD Solder Mask Opening (mm) Figure 3.4	Optimum PCB NSMD Solder Land Diameter (mm) Figure 3.3
0.35 mm Ball Pitch		
16, 25 WLCSP, 36 WLCSP (Option 1[4])	0.200	0.200[7]
0.4 mm Ball Pitch		
36, 49, 64, 81, 121, 132, 225 ucBGA	0.200[7]	0.170
25 WLCSP	0.200	0.200[7]
30 WLCSP	0.200	0.200[7]
36 WLCSP (Option 3[5]), 36 WLCSP (Option 2[6]), 49, 81 WLCSP	0.250	0.250[7]
72 WLCSP	0.270	0.250
0.5 mm Ball Pitch		
56, 64, 81, 100, 121, 132, 144, 184, 196, 284, 328 csBGA	0.250[7]	0.230
132 csBGA (Option2[4])	0.275[7]	NA
289 csBGA	0.290	0.350
285 csfBGA	0.280[7]	0.340
121, 256, 324 csfBGA	0.300[7]	0.350
256 FOWLCSP	0.300	0.250
0.65 mm Ball Pitch		
80 ckfBGA/ctfBGA	0.300[7]	0.200
0.80 mm Ball Pitch		
100, 121, 256, 324, 332, 484 caBGA	0.400[7]	0.350
196 caBGA	0.500	0.450
381, 400, 554, 756 caBGA	0.500[7]	0.400
1.00 mm Ball Pitch		
100 fpBGA, 256 ftBGA (option 1[2]), 256 ftBGA (option 3[5])	0.400[7]	0.350
237 ftBGA	0.550[7]	0.450
256 ftBGA (option 2[3]), 324 ftBGA, 144, 208, 256, 388, 484, 672, 676, 900, 1152, 1156 fpBGA	0.450[7]	0.400
1020, 1152, 1704 Organic fcBGA	0.550[7]	0.520
1.27 mm Ball Pitch		
272, 388 PBGA, 256, 352 SBGA	0.630[7]	0.580

Notes:

1. These Lattice recommended PCB design values results in optimum Board Level Reliability (BLR) performance for each corresponding package. Designers who use PCB design values which deviate from these recommendations should understand that the BLR performance may be reduced.
2. ispMACH 4000, MachXO, and LatticeXP2 (refer to the Package Diagrams document for MachXO options)
3. LatticeECP3 and MachXO2 (refer to the Package Diagrams document for MachXO2 options)
4. iCE40
5. MachXO, MachXO2, and MachXO3 (refer to the Package Diagrams document for MachXO and MachXO2 options)
6. CrossLink
7. Recommended value based on package solder pad type (refer to BGA Board Layout Recommendations section)

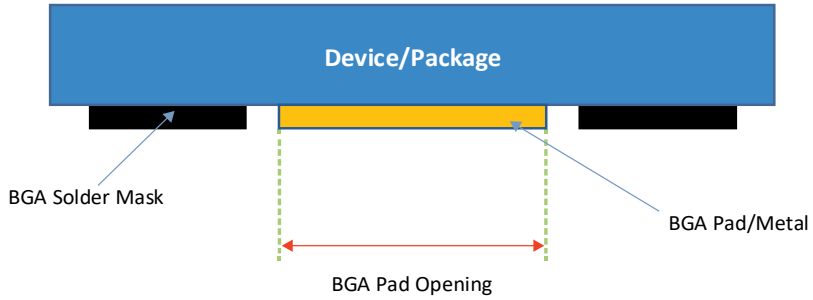

Figure 3.1. Device/Package (NSMD)

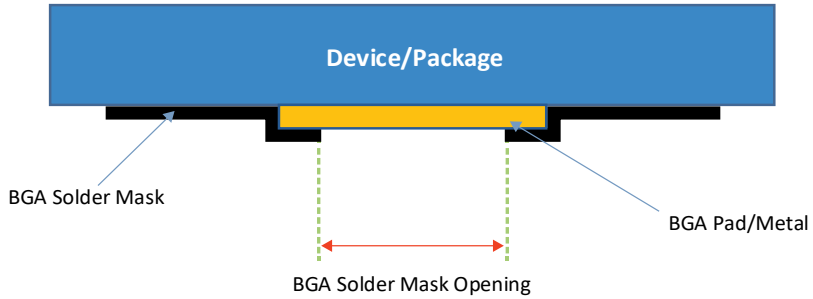

Figure 3.2. Device/Package (SMD)

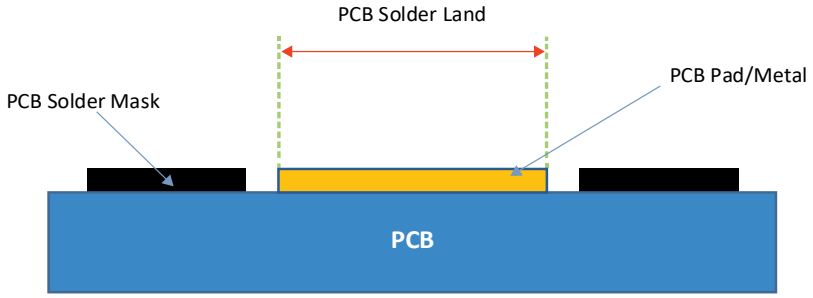

Figure 3.3. PCB (NSMD)

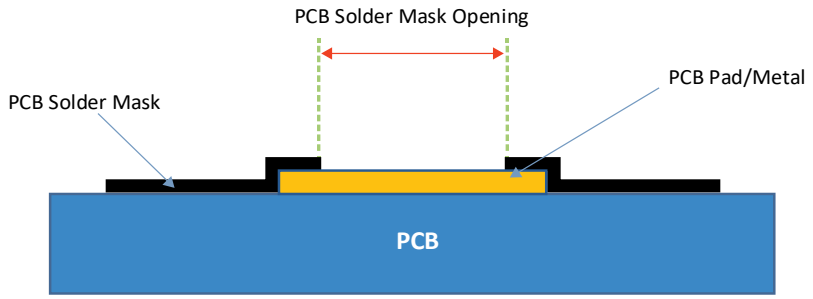

Figure 3.4. PCB (SMD)

4. BGA Breakout and Routing Examples

Lattice provides several resources and different design implementations that show BGA breakout and routing of various fine-pitch BGA packages. Different stack up and layer counts are also used to show a range of design rules and fabrication costs. It is important to consult with your board fabrication and assembly houses as to the most economical and reliable process for your application.

Currently there is a wide choice of BGAs from Lattice, with many devices offered in multiple packages and pitches of BGA densities as well as non-BGA options such as TQFP, QFN and others. The BGA pitch or “center to center” ball dimensions include, 1.00 mm BGAs, space-saving 0.5 mm pitch chip scale BGA and 0.4 mm pitch ultra chip scale BGA packages. Fine pitch packages offer advantages and disadvantages alike. Finer pitch means that the trace and space limits is adjusted down to match the BGA. Many times a design can get away with small traces underneath the BGA then fan out with a slightly larger trace width. The PCB fabrication facility is aware of your design objectives and check for the smallest trace dimensions supported. Smaller traces take more time to inspect, check and align, and others. Etching needs to be closely monitored when trace and space rules reach their lower limit.

The combination of fanout traces, escape vias, and escape traces that allow routing out from under the BGA pin array to the perimeter of the device are collectively referred to as the *BGA breakout*. The fanout pattern arranges the breakout via, layer, and stack-up to maximize the number of I/O that can be routed. Fanout patterns are an important consideration for devices over 800 pins and can be follow polar (north/south/east/west) or layer- biased directions. (Source: BGA Breakouts and Routing, Charles Pfeil, Mentor Graphics).

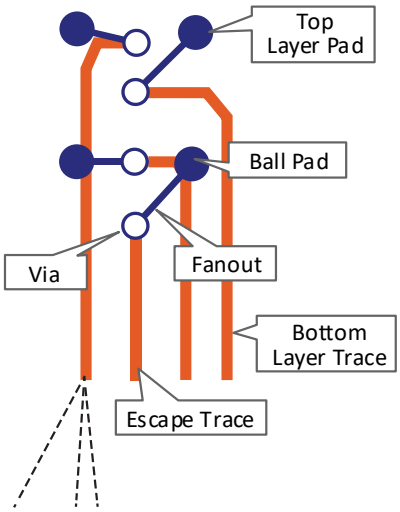

Figure 4.1. BGA Breakout Routing Terms

Lattice provides BGA breakout and routing examples for various fine pitch packages (http://www.latticesemi.com/en/Products/DevelopmentBoardsAndKits). Each package example is built to comply with IPC7351 (www.ipc.org) specifications and nomenclature conventions. Some examples include different layout options depending on design and cost goals. For example, the 256-ball chip array BGA (BN256/BG256) examples demonstrate a design with fully utilized I/O, fine trace width and pitch, on a 6-layer PCB stack-up and a less expensive design with relaxed design rules, and fewer I/O pads routed, on a 4-layer PCB stack up.

Table 4.1. Package Layout Example Summary

Package	Example #	Pitch (mm)	Signal/ Power Layers	Trace/ Width Space (mm)	Ball Pad (mm)	Ball Mask (mm)	Via Pad (mm)	Via Drill (mm)
MN64/MG64	1	0.5	6	0.100/0.100	0.23	0.33	0.30	0.125
UMN64/UMG64	1	0.4	6	0.100/0.100	0.18	0.28	0.25	0.10
MN100	1	0.5	4	0.085/0.085	0.23	0.38	0.45	0.20
	2	0.5	4	0.010/0.100	0.23	0.38	0.45	0.20
MN132/MG132	1	0.5	4	0.085/0.085	0.23	0.38	0.40	0.15
	2	0.5	4	0.100/0.100	0.23	0.38	0.40	0.15
MN144	1	0.5	6	0.100/0.100	0.23	0.33	0.30	0.125
	2	0.5	4	0.100/0.100	0.23	0.38	0.30	0.125
BN256/BG256	1	0.8	6	0.100/0.100	0.35	0.50	0.40	0.125
	2	0.8	4	0.100/0.100	0.35	0.50	0.40	0.1500
M328/MG328	1	0.5	6	0.070/0.070	0.25	0.40	0.25	0.12

Table 4.2. iCE40 Package Layout Example Summary

Package	Pitch (mm)	iCE40 Family Offering	Max. I/O	SMD/ NSMD	Total Layers	Signal Layers	Solder Pad Size (mm)	Solder Mask (mm)	Via Drill (mil)	Via Size (mil)	Trace Width (mil)	Trace Space (mil)
NSMD												
CM36	0.4	LP	25	NSMD	4	2	0.20	0.34	5	10	5	3.5
CM49	0.4	LP	35	NSMD	4	2	0.20	0.34	5	10	5	3.5
CM81	0.4	LP	63	NSMD	6	4	0.20	0.34	5	10	5	3.5
CM81	0.4	LP	48	SMD	4	2	0.20	0.20	5	10	5	3.5
CM121	0.4	LP	95	NSMD	6	4	0.20	0.34	5	10	5	3.5
CM121	0.4	LP		SMD	4	2	0.20	0.20	5	10	5	3.5
CM225	0.4	LP, HX	178	NSMD	10	6	0.20	0.34	5	10	5	3.5
CM225	0.4	LP, HX	153	SMD	8	4	0.20	0.20	5	10	5	3.5
CM225	0.4	LP, HX	100	SMD	6	2	0.20	0.20	5	10	5	3.5
CB81	0.5	LP	62									
CB121	0.5	LP	93									
CB132	0.5	HX	95	NSMD	6	4	0.254	0.4064	6	12	4	4
CB132	0.5	HX		NSMD	4	2	0.254	0.4064	5	10	3	3
CT256	0.8	HX	206	NSMD	6	4	0.32	0.47	9	18	4.5	4.25

For mechanical dimension details on packages, see the Lattice Package Diagrams document.

In order to show how some of the routing challenges are solved, examples are provided for fine-pitch BGA pack- ages from the MachXO and the ispMACH 4000ZE families. Principles for these apply to other Lattice BGA packaged products.

For iCE40 product family, all the examples assume that each I/O bank and the SPI bank each uses a different I/O voltage. In the layout examples for a reduced number of layers, all the mandatory pins connections are routed out, including connections such as the VPP_2V5 and the SPI connections. The PLL pins are also routed out on the packages that support PLLs.

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4.1. caBGA BGA Breakout Examples

4.1.1. 121-Ball caBGA BGA Breakout Example

This breakout places an ICE40HX8K in a 9 mm × 9 mm, 0.8 mm pitch, 121-ball caBGA package in a 4-layer stack up with maximum I/O utilization. This example utilizes a 0.127 mm trace width/space, escape via pad of 0.350 mm and via drill of 0.200 mm. Two metal layers are set as reference planes.

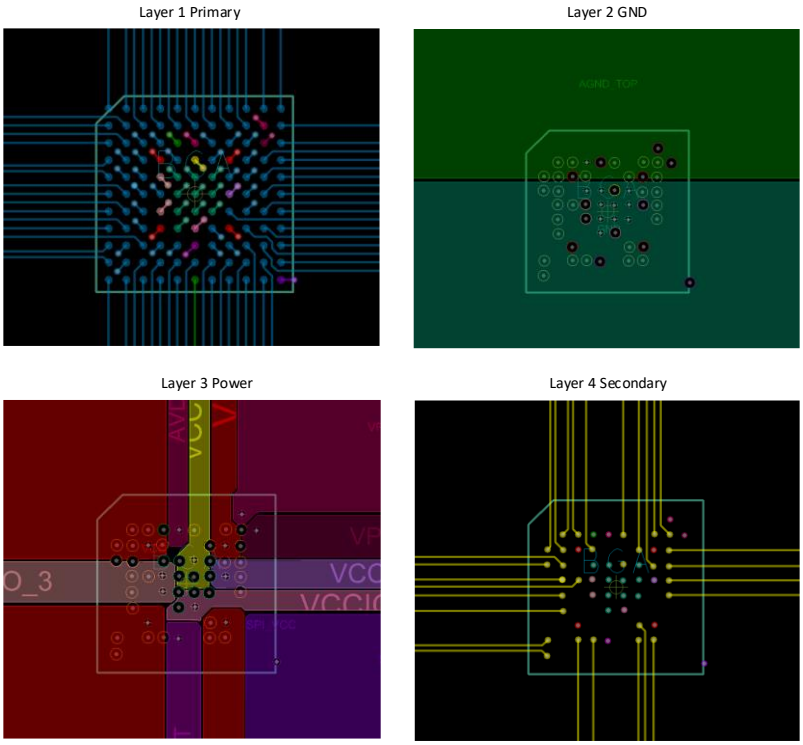


Figure 4.2. CAM Artwork Screen Shots 121-Ball caBGA

4.1.2. 196-Ball caBGA BGA Breakout Example

This breakout uses a Certus-NX in a 12 mm × 12 mm, 0.80 mm pitch, 196-ball caBGA package (LFD2NX-40-BG196) in a 6-layer stackup with maximum I/O. This example utilizes a 0.10 mm trace width/space and 0.25 mm via drill. Two internal layers are used as reference planes.

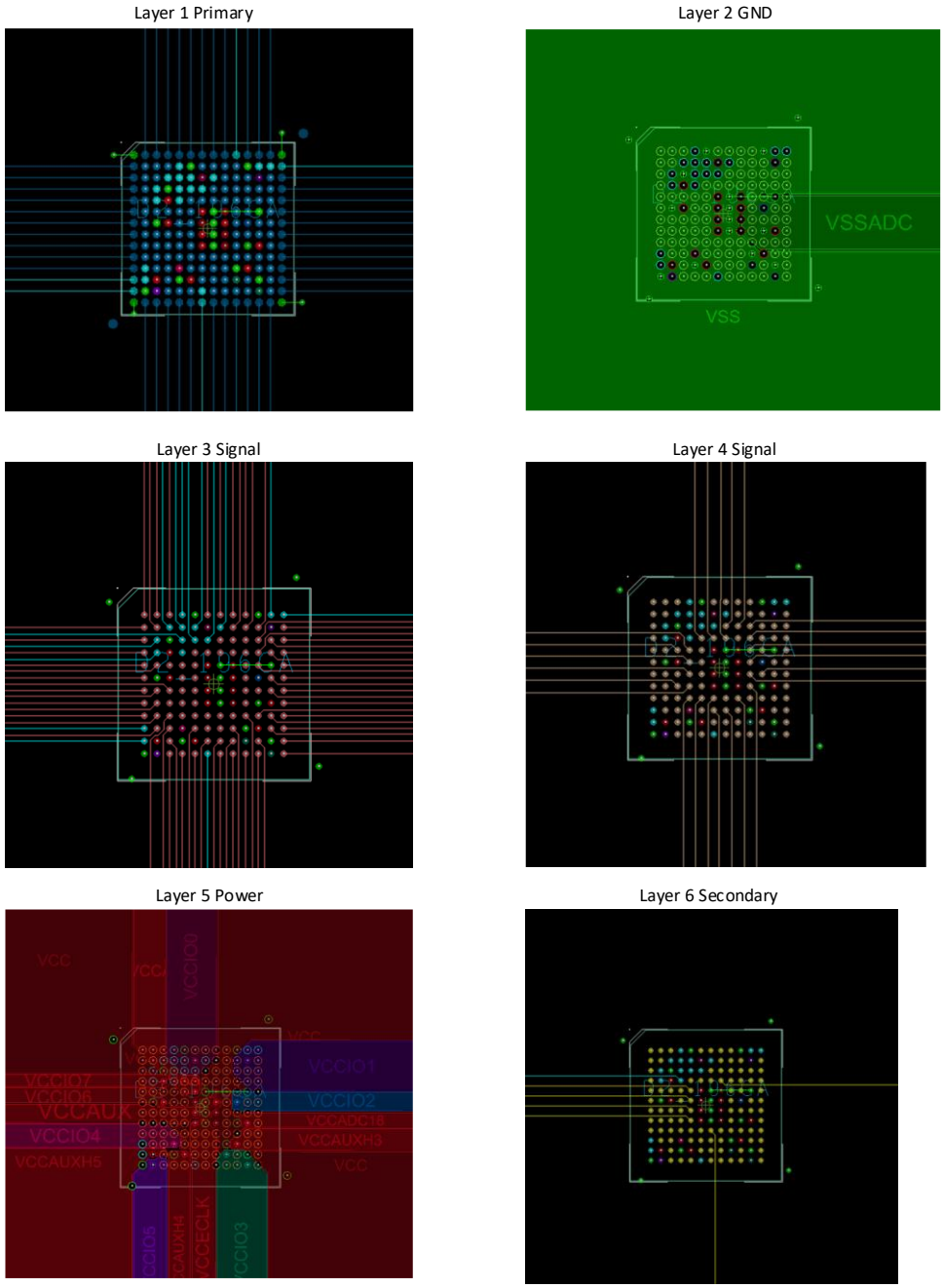


Figure 4.3. CAM Artwork Screen Shots 196-Ball caBGA

4.1.3. 256-Ball caBGA BGA Breakout Example (MachXO)

This BGA breakout and routing example places a MachXO PLD in a 14 mm × 14 mm, 0.8 mm pitch, 256-ball caBGA package (LCMXO2280-B256/BN256) into two fabrication scenarios. One for a 6-layer stack up with maximum I/O utilization and a 4-layer with about 10% fewer I/O. The 6-layer design (Example #1), demonstrates the best use of mechanically drill blind vias to place caps near power pins to minimize layers.

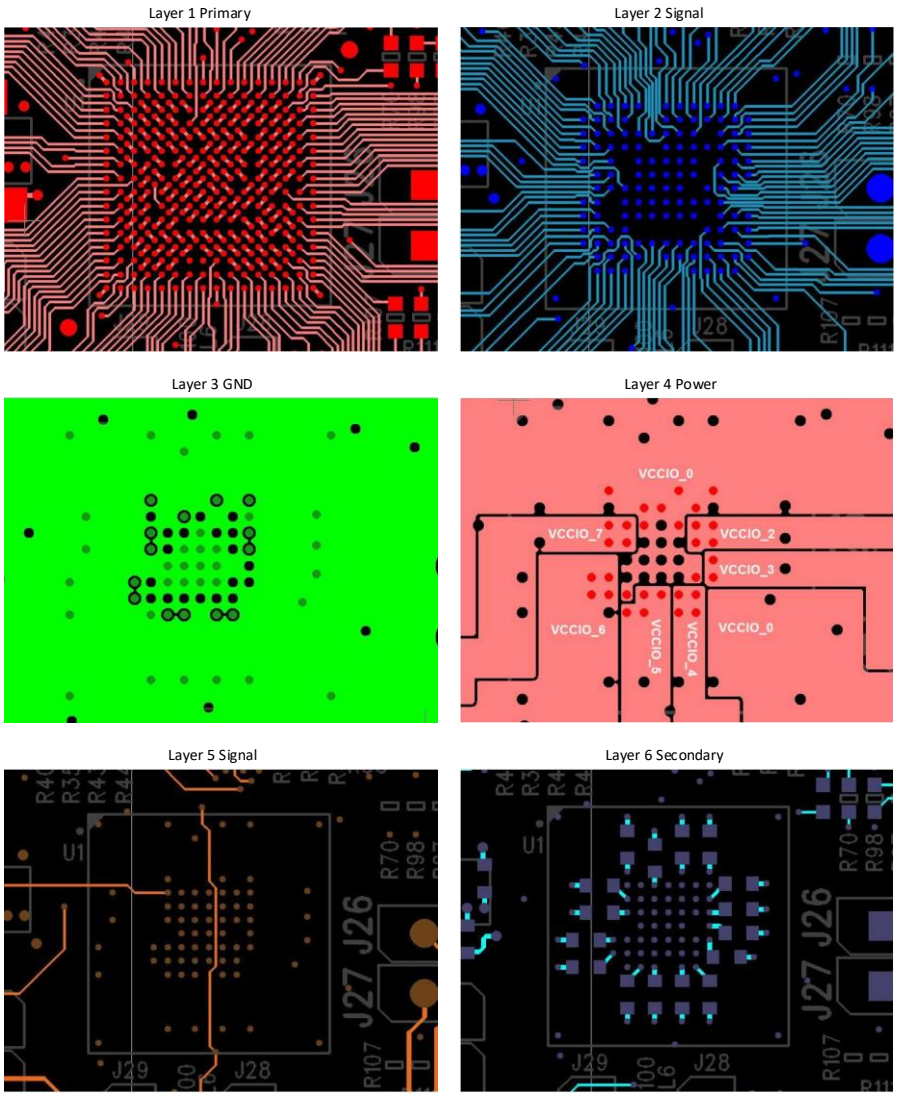


Figure 4.4. CAM Artwork Screen Shots, Example #1, 256-Ball caBGA

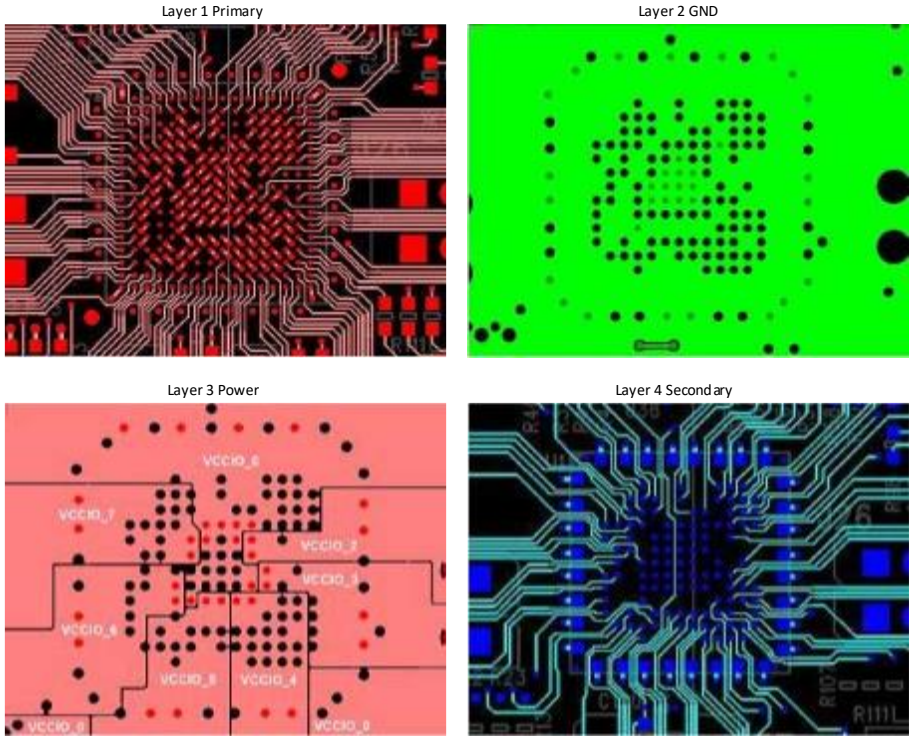


Figure 4.5. CAM Artwork Screen Shots, Example #2, 256-Ball caBGA

4.1.4. 256-Ball caBGA BGA Breakout Example (MachXO3)

This breakout uses a MachXO3 PLD in a 14 mm × 14 mm, 0.80 mm pitch, 256-ball caBGA package (MXO3L-6900-BC256) in a 6-layer stackup with maximum I/O. This example utilizes a 0.10 mm trace width/space and 0.25 mm via drill. Two internal layers are used as reference planes. VCC is tied to a plane while VCCIOs are routed and have decoupling capacitors at secondary layer.

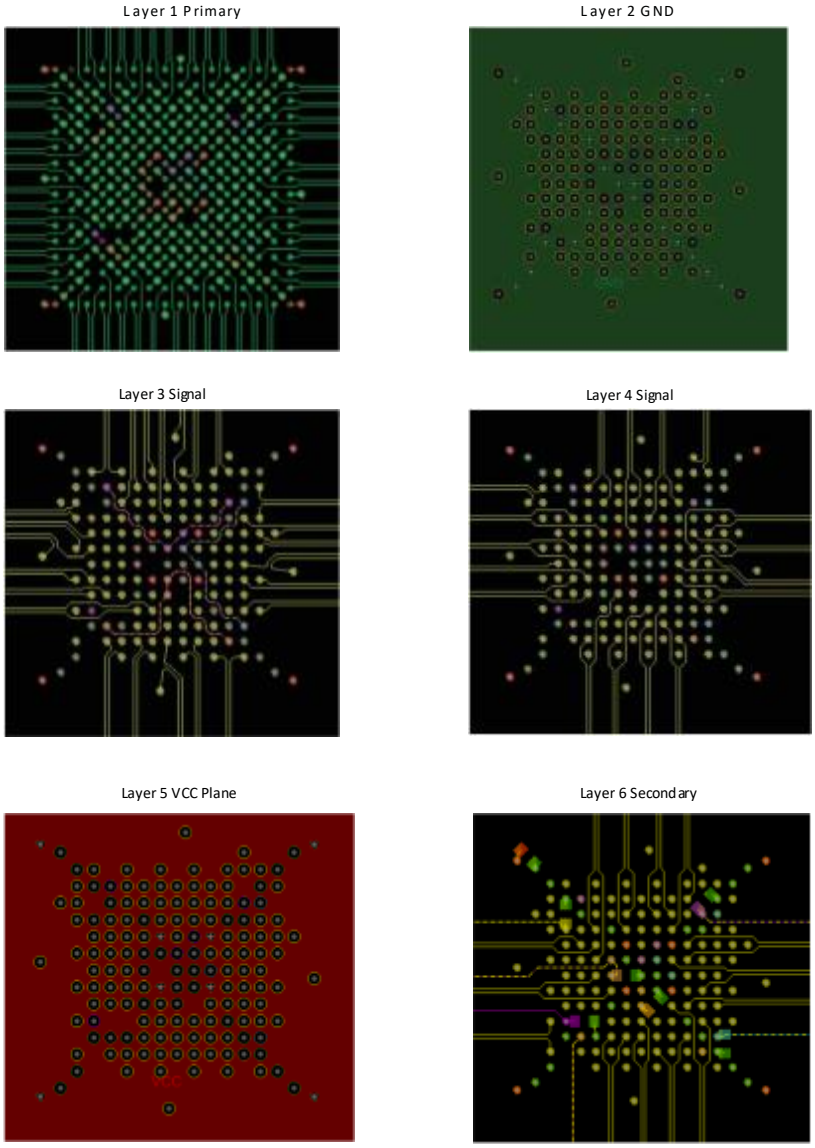


Figure 4.6. Layout Screen Shots, 256-Ball caBGA, 0.80 mm Pitch

4.1.5. 332-Ball caBGA BGA Breakout Example

This BGA breakout and routing example places a MachXO2 PLD in a 17 mm × 17 mm, 0.8 mm pitch, 332-ball caBGA package (MXO2-332-BG332) in 4-layer routing with maximum I/O utilization. This example utilizes a 0.09 mm trace width and space and 0.18 mm escape via drill. Layers have been set to use as reference planes for high speed signal traces.

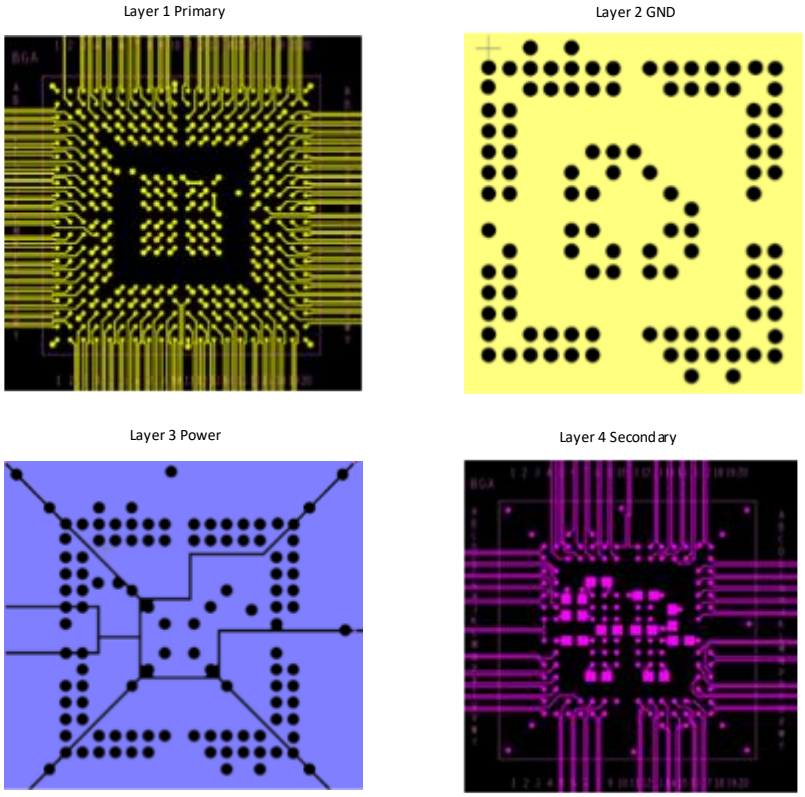


Figure 4.7. CAM Artwork Screen Shots, 332-Ball caBGA

4.1.6. 324-Ball caBGA BGA Breakout Example

This breakout uses a MachXO3 PLD in a 15 mm × 15 mm, 0.80 mm pitch, 324-ball caBGA package (MXO3L-6900-BC324) in a 6-layer stackup with maximum I/O. This example utilizes a 0.10 mm trace width/space and 0.25 mm via drill. Two internal layers are used as reference planes. VCC is tied to a plane while VCCIOs are routed and have decoupling capacitors at secondary layer.

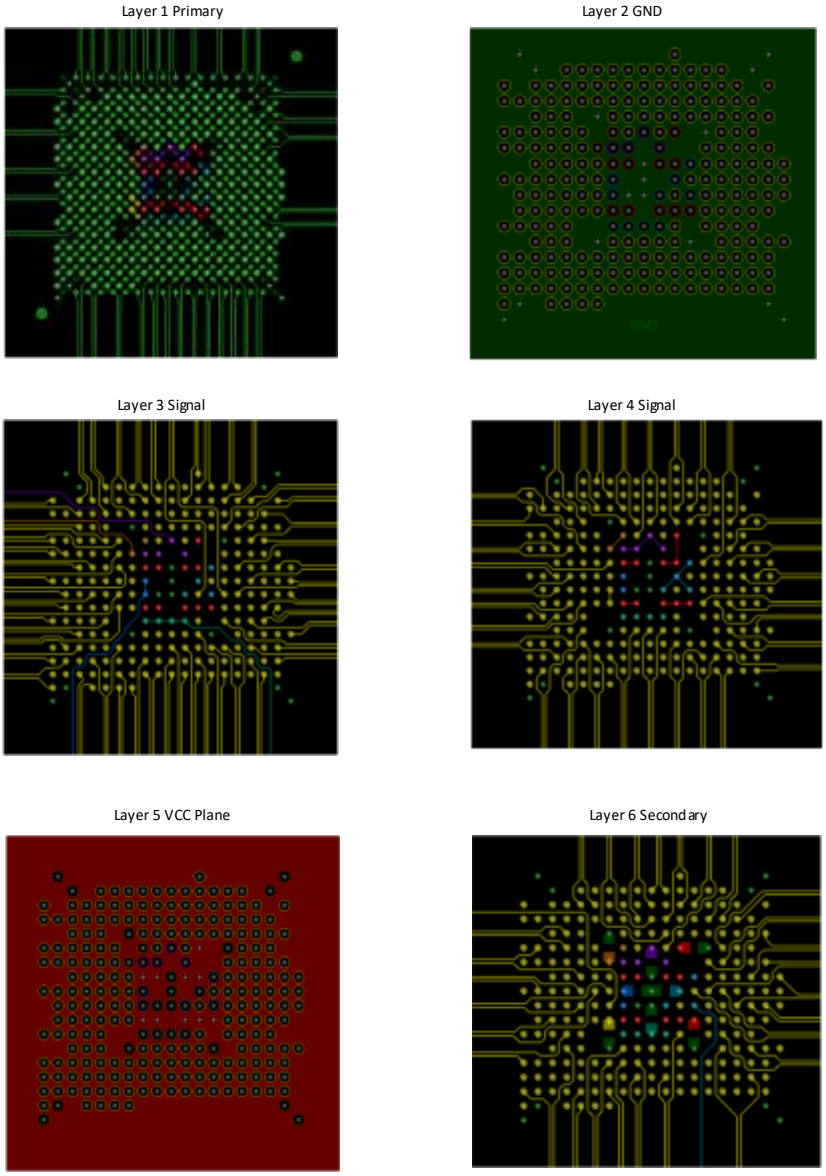


Figure 4.8. Layout Screen Shots, 324-Ball caBGA, 0.80 mm Pitch

4.1.7. 381-Ball caBGA BGA Breakout and Routing Example

This example places an ECP5 FPGA in a 17 mm × 17 mm, 0.8 mm pitch, 381-ball caBGA package (LFE5UM-85FMG381) in a 4-layer stack up with maximum I/O utilization. This example utilizes 4-mil traces and 7-mil via drills for BGA escape routing. Two internal layers are used as reference planes.

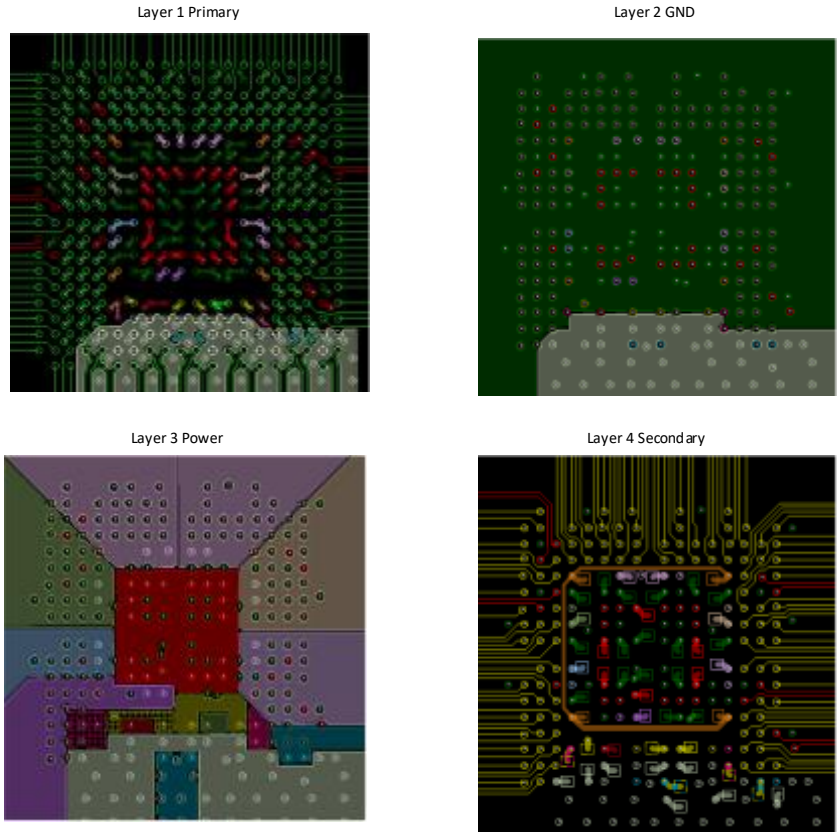


Figure 4.9. CAM Artwork Screen Shots, 381-Ball caBGA

4.1.8. 400-Ball caBGA BGA Breakout Example

This breakout uses a MachXO3 PLD in a 17 mm × 17 mm, 0.80 mm pitch, 400-ball caBGA package (MXO3L-6900-BC400) in a 6-layer stackup with maximum I/O. This example utilizes a 0.10 mm trace width/space and 0.25 mm via drill. Two internal layers are used as reference planes. VCC is tied to a plane while VCCIOs are routed and have decoupling capacitors at secondary layer.

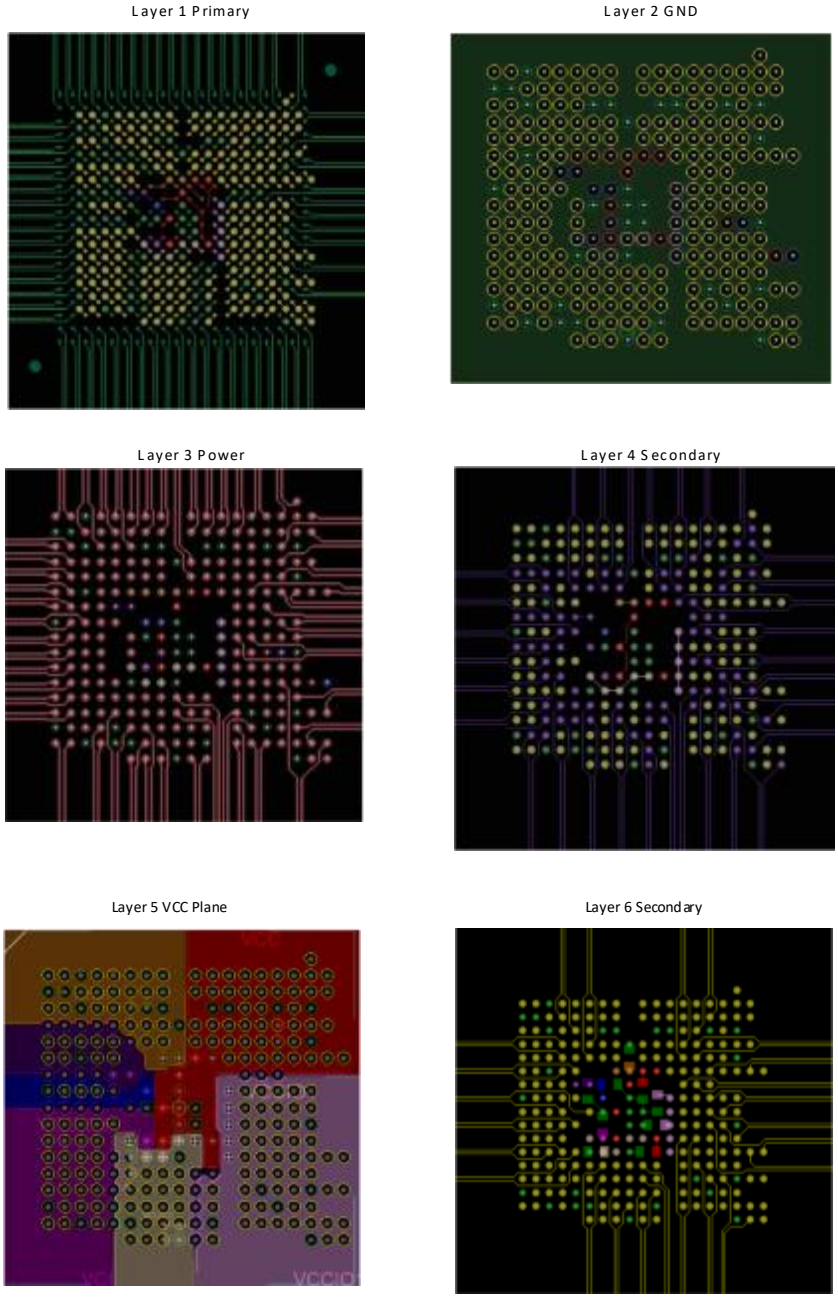


Figure 4.10. Layout Screen Shots, 400-Ball caBGA, 0.80 mm Pitch

4.1.9. 484-Ball caBGA BGA Breakout Example

This breakout uses a MachXO3L 9400C in a 19 mm × 19 mm, 0.8 mm pitch, 484 ball caBGA package (MXO3L-9400CBCG484) in a 6-layer routing. All vias are to be non-conductive epoxy filled. Flat surface at top land. This example utilizes a 0.100 mm trace width/space, escape via pad of 0.400 mm and via drill of 0.254mm. Three metal layers are set as reference planes.

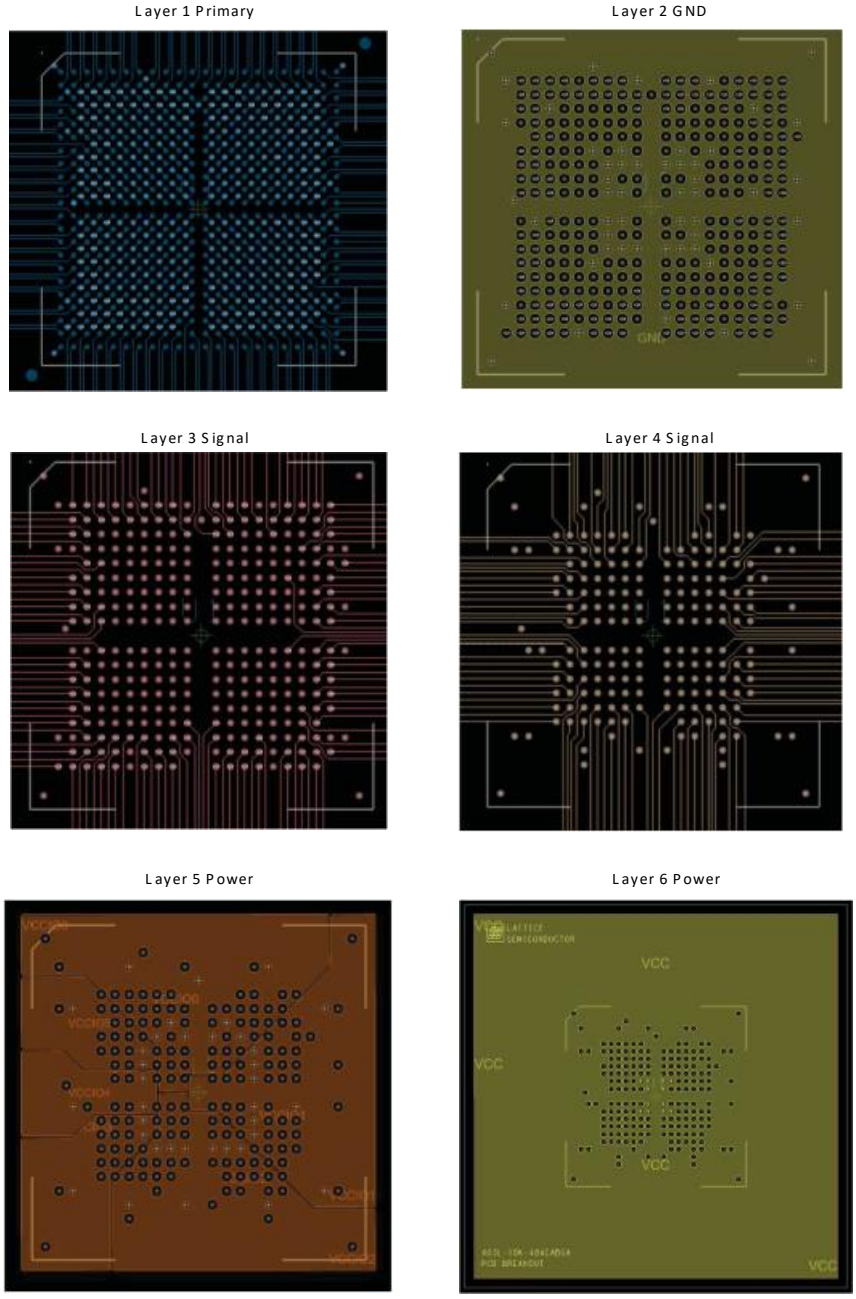


Figure 4.11. Layout Screen Shots, 484-Ball caBGA, 0.80 mm Pitch

4.1.10. 554-Ball caBGA BGA Breakout and Routing Example

This example places an ECP5 FPGA in a 23x23 mm, 0.8 mm pitch, 554-ball caBGA package (LFE5UM-85FMG554) in a 4-layer stack up with maximum I/O utilization. This example utilizes 4-mil traces and 7-mil via drills for BGA escape routing. Two internal layers are used as reference planes.

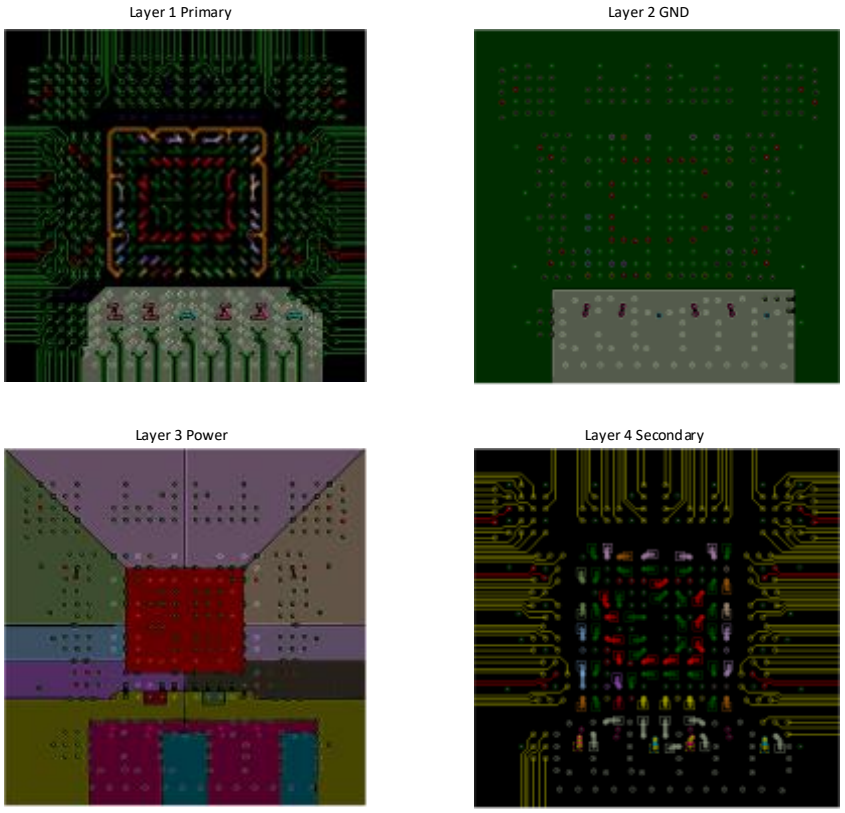


Figure 4.12. Layout Screen Shots, CAM Artwork Screen Shots, 554-Ball caBGA

4.1.11. 756-Ball caBGA BGA Breakout and Routing Example

This example places an ECP5 FPGA in a 27 mm × 27 mm, 0.8 mm pitch, 756-ball caBGA package (LFE5U-85FMG756) in a 4-layer stack up with maximum I/O utilization. This example utilizes 4-mil traces and 7-mil via drills for BGA escape routing. Two internal layers are used as reference planes.

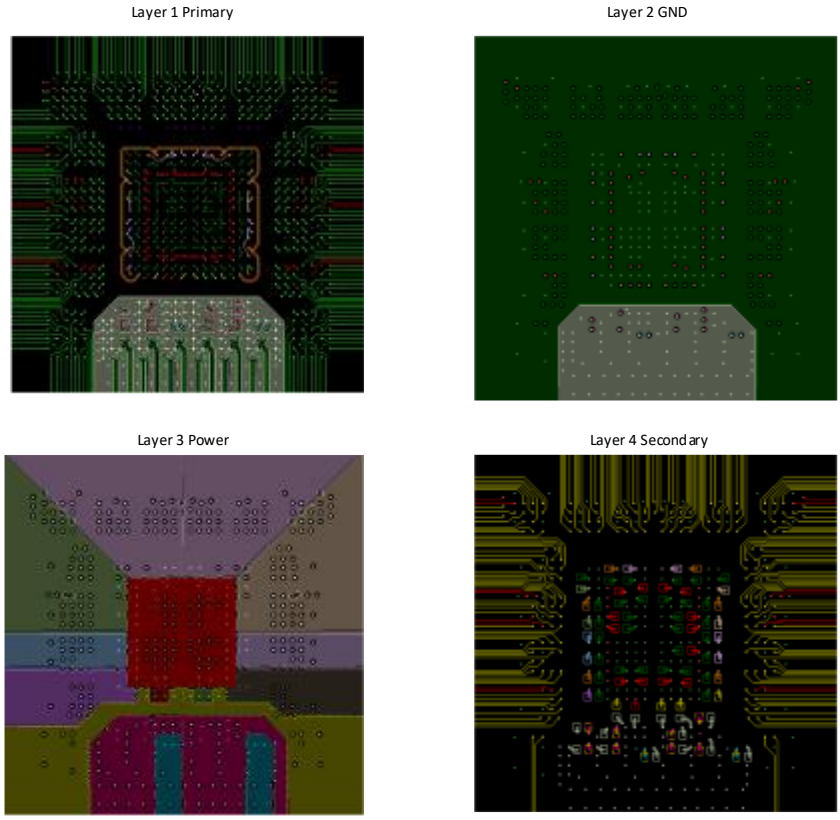


Figure 4.13. CAM Artwork Screen Shots, 756-Ball caBGA

4.2. csBGA BGA Breakout and Routing Examples

4.2.1. 64-Ball csBGA BGA Breakout and Routing Example

This example places an ispMACH 4000ZE CPLD in a 5 mm × 5 mm, 0.5 mm pitch, 64-ball csBGA package (LC4064ZE-MN64) in a 6-layer stack up with maximum I/O utilization.

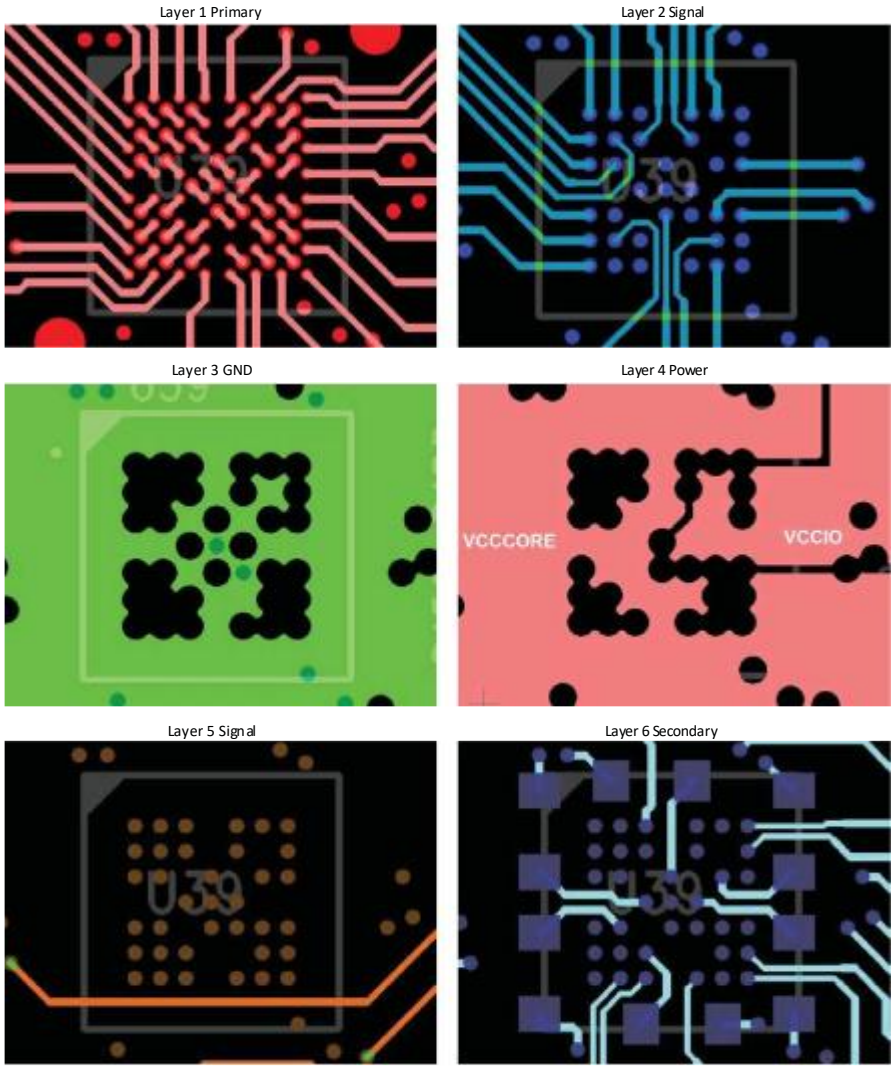


Figure 4.14. CAM Artwork Screen Shots 64-Ball csBGA

4.2.2. 100-Ball csBGA BGA Breakout and Routing Examples

These examples place a MachXO PLD in a 8 mm × 8 mm, 0.5 mm pitch, 100-ball csBGA package (LCMXO640-M132/MN132) into two fabrication scenarios. Both examples utilize a 4-layer stack-up. The first example uses 0.085 mm trace and 0.085 mm space design rules for maximum I/O accessibility; while the second example uses 0.100 mm trace and 0.100 mm space design rules and provides 15% less I/O.

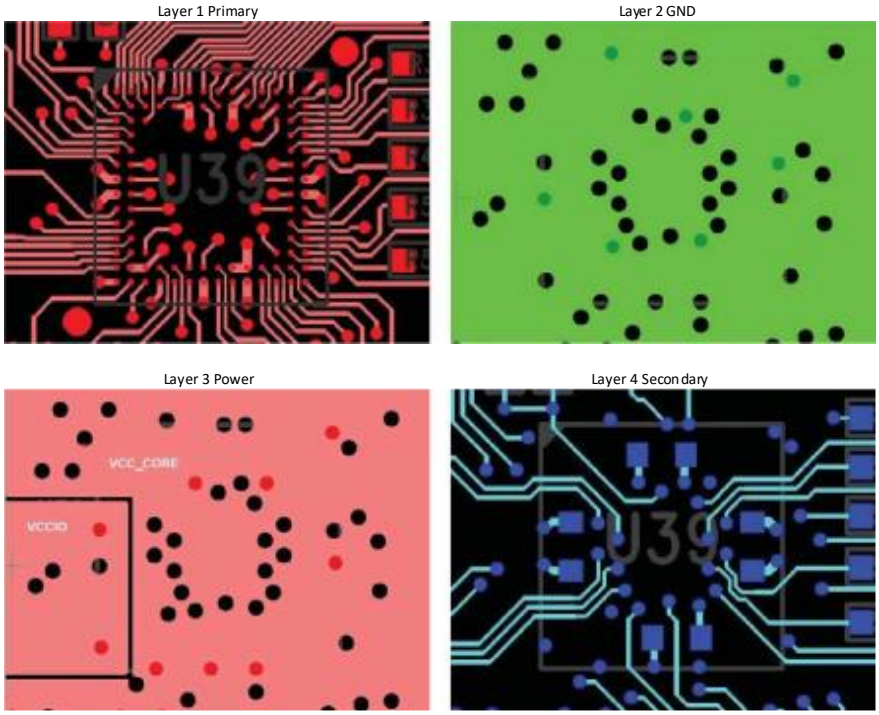


Figure 4.15. CAM Artwork Screen Shots, Example #1, 100-Ball csBGA

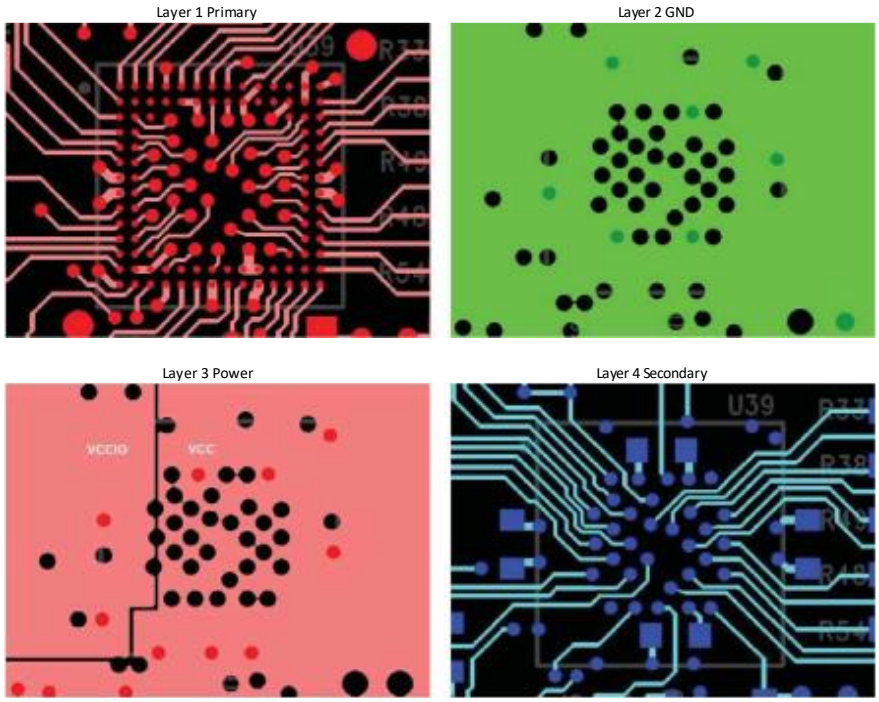


Figure 4.16. CAM Artwork Screen Shots, Example #2, 100-Ball csBGA

4.2.3. 132-Ball csBGA BGA Breakout Examples

These examples place a MachXO PLD in a 8 mm × 8 mm, 0.5 mm pitch, 132-ball csBGA package (LCMXO640-M132/MN132) into two fabrication scenarios. Both examples utilize a 4-layer stack-up. The first example uses 0.085 mm trace and 0.085 mm space design rules for maximum I/O accessibility; while the second example uses 0.100 mm trace and 0.100 mm space design rules and provides 15% less I/O.

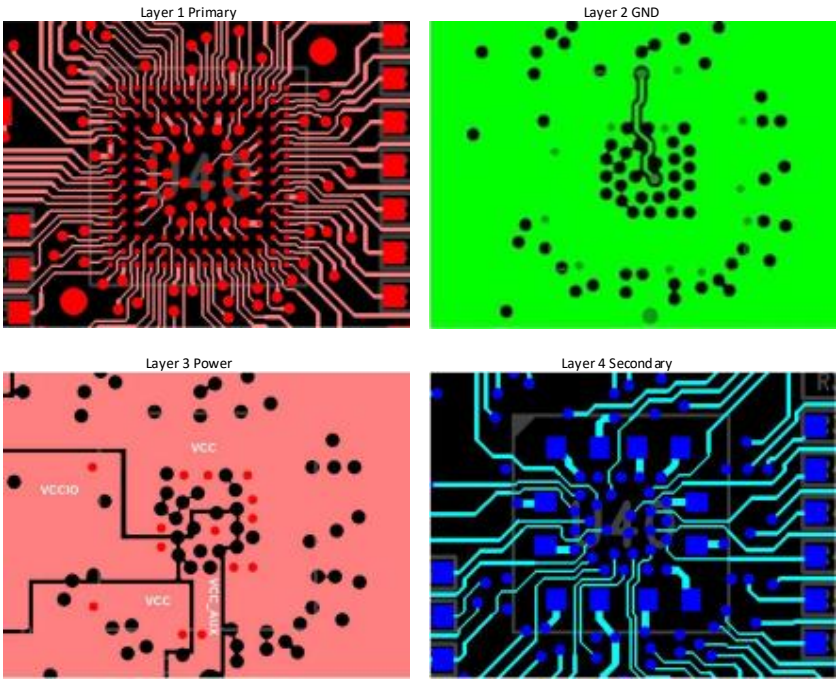


Figure 4.17. CAM Artwork Screen Shots, Example #1, 132-Ball csBGA

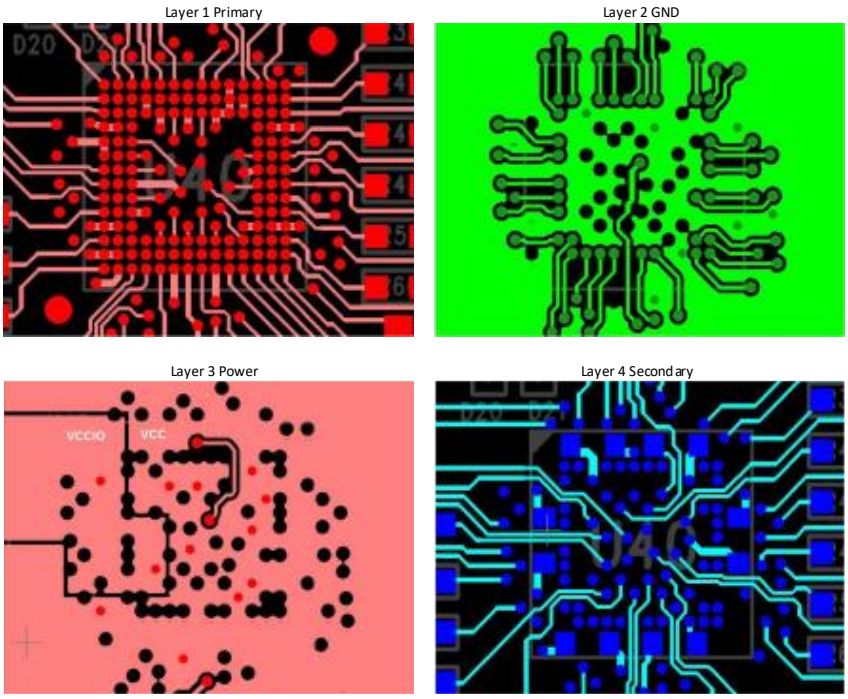


Figure 4.18. CAM Artwork Screen Shots, Example #2, 132-Ball csBGA

4.2.4. 144-Ball csBGA BGA Breakout Examples

These examples place an ispMACH 4000ZE in a 7 mm × 7 mm, 0.5 mm pitch, 144-ball csBGA package (LC4256ZE-MN144) into two fabrication scenarios. One for a 6-layer stack up with maximum I/O utilization and a 4-layer with about 5% fewer I/O. The 6-layer (Example #1) design avoids uses of micro vias and takes advantage of removed pads on inner layers to route all pins out to 6 layers with good layer structure for high-speed signal integrity.

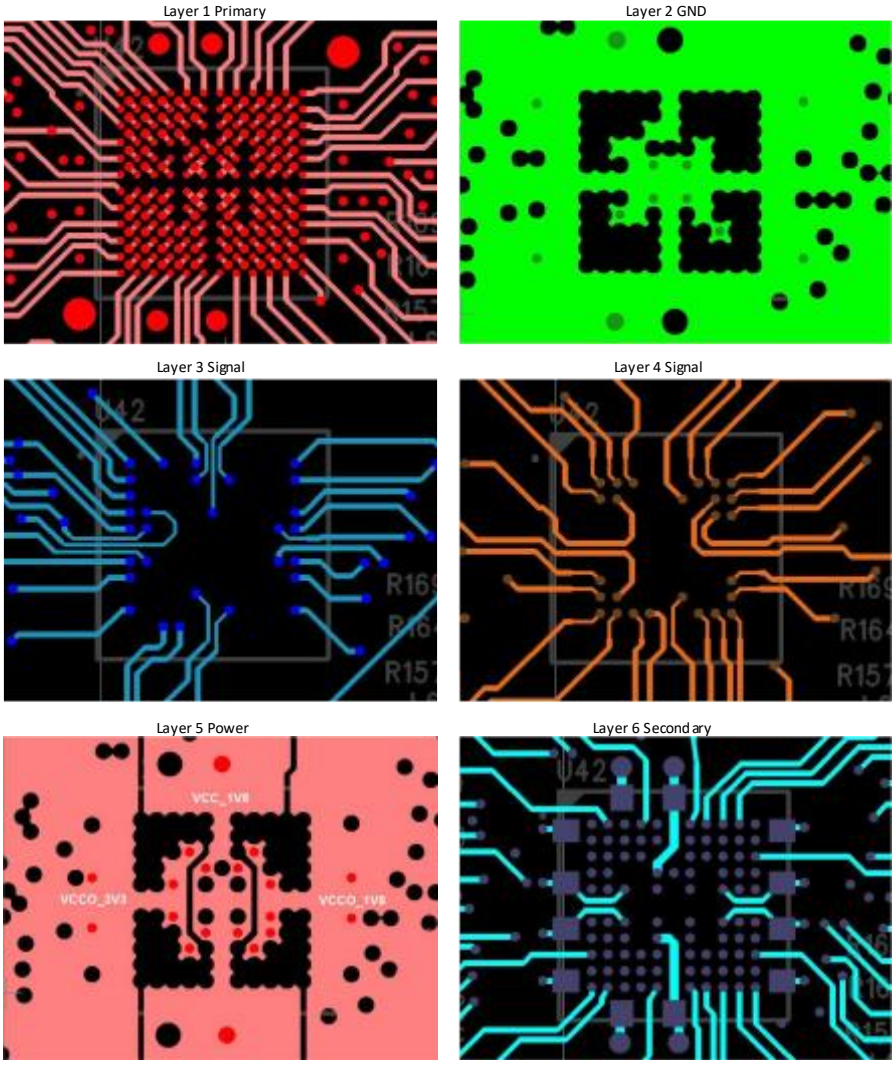


Figure 4.19. CAM Artwork Screen Shots, Example #1, 144-Ball csBGA

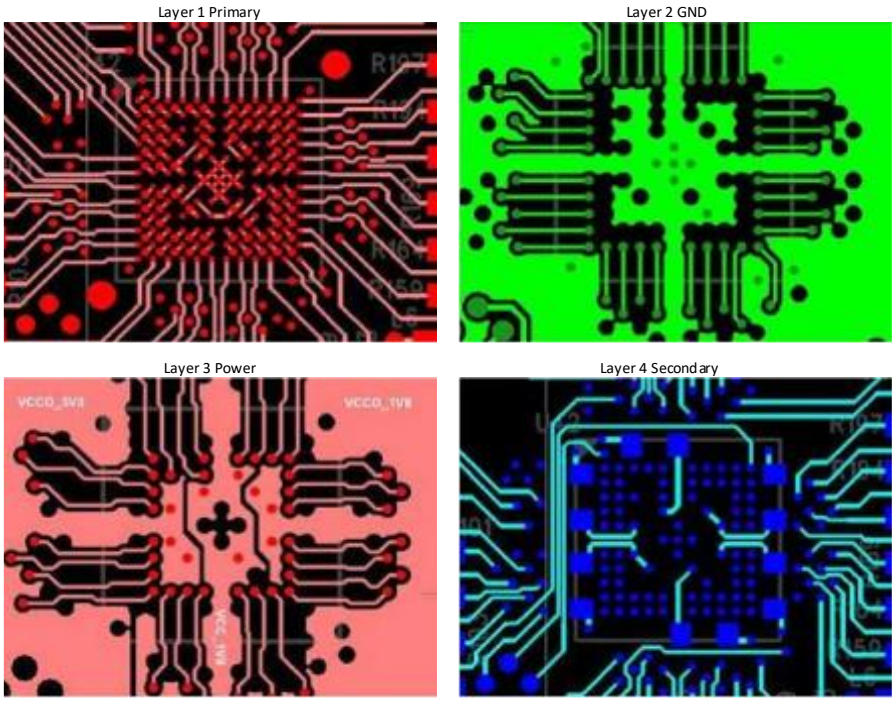


Figure 4.20. CAM Artwork Screen Shots, Example #2, 144-Ball csBGA

4.2.5. 328-Ball csBGA BGA Breakout and Routing Example

This example places a LatticeECP3-17 FPGA in a 10 mm × 10 mm, 0.5 mm pitch, 328-ball csBGA package (LFE3-17EA-MG328) in a 6-layer stack up with maximum I/O utilization. This example utilizes a 3-mil trace neck down and 5-mil via for BGA escape routing. Layers have been set to use as reference planes for high-speed signal traces.

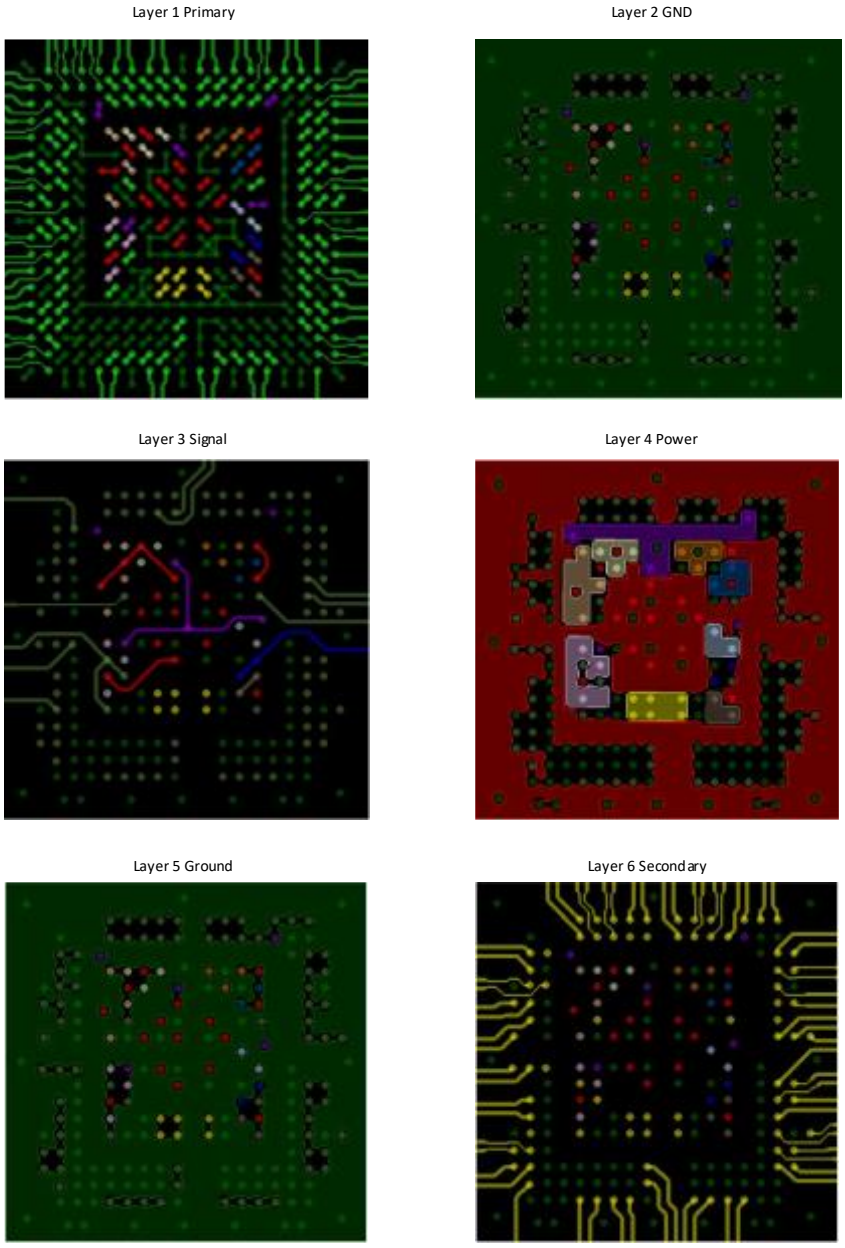


Figure 4.21. CAM Artwork Screen Shots, 328-Ball csBGA

4.3. ckfBGA/ctfBGA BGA Breakout Example

4.3.1. 80-Ball ckfBGA/ctfBGA BGA Breakout Example

This breakout uses an LIF-MD6000 PLD in a 7.0 mm × 7.0 mm (ckfBGA) and 6.5 mm × 6.5 mm (ctfBGA), 0.65 mm pitch, 80-ball ckfBGA/ctfBGA package (LIF-MD6000-6JMG80) in a 4-layer routing using via-in-pad technology. All vias are to be non-conductive epoxy filled. Flat surface at top land. This example utilizes a 0.127 mm trace width/space, escape via pad of 0.400 mm and via drill of 0.150 mm. Two internal layers are set as reference planes.

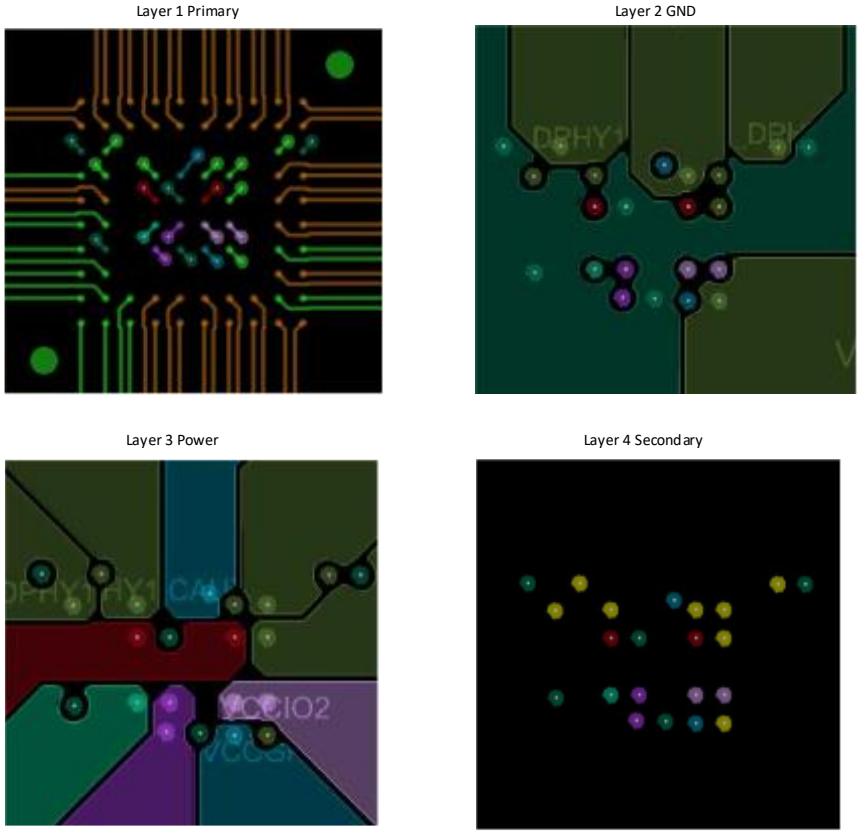


Figure 4.22. Layout Screen Shots, 80-Ball ctfBGA, 0.65 mm Pitch

4.4. csfBGA BGA Breakout Examples

4.4.1. 81-Ball csfBGA BGA Breakout Example

This breakout uses an LIF-MD6000 PLD in a 4.5 mm × 4.5 mm, 0.5 mm pitch, 81-ball csfBGA package (LIF-MD6000-6FMG81) in a 4-layer routing using via-in-pad technology. All vias are to be non-conductive epoxy filled. Flat surface at top land. This example utilizes a 0.076 mm trace width/space, escape via pad of 0.254 mm and via drill of 0.102 mm. Two internal layers are set as reference planes.

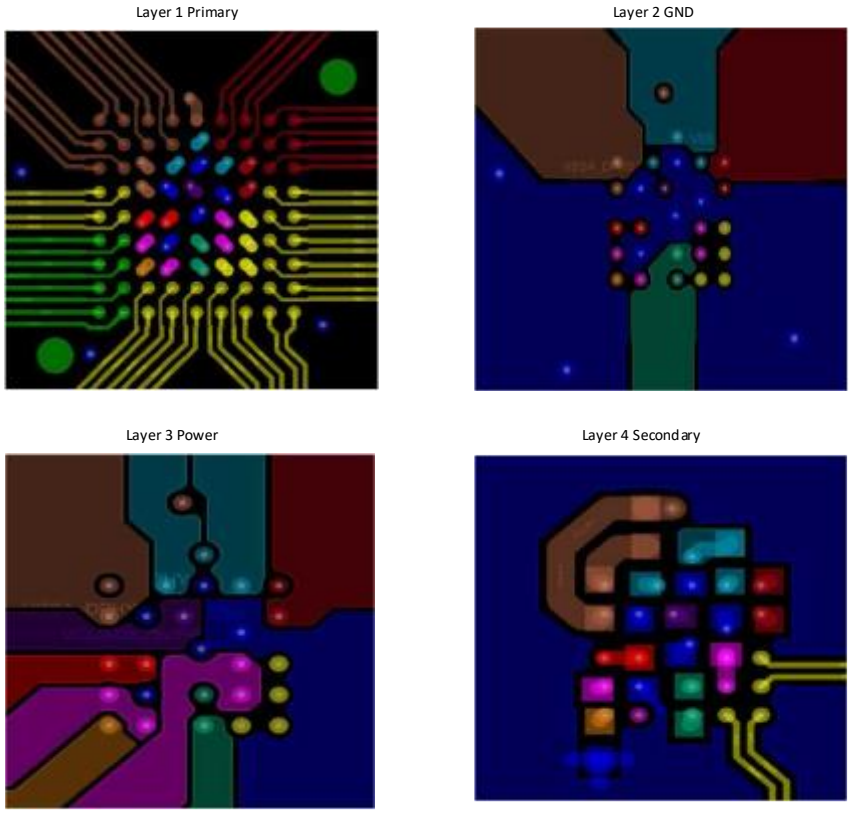


Figure 4.23. Layout Screen Shots, 81-Ball csfBGA, 0.50 mm Pitch

4.4.2. 121-Ball csfBGA BGA Breakout Example

This breakout uses an MXO3 PLD in a 6 mm × 6 mm, 0.50 mm pitch, 121-ball csfBGA package (MXO3L-6900-MG121) in a 6-layer stackup with maximum I/O. This example utilizes a through microvia technology of 0.10 mm via drill. Trace width/space used is 0.10 mm. Two internal layers are used as reference planes for GND and PWR.

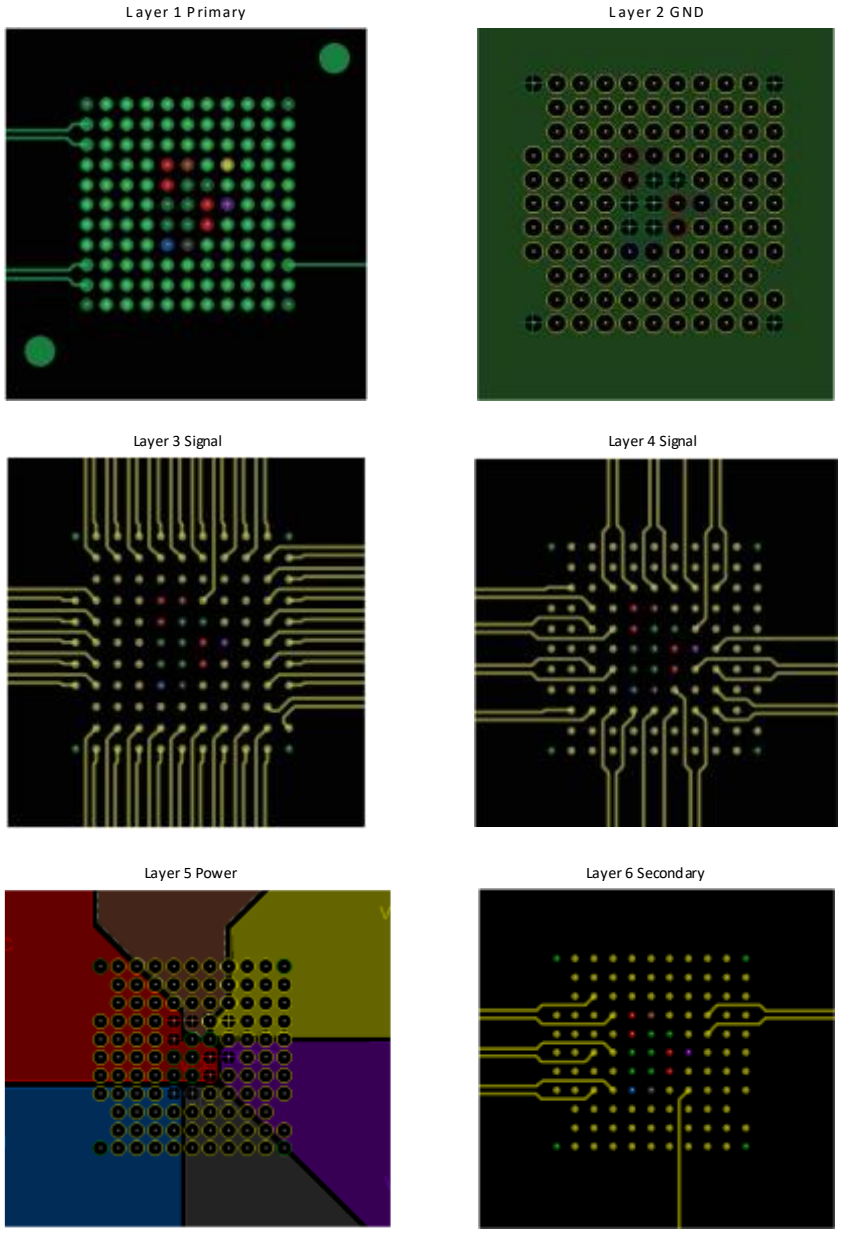


Figure 4.24. Layout Screen Shots, 121-Ball csfBGA, 0.50 mm Pitch

4.4.3. 256-Ball csfBGA BGA Breakout Example

This breakout uses a MXO3 PLD in a 9 mm × 9 mm, 0.50 mm pitch, 256-ball csfBGA package (MXO3L-6900-MG256) in a 6-layer stackup with maximum I/O. This example utilizes a blind microvia technology of 0.10 mm via drill. Trace width/space used is 0.10 mm. Two internal layers are used as reference planes for GND and PWR.

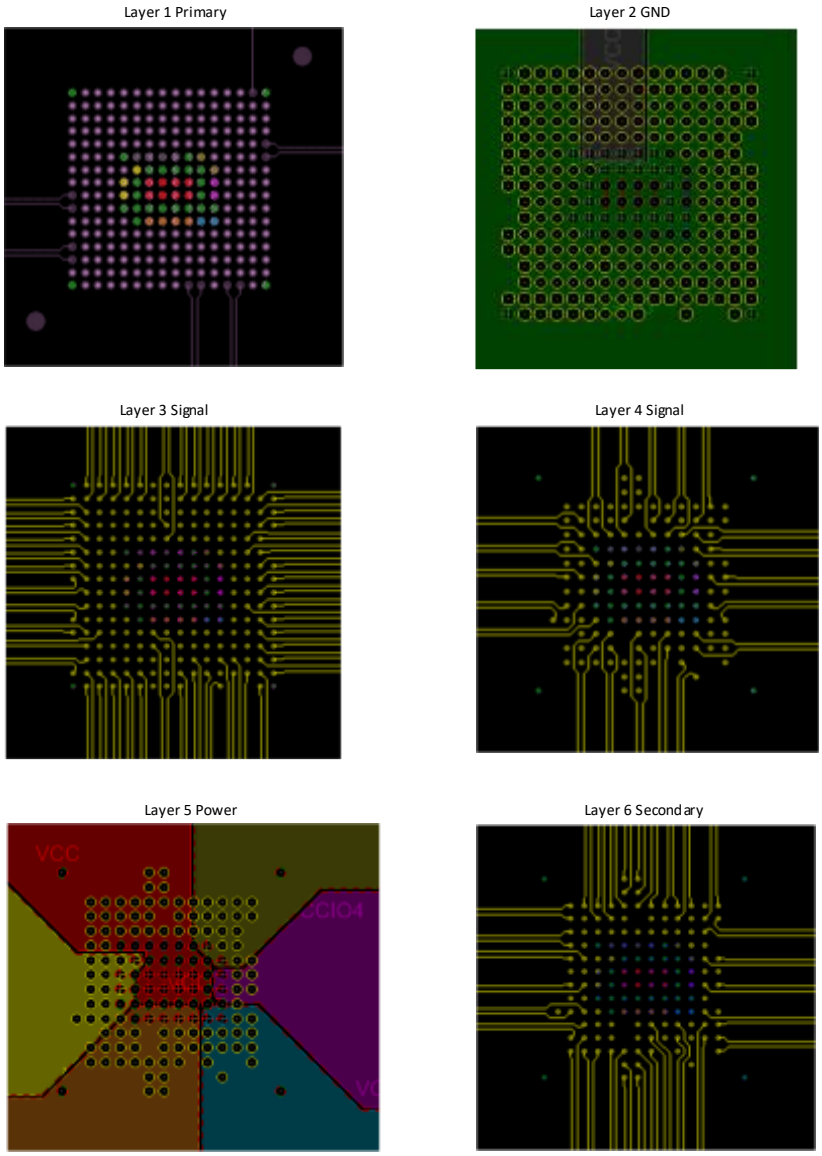


Figure 4.25. Layout Screen Shots, 256-Ball csfBGA, 0.50 mm Pitch

4.4.4. 285-Ball csfBGA BGA Breakout and Routing Example

This example places an ECP5™ FPGA in a 10 mm × 10 mm, 0.5 mm pitch, 285-ball csfBGA package (LFE5UM-25F-MG285) in a 4-layer stack up with maximum I/O utilization. This example utilizes 4-mil traces and 4-mil via drills for BGA escape routing. Two internal layers are used as reference planes. Blind and buried vias are not necessary in this example. Decoupling 0402 capacitors are placed at secondary layer for VCC and VCCIOs.

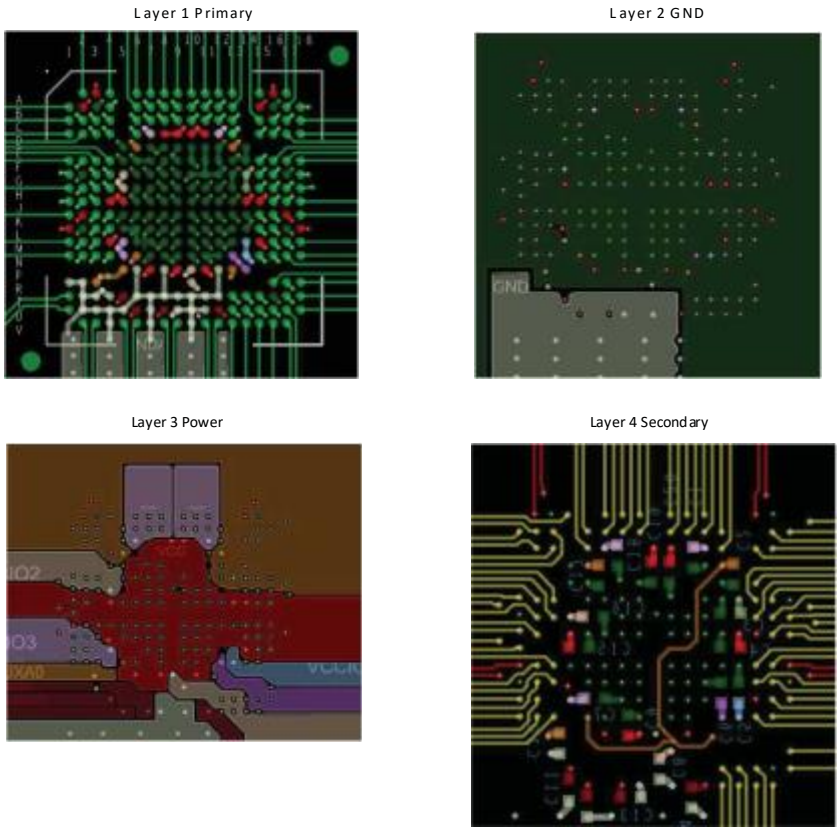


Figure 4.26. CAM Artwork Screen Shots, 285-Ball csfBGA

4.4.5. 289-Ball csBGA BGA Breakout Example

This breakout uses a Crosslink™-NX in a 9.5 mm × 9.5 mm, 0.50 mm pitch, 289-ball csBGA package (JE5D30-BGA289) in a 6-layer stackup with maximum I/O. This example utilizes a 0.10 mm trace width/space and 0.20 mm via drill. Two internal layers are used as reference planes for GND and PWR.

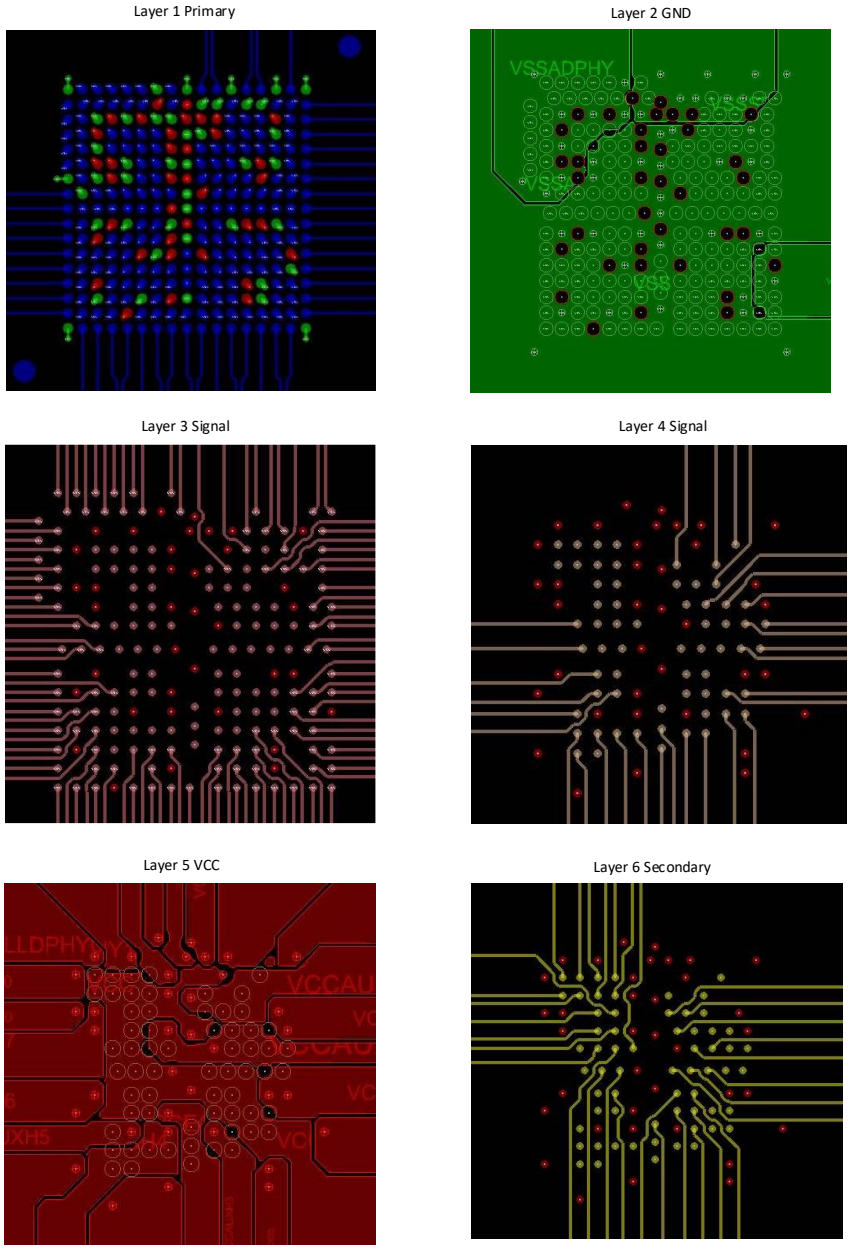


Figure 4.27. Layout Screen Shots, 289-Ball csfBGA, 0.50 mm Pitch

4.4.6. 324-Ball csfBGA BGA Breakout Example

This breakout uses a MachXO3 PLD in a 10 mm × 10 mm, 0.50 mm pitch, 324-ball csfBGA package (MXO3L-6900-MG324) in a 6-layer stackup with maximum I/O. This example utilizes a blind microvia technology of 0.10 mm via drill. Trace width/space used is 0.10 mm. Two internal layers are used as reference planes for GND and PWR.

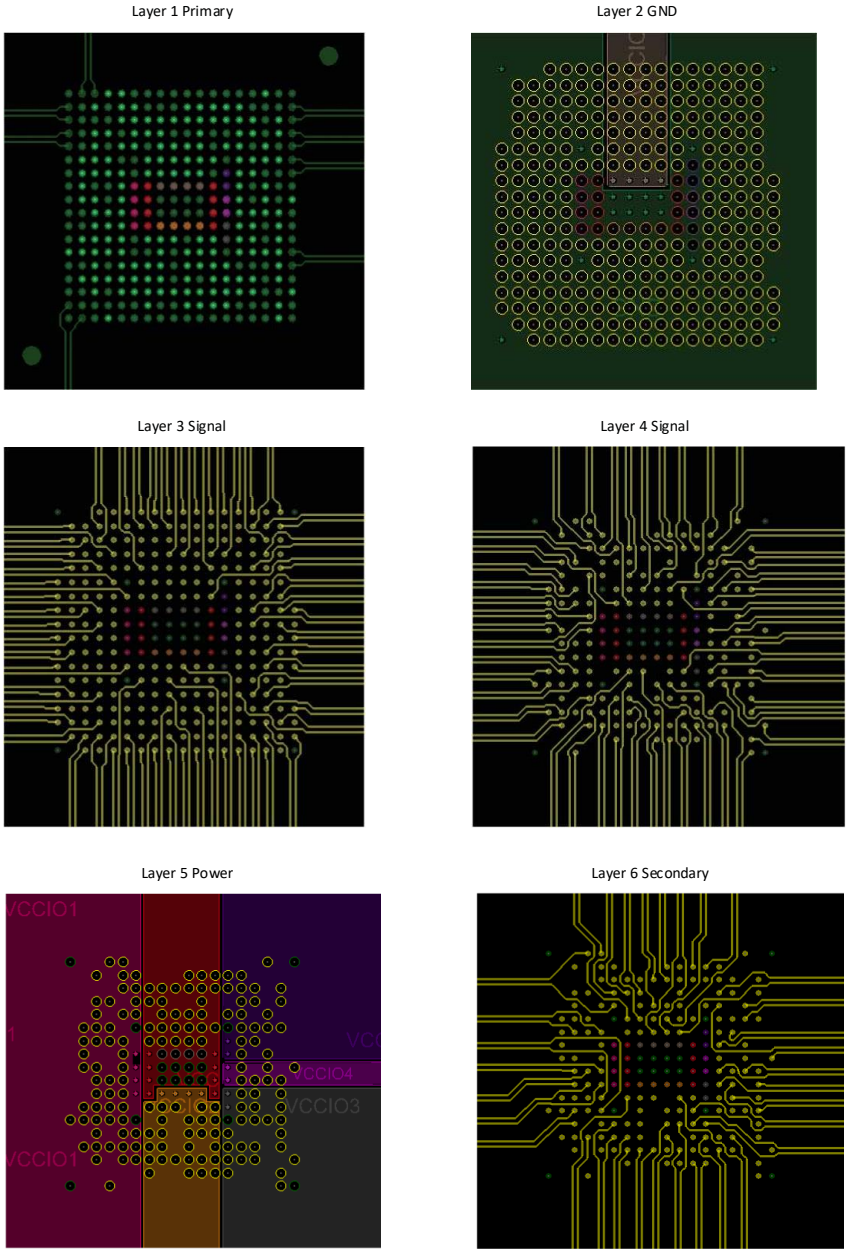


Figure 4.28. Layout Screen Shots, 324-Ball csfBGA, 0.50 mm Pitch

4.5. fcBGA BGA Breakout Example

4.5.1. 672-Ball fcBGA Breakout Example

This breakout uses a CertusPro-NX in a 27 mm × 27 mm, 1.00 mm pitch, 672-ball FCBGA package (LFCPNX-100-LFG672) in a 6-layer stackup with maximum I/O. This example utilizes a 0.101 mm trace width/space; via pad size is 0.20 mm with 0.10 via drill. Two internal layers are used as reference planes for GND and PWR.

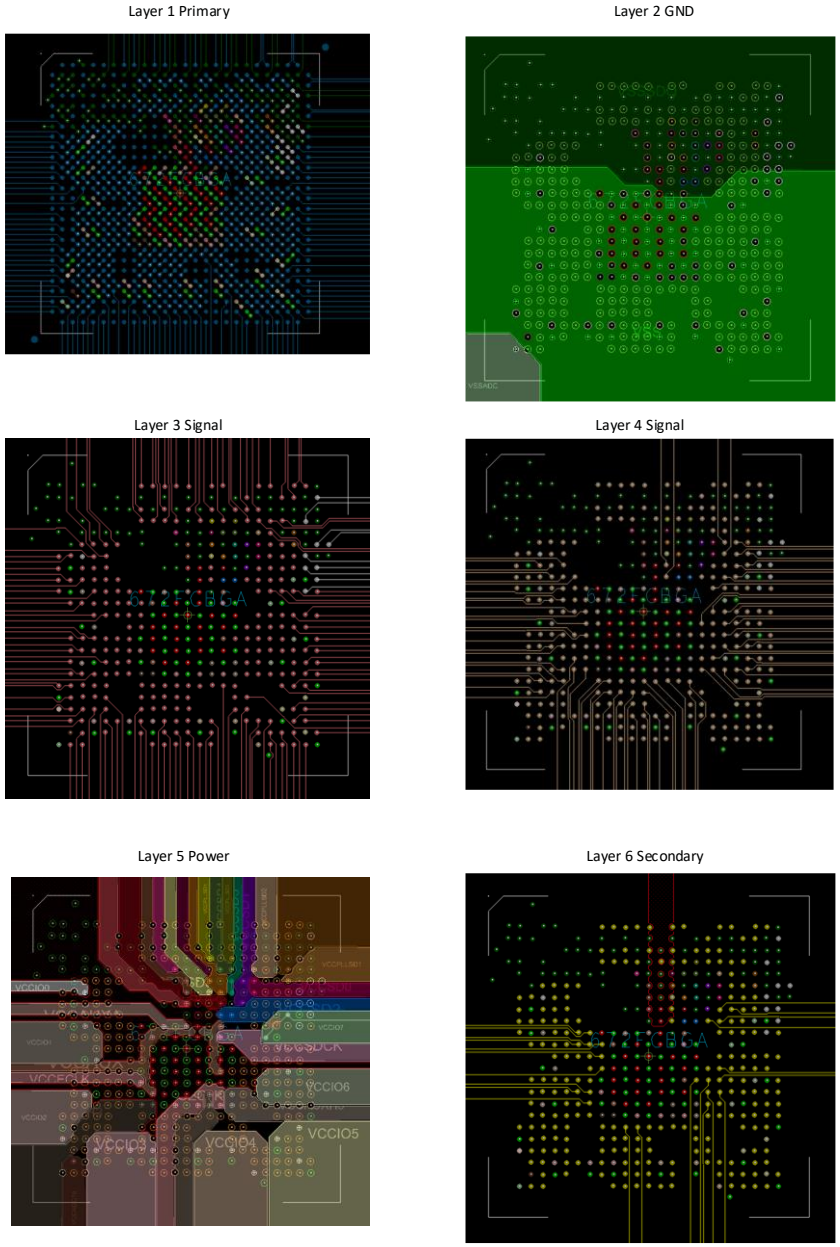
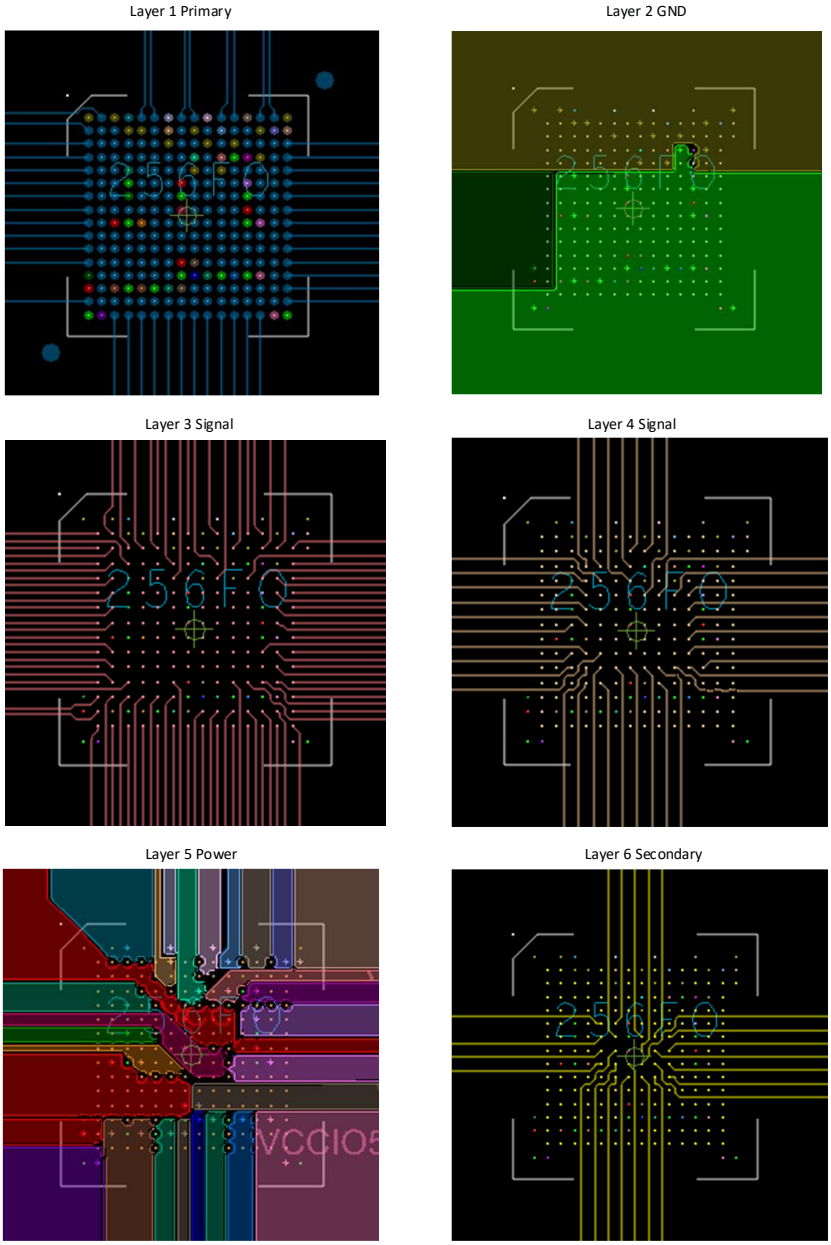


Figure 4.29. Layout Screen Shots, 672-Ball fcBGA, 1.00 mm Pitch

4.6. FOWLCSP BGA Breakout Example

4.6.1. 256-Ball FOWLCSP Breakout Example

This breakout uses a CertusPro-NX in a 9 mm × 9 mm, 0.50 mm pitch, 256-ball fan-out WLCSP package (LFCPNX-100-ASG256) in a 6-layer stackup with maximum I/O. This example utilizes a 0.10 mm trace width/space; via pad size is 0.20 mm with 0.10 via drill. Two internal layers are used as reference planes for GND and PWR.



4.7. ftBGA BGA Breakout Example

4.7.1. 237-Ball ftBGA BGA Breakout Example

This breakout uses an LPTM21 PLD in a 17 mm × 17 mm, 1.00 mm pitch, 237-ball ftBGA package (LPTM21-237ftBGA) in a 4-layer stackup with maximum I/O. This example utilizes a 0.254 mm trace width/space; via pad size is 0.45 mm with 0.25 via drill. Two internal layers are used as reference planes for GND and PWR.

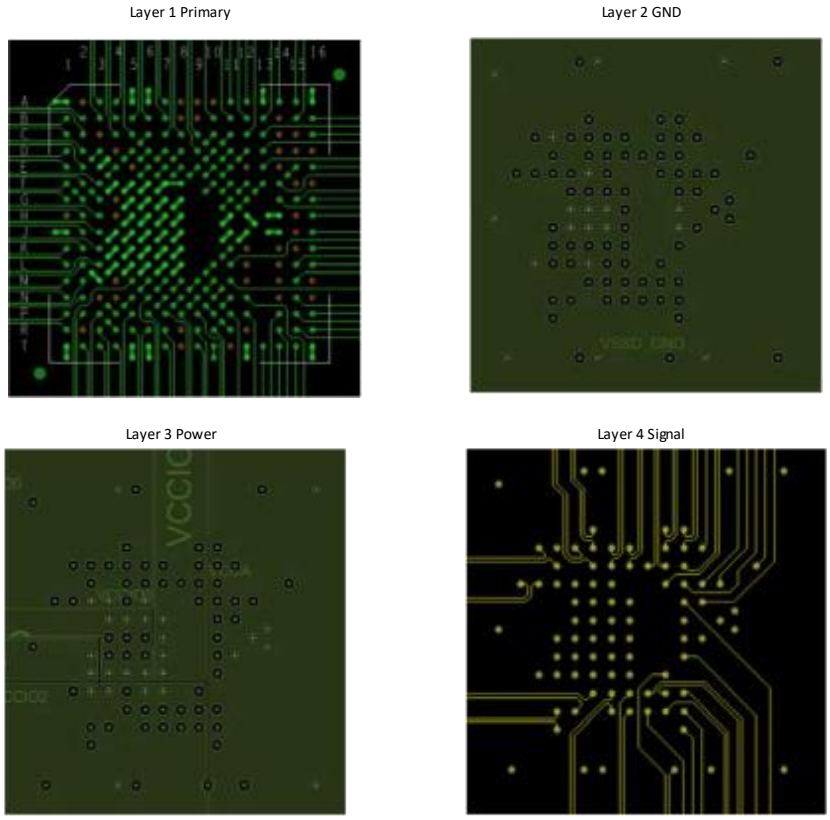


Figure 4.30. Layout Screen Shots, 237-Ball ftBGA, 1.00 mm Pitch

4.8. ucBGA BGA Breakout and Routing Examples

4.8.1. 64-Ball ucBGA BGA Breakout and Routing Example

This example places an ispMACH 4000ZE CPLD in a 4 mm × 4 mm, 0.4 mm pitch, 64-ball ucBGA package (LC4064ZE-UMN64) in a 6-layer stack up with maximum I/O utilization. This example demonstrates a modified dogbone fanout technique to get access to all pins yet limiting number of layers and via schedules, while setting up layers to use reference planes for high-speed signal traces.

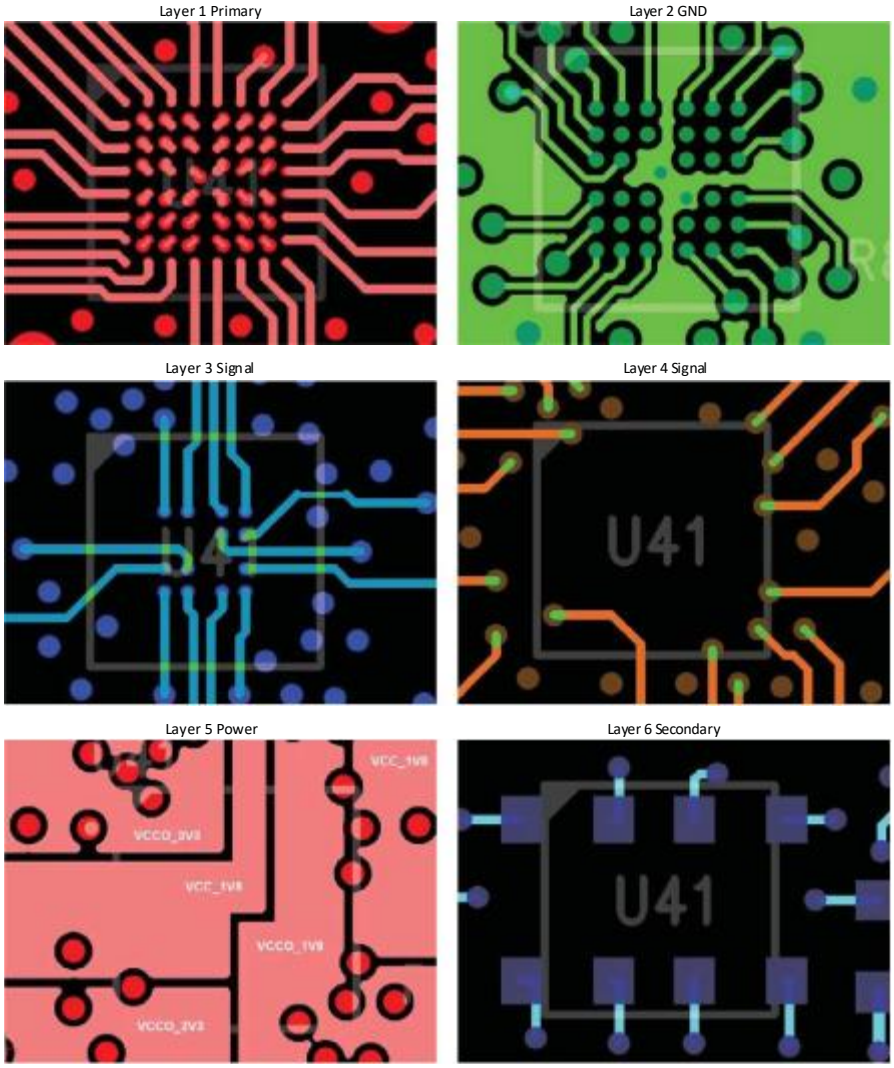


Figure 4.31. CAM Artwork Screen Shots 64-Ball ucBGA

4.8.2. 64-Ball ucfBGA BGA Breakout and Routing Example

This breakout uses an LIF-MD6000 CrossLink PLD in a 3.5 mm × 3.5 mm, 0.4 mm pitch, 64-ball ucfBGA package (LIF-MD6000-6UFG64) in a 6-layer routing using via-in-pad technology. All vias are to be non-conductive epoxy filled. Flat surface at top land. This example utilizes a 0.127/0.089 mm trace width/space, escape via pad of 0.254 mm and via drill of 0.127 mm.

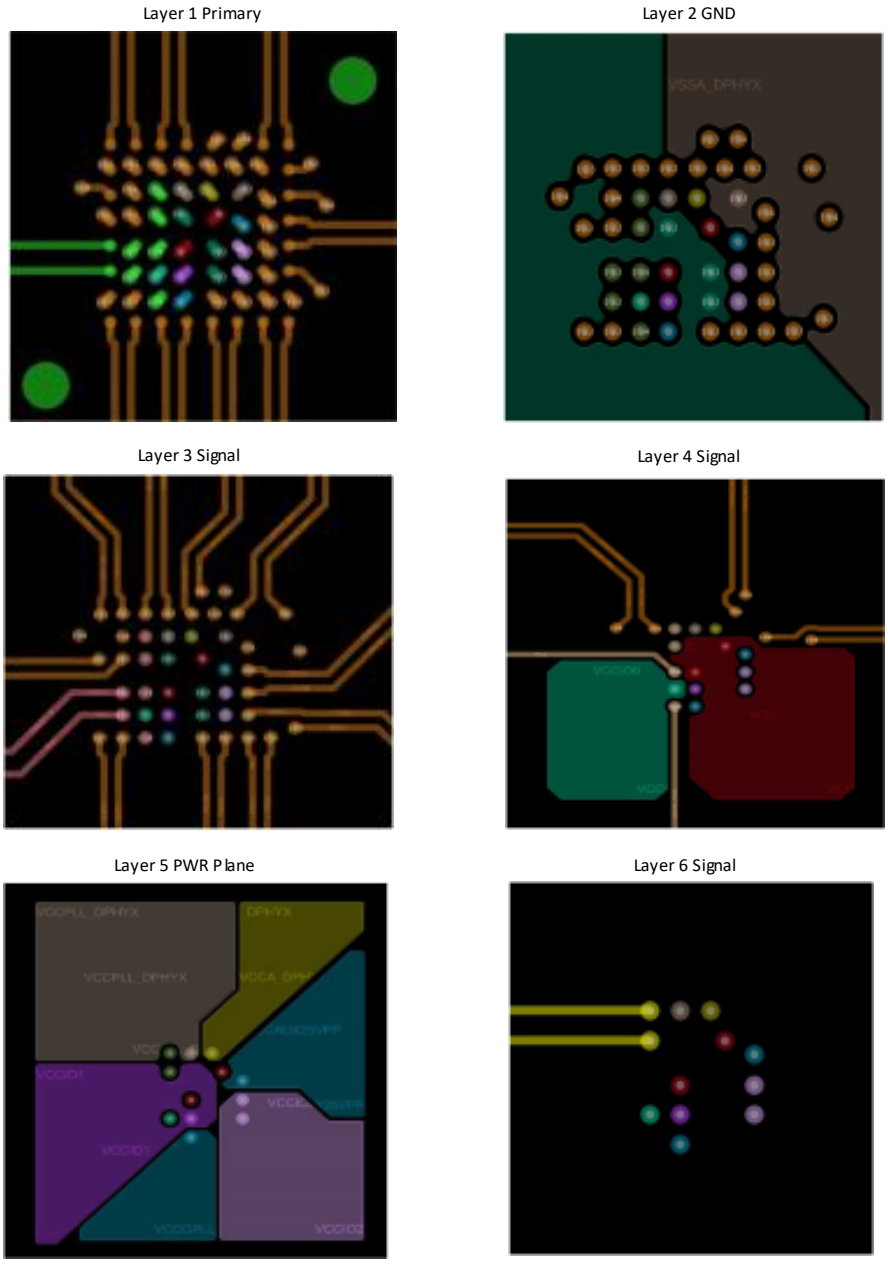


Figure 4.32. Layout Screen Shots, 64-Ball ucfBGA, 0.4 mm Pitch

4.9. WLCSP Breakout Examples

4.9.1. 16-Bump WLCSP Breakout Example

This WLCSP breakout example uses an iCE40LP device in a 1.40 mm × 1.48 mm, 0.35 mm pitch, 16-bump WLCSP package (iCE40LPXX-SWG16) in a 4-layer routing using via-in-pad technology. Four via-in-pads are to be non-conductive epoxy filled and planarized. This example utilizes a 0.10 mm trace width/space, escape via land of 0.20 mm and via drill of 0.10 mm. Two internal layers are set as reference planes.

The above recommendations for trace width/space, via drill and pad are also applicable to iCE40 UltraLite device (1.409 mm × 1.409 mm, 0.35 mm pitch, 16-Bump WLCSP package, iCE40ULXX-SWG16.)

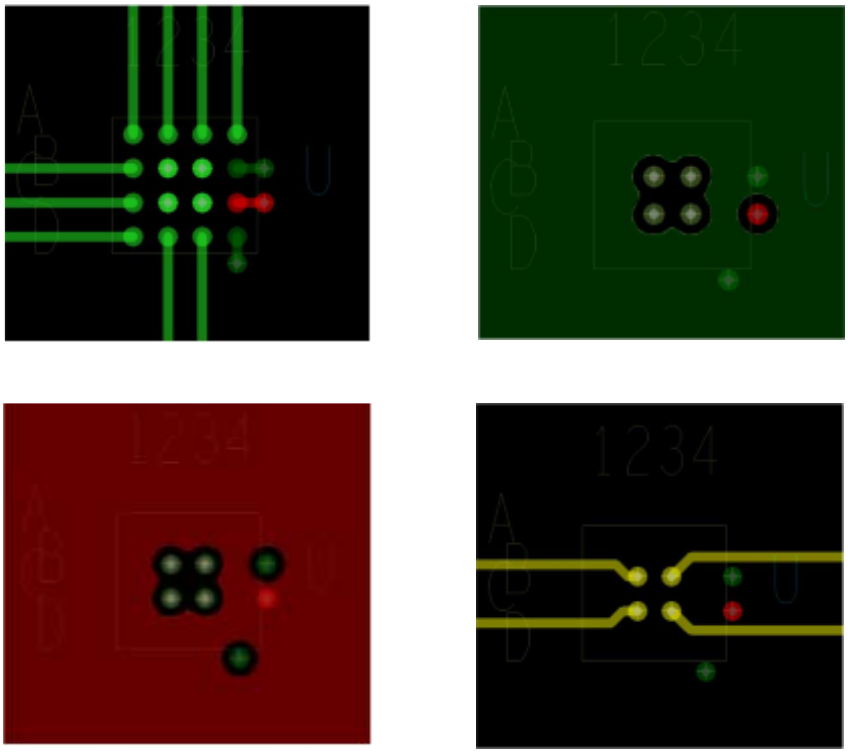


Figure 4.33. CAM Artwork Screen Shots for iCE40LP Device, 16-Bump WLCSP

4.9.2. 25-Bump WLCSP Breakout and Routing Example 1

This WLCSP breakout and routing examples use two different package pitches. Example #1 uses an iCE40LM4K PLD in a 1.7 mm × 1.7 mm, 0.35 mm pitch, 25-bump WLCSP package (iCE40LM4K-SWG25) in a 4-layer routing using via-in-pad technology. Nine via-in-pads are to be non-conductive epoxy filled and planarized. This example utilizes a 0.10 mm trace width/space, neck trace width and space of 0.05 mm. Escape via land of 0.20 mm and via drill of 0.10 mm. Two internal layers are set as reference planes.

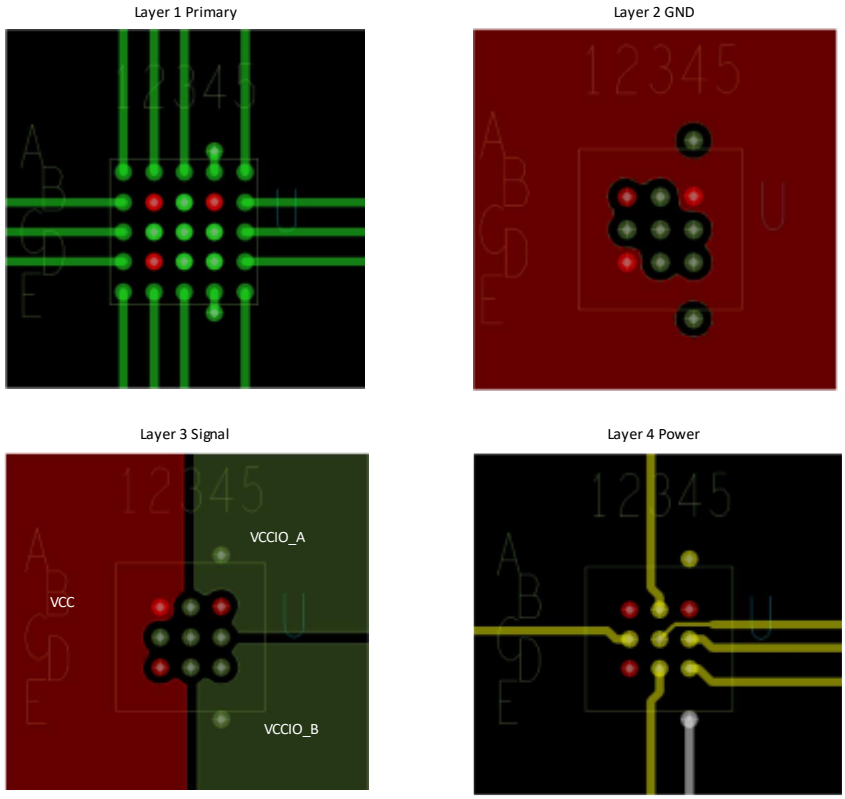


Figure 4.34. CAM Artwork Screen Shots, Example #1 25-Bump WLCSP, 0.35 mm Pitch

4.9.3. 25-Bump WLCSP Breakout and Routing Example 2

Example #2 uses a MachXO2 PLD in a 2.5 mm × 2.5 mm, 0.40 mm pitch, 25-bump WLCSP package (ICE40LM4KSWG25) in a 4-layer routing using via-in-pad technology. All eleven via-in-pads are to be non-conductive epoxy filled and planarized. This example utilizes a 0.12 mm trace width/space, escape via land of 0.25 mm and via drill of 0.12 mm. Two internal layers are set as reference planes.

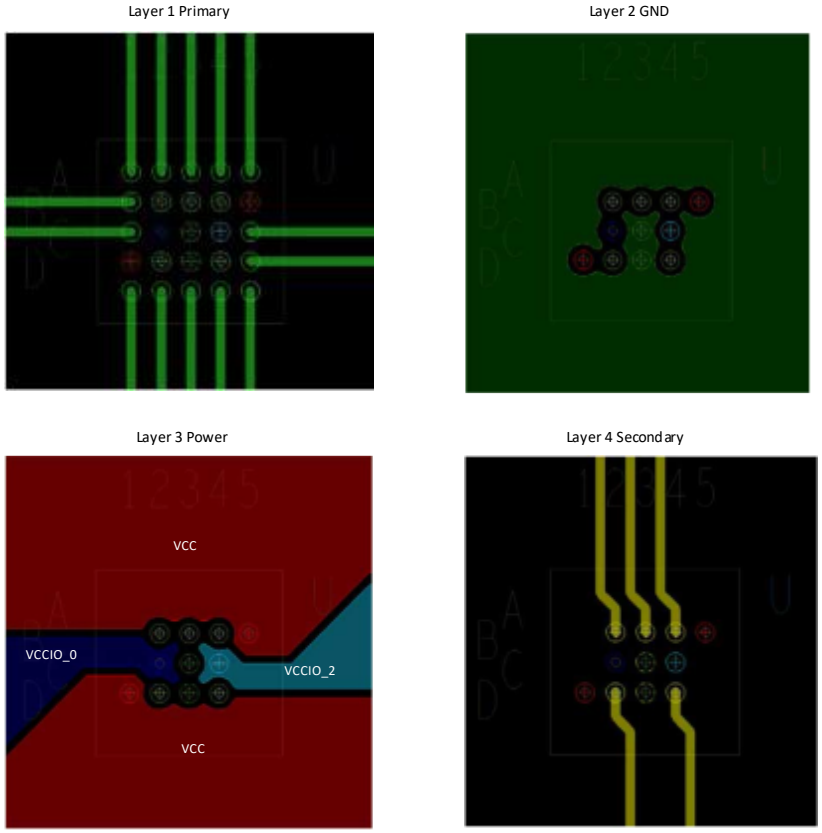


Figure 4.35. CAM Artwork Screen Shots, Example #2 25-Bump WLCSP, 0.4 mm Pitch

4.9.4. 30-Ball WLCSP Breakout and Routing Example

This breakout uses an iCE40UP5K PLD in a 2.11 mm × 2.537 mm, 0.40 mm pitch, 30-ball WLCS package (iCE40UP5K-UWG30) in a 4-layer routing using via-in-pad technology. Seventeen vias are to be non-conductive epoxy filled and planarized. This example utilizes a 0.100 mm trace width/space, escape via pad of 0.200 mm and via drill of 0.100 mm. Two internal layers are set as reference planes.

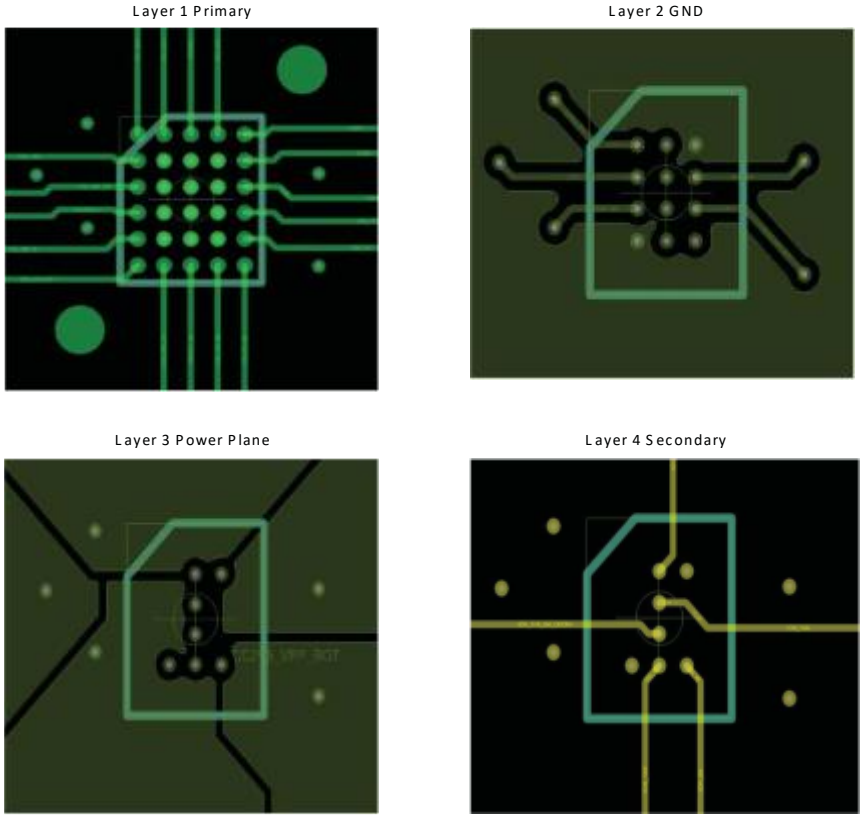


Figure 4.36. Layout Screen Shots, 30-Ball WLCSP, 0.40 mm Pitch

4.9.5. 36-Bump WLCSP Breakout Example 1

This breakout uses a MachXO3 PLD in a 2.487 mm × 2.541 mm, 0.40 mm pitch, 36-bump WLCSP package (MXO3L-1300E-UWG36) with two different routing options. Example1: in a 4-layer routing using through microvia technology. Twenty-five via-in-pads are to be non-conductive epoxy filled and planarized. This example utilizes a 0.07 mm trace width and 0.05 space, escape via land of 0.20 mm and via drill of 0.10 mm. Two internal layers are set as signal layer and a reference plane.

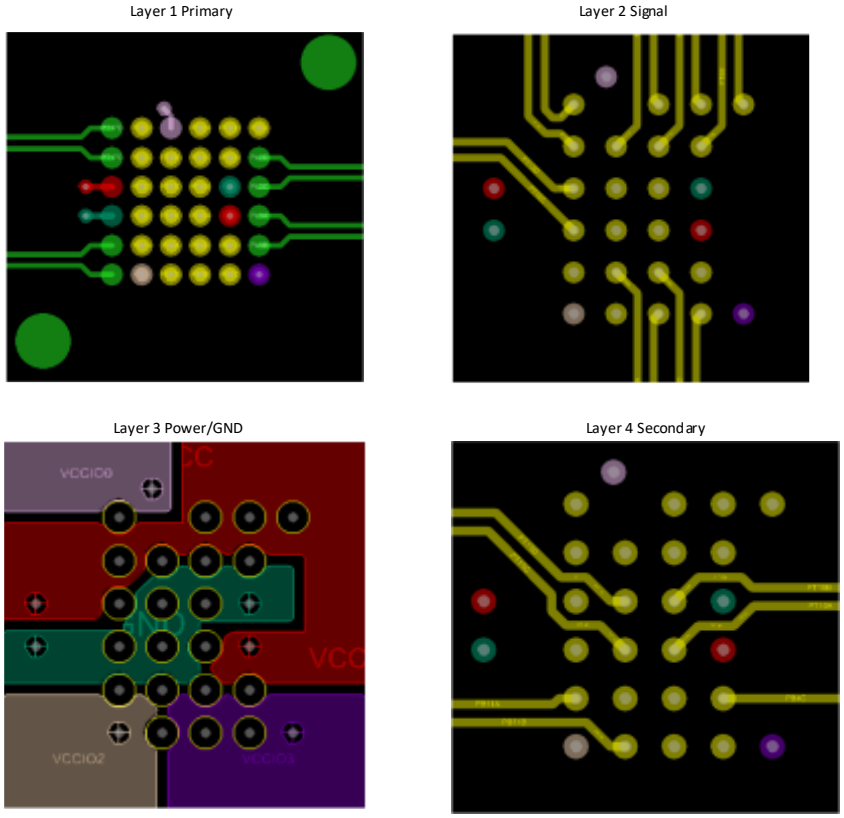


Figure 4.37. Layout Screen Shots, Example #1 36-Bump WLCSP, 0.40 mm Pitch

4.9.6. 36-Bump WLCSP Breakout Example 2

Example 2 is also in a 4-layer routing using blind vias, microvia technology. Twenty-three via-in-pads are to be non-conductive epoxy filled and planarized. This example utilizes a 0.10 mm trace width/space and neck down width/space of 0.07 mm. Escape via land of 0.20 mm and via drill of 0.10 mm. Two internal layers are set as signal layer and a reference plane.

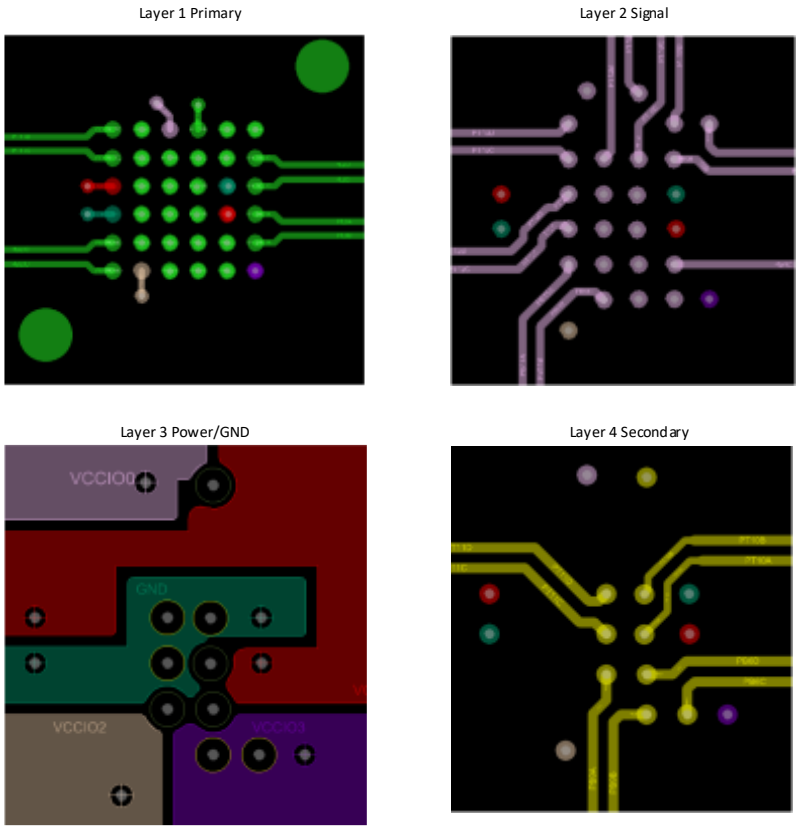


Figure 4.38. Layout Screen Shots, Example # 2 36-Bump WLCSP, 0.40 mm Pitch

4.9.7. 36-Bump WLCSP Breakout Example 3

This breakout uses an iCE40 Ultra PLD in a 2.06 mm × 2.06 mm, 0.35 mm pitch, 36-bump WLCSP package (ICE5LP4K-SWG36) in a 4-layer routing using via-in-pad technology. Sixteen via-in-pads are to be non-conductive epoxy filled and planarized. This example utilizes a 0.10 mm trace width/space (neck down trace width of 0.08 mm), escape via land of 0.20 mm and via drill of 0.10 mm. Two internal layers are set as reference planes.

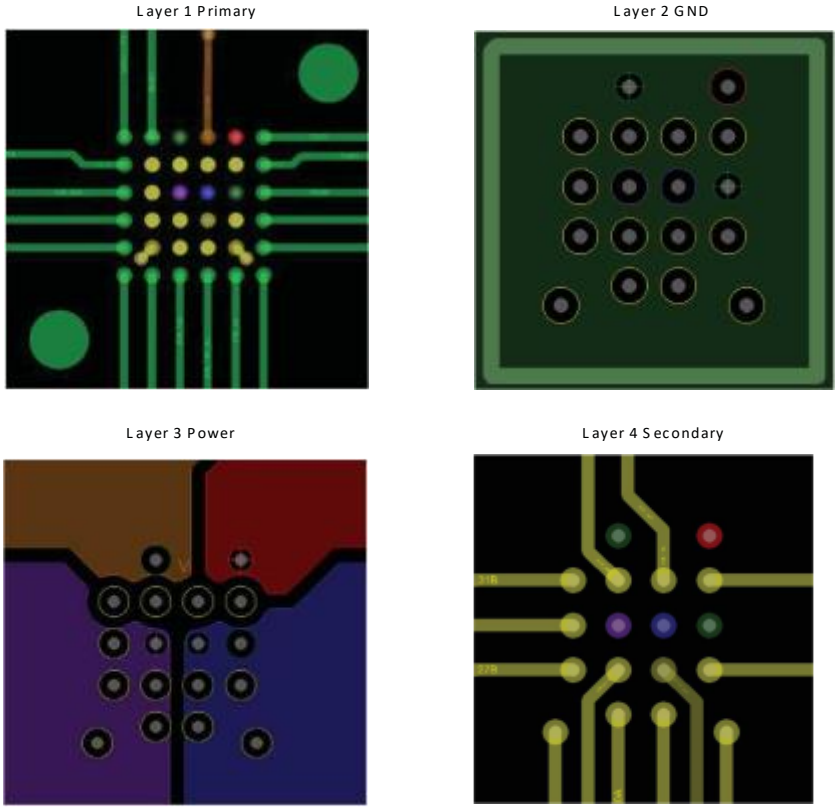


Figure 4.39. Layout Screen Shots, Example # 3 36-Bump WLCSP, 0.40 mm Pitch

4.9.8. 36-Bump WLCSP Breakout Example 4

This breakout uses an LIF-MD6000 PLD in a 2.51 mm × 2.51 mm, 0.4 mm pitch, 36-bump WLCSP package (LIFMD6000-6UWG36) in a 4-layer routing using via-in-pad technology. All vias are to be non-conductive epoxy filled. Flat surface at top land. This example utilizes a 0.063/0.043 mm trace width/space, escape via pad of 0.20 mm and via drill of 0.10 mm. Two internal layers are set as reference planes.

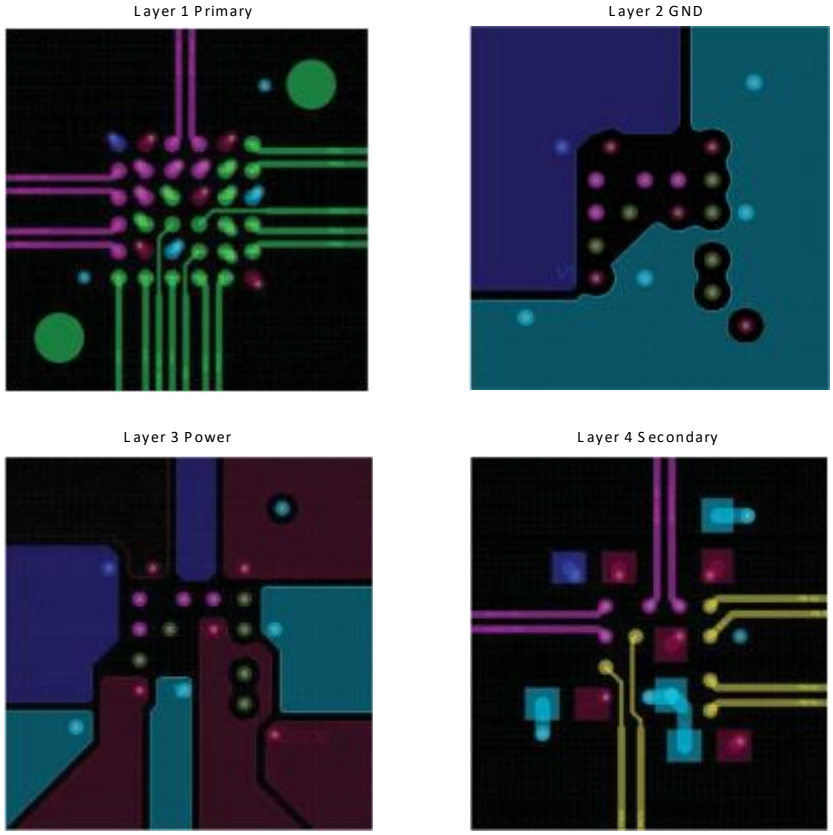


Figure 4.40. Layout Screen Shots, Example # 4 36-Bump WLCSP, 0.40 mm Pitch

4.9.9. 49-Bump WLCSP Breakout Example 1

This breakout uses a MachXO3 PLD in a 3.106 mm × 3.185 mm, 0.40 mm pitch, 49-bump WLCSP package (MXO3L-2100E-UWG49) with two different routing options. Example1: in a 4-layer routing using through microvia technology. Twenty-five via-in-pads are to be non-conductive epoxy filled and planarized. This example utilizes a BGA land of 0.30 mm, 0.07 mm trace width and 0.05 space, escape via land of 0.20 mm and via drill of 0.10 mm. Two internal layers are set as signal layer and a reference plane.

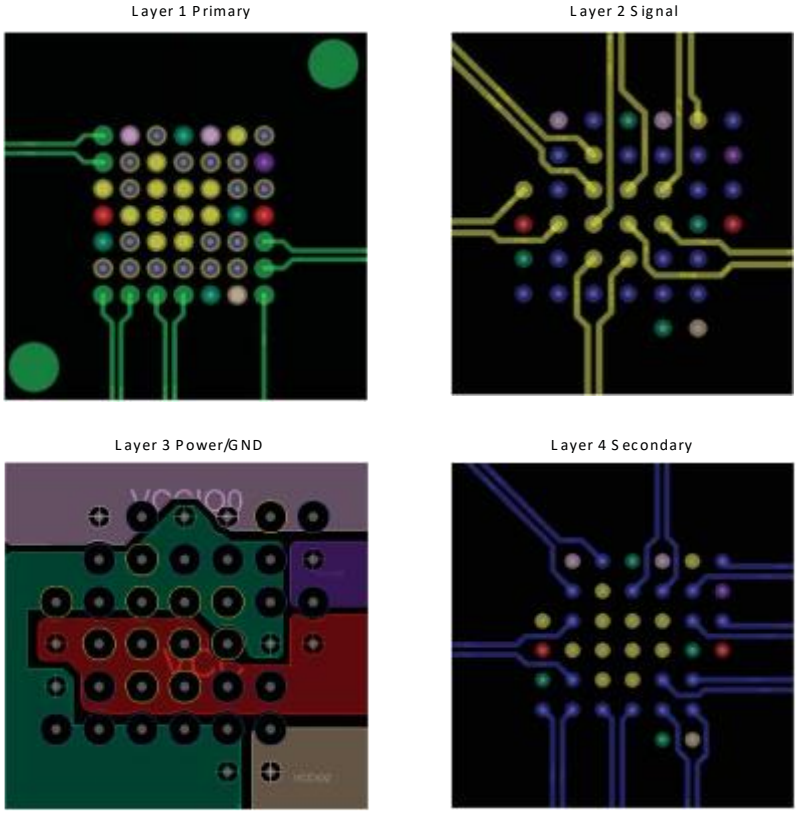


Figure 4.41. Layout Screen Shots, Example #1 49-Bump WLCSP, 0.40 mm Pitch

4.9.10. 49-Bump WLCSP Breakout Example 2

Example 2 is also in a 4-layer routing using blind vias, microvia technology. Twenty-three via-in-pads are to be nonconductive epoxy filled and planarized. This example utilizes a BGA land of 0.25 mm, 0.10 mm trace width/space and neck down width/space of 0.07 mm. Escape via land of 0.20 mm and via drill of 0.10 mm. Two internal layers are set as signal layer and a reference plane.

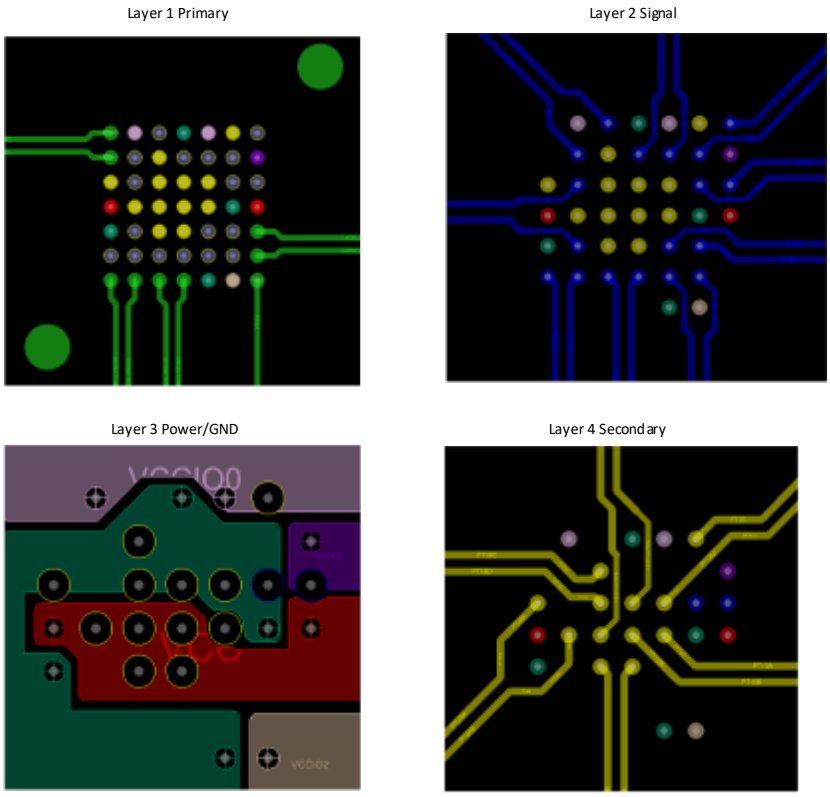


Figure 4.42. Layout Screen Shots, Example #2 49-Bump WLCSP, 0.40 mm Pitch

4.9.11. 72-Bump WLCSP Breakout Example

This breakout uses a Crosslink-NX in a 4.125 mm × 3.807 mm, 0.40 mm pitch, 72-bump WLCSP package (LIFCL-17-UWG72) in a 4-layer routing using via-in-pad technology. Fifty seven vias are to be non-conductive epoxy filled and planarized. This example utilizes a 0.076 mm trace width and 0.050 mm space, escape via pad of 0.200 mm and via drill of 0.100 mm. Two internal layers are set as reference planes..

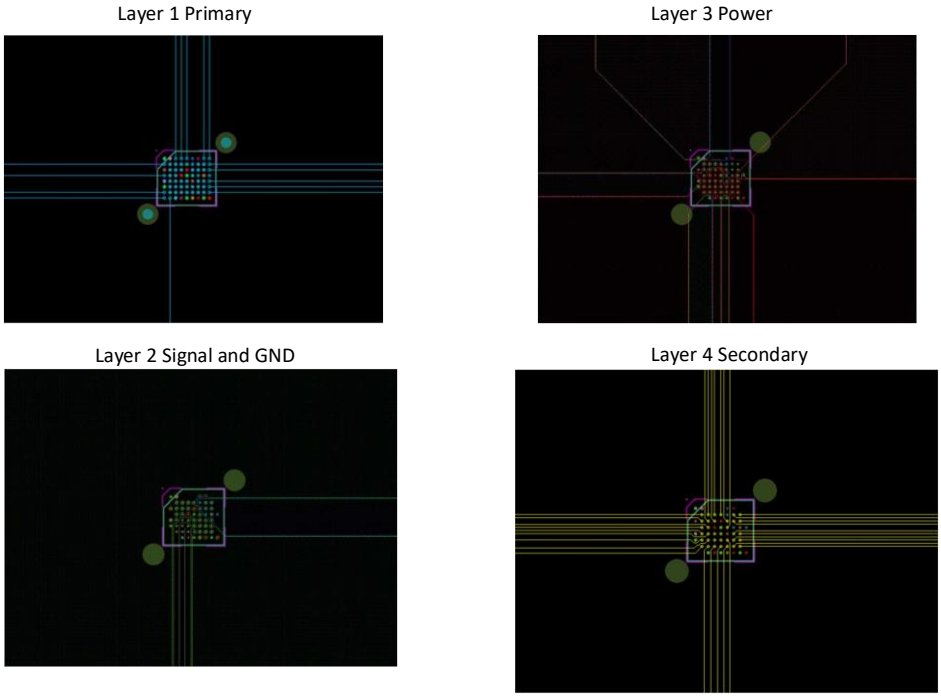


Figure 4.43. Layout Screen Shots, Example 72-Bump WLCSP, 0.40 mm Pitch

4.9.12. 81-Bump WLCSP Breakout Example 1

This breakout uses a MXO3 PLD in a 3.797 mm × 3.693 mm, 0.40 mm pitch, 81-bump WLCSP package (MXO3L-2100E-UWG81) with two different routing options. Example1: in a 4-layer routing using through microvia technology. Twenty-five via-in-pads are to be non-conductive epoxy filled and planarized. This example utilizes a BGA land of 0.30 mm, 0.07 mm trace width and 0.05 space, escape via land of 0.20 mm and via drill of 0.10 mm. Two internal layers are set as signal layer and a reference plane.

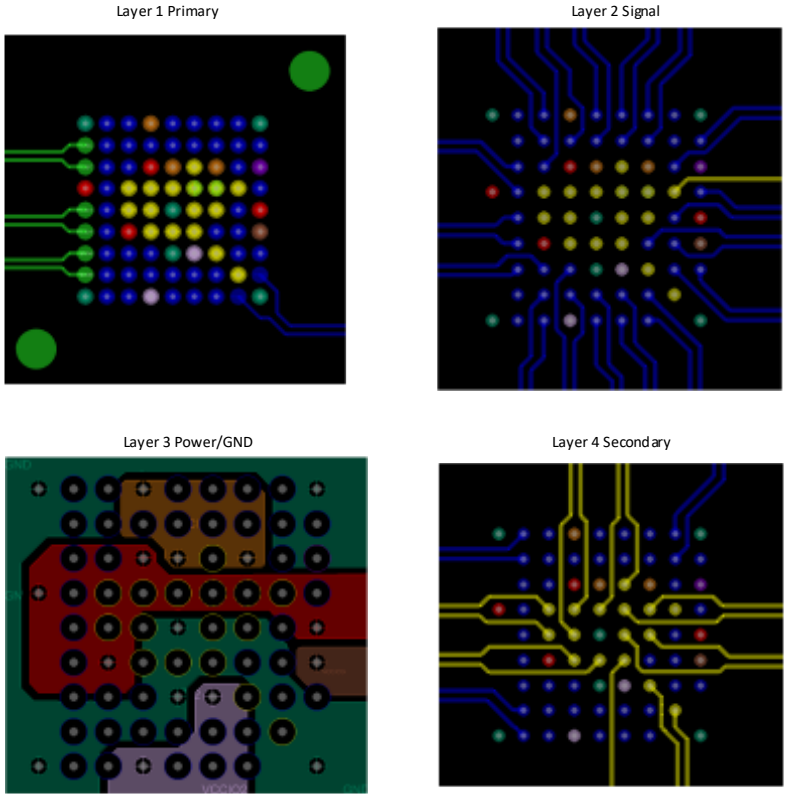


Figure 4.44. Layout Screen Shots, Example #1 81-Bump WLCSP, 0.40 mm Pitch

4.9.13. 81-Bump WLCSP Breakout Example 2

Example 2 is also in a 4-layer routing using blind vias, microvia technology. Twenty-three via-in-pads are to be nonconductive epoxy filled and planarized. This example utilizes a BGA land of 0.25 mm, 0.10 mm trace width/space and neckdown width/space of 0.07 mm. Escape via land of 0.20 mm and via drill of 0.10 mm. Two internal layers are set as signal layer and a reference plane.

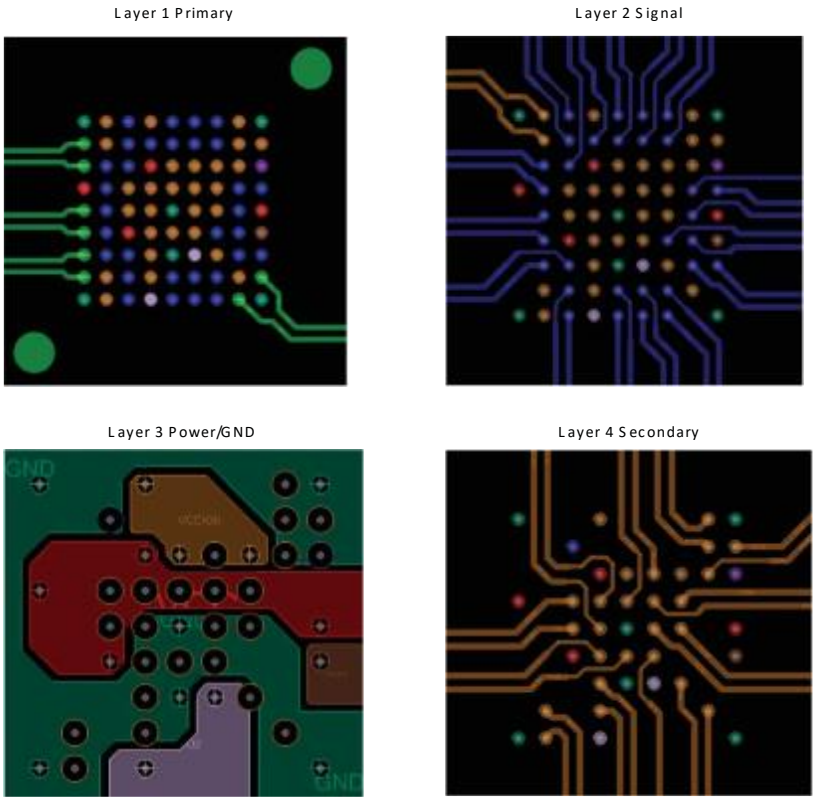


Figure 4.45. Layout Screen Shots, Example #2 81-Bump WLCSP, 0.40 mm Pitch

4.10. Fully-/Partially-Populated Ball Grid Array

4.10.1. CM36/CM36A Fully-Populated Ball-Grid Array, All 25 User I/O

The CM36/CM36A package is a 6 × 6, fully-populated array of 0.4 mm solder balls.

Table 4.3. CM36/CM36A, Four-Layer Layout Dimensions

Standard	Dimension	
Layers	4	
BGA Solder Pad Size	0.20 mm	7.87 mils
BGA Pad Solder Mask	0.34 mm	13.39 mils
BGA Via Size (Drill)	0.1270 mm	5 mils
BGA Via Size (Pad)	0.2540 mm	10 mils
Trace Width	0.1270 mm	5 mils
Trace Spacing	0.0889 mm	3.5 mils

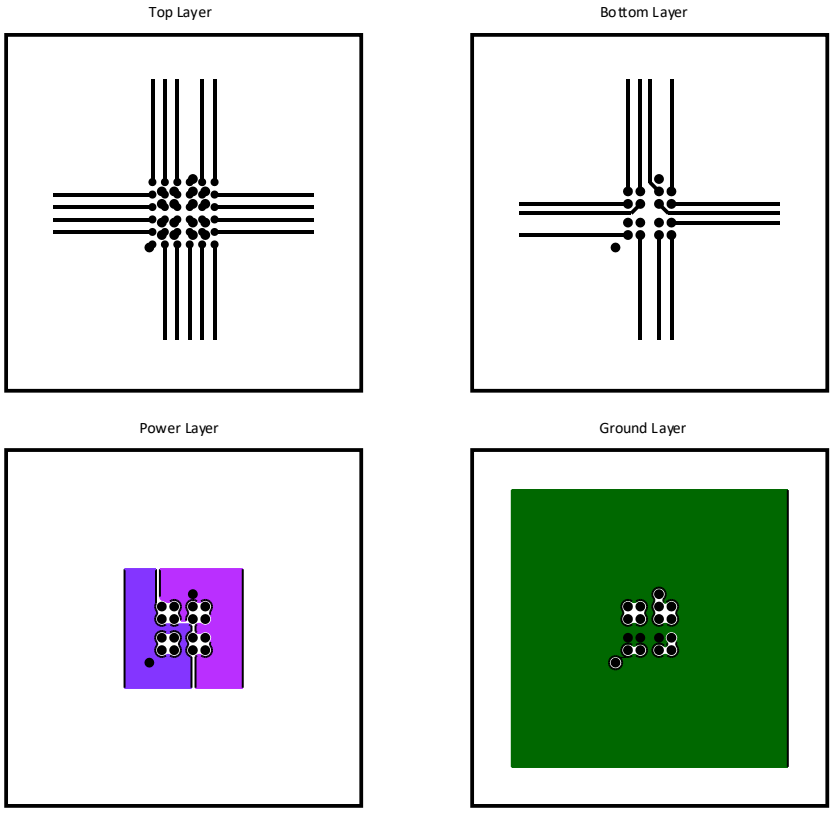


Figure 4.46. Four-Layer Example Shown for CM36

4.10.2. CM49 Fully-Populated Ball-Grid Array, All 35 User I/O

The CM49 package is a 7 × 7, fully-populated array of 0.4 mm solder balls.

Table 4.4. CM49, Four-Layer Layout Dimensions

Standard	Dimension	
Layers	4	
BGA Solder Pad Size	0.20 mm	7.87 mils
BGA Pad Solder Mask	0.34 mm	13.39 mils
BGA Via Size (Drill)	0.1270 mm	5 mils
BGA Via Size (Pad)	0.2540 mm	10 mils
Trace Width	0.1270 mm	5 mils
Trace Spacing	0.0889 mm	3.5 mils

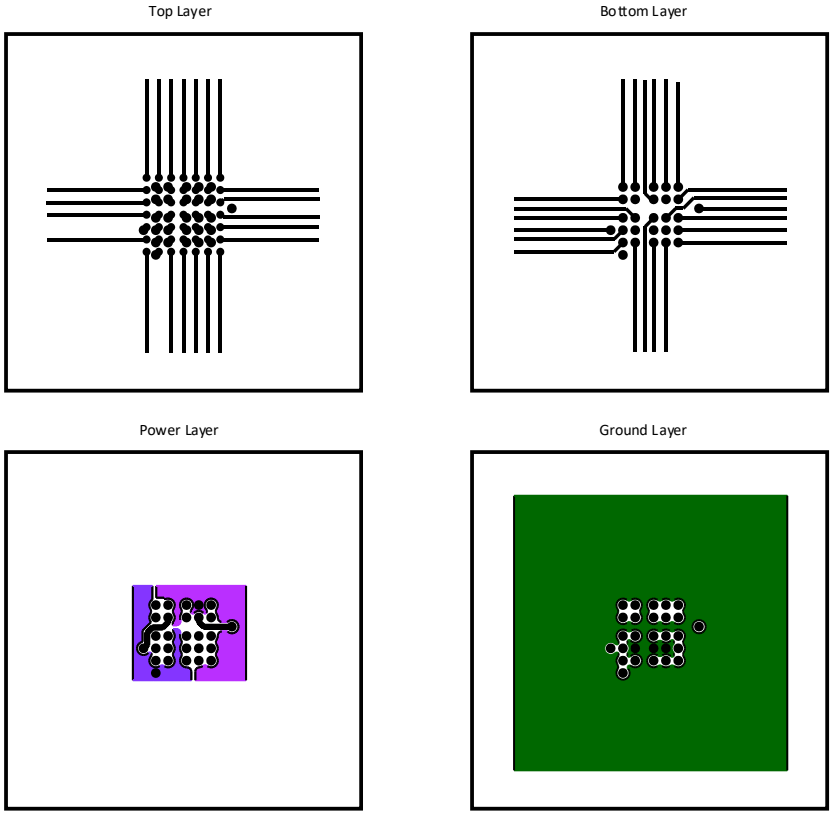


Figure 4.47. Four-Layer Example Shown for CM49

4.10.3. CM81 Fully-Populated Ball-Grid Array - Four Layers, 48 User I/O

The CM81 package is a 9 × 9, fully-populated array of 0.4 mm solder balls. This layout option uses just four total layers but still provides 48 user I/O, 15 less than the six-layer option. This option provides 13 more I/O than the CM49 but still uses just four PCB layers.

Table 4.5. CM81, Four-Layer Layout Dimensions

Standard	Dimension	
Layers	4	
BGA Solder Pad Size	0.20 mm	7.87 mils
BGA Pad Solder Mask	0.20 mm	7.87 mils
BGA Via Size (Drill)	0.1270 mm	5 mils
BGA Via Size (Pad)	0.2540 mm	10 mils
Trace Width	0.1270 mm	5 mils
Trace Spacing	0.0889 mm	3.5 mils

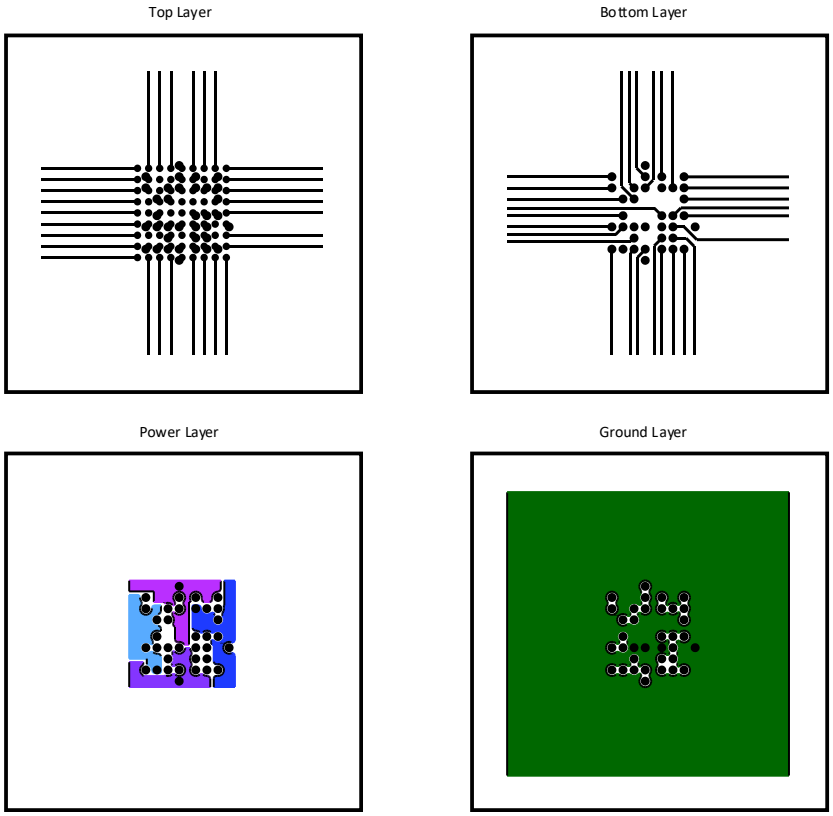


Figure 4.48. Four-Layer CM81

4.10.4. CM81 Fully-Populated Ball-Grid Array - Six Layers, All 63 User I/O

The CM81 package is a 9 × 9, fully-populated array of 0.4 mm solder balls.

Table 4.6. CM81, Six-Layer Layout Dimensions

Standard	Dimension	
Layers	6	
BGA Solder Pad Size	0.20 mm	7.847 mils
BGA Pad Solder Mask	0.34 mm	13.39 mils
BGA Via Size (Drill)	0.1270 mm	5 mils
BGA Via Size (Pad)	0.2540 mm	10 mils
Trace Width	0.1270 mm	5 mils
Trace Spacing	0.0889 mm	3.5 mils

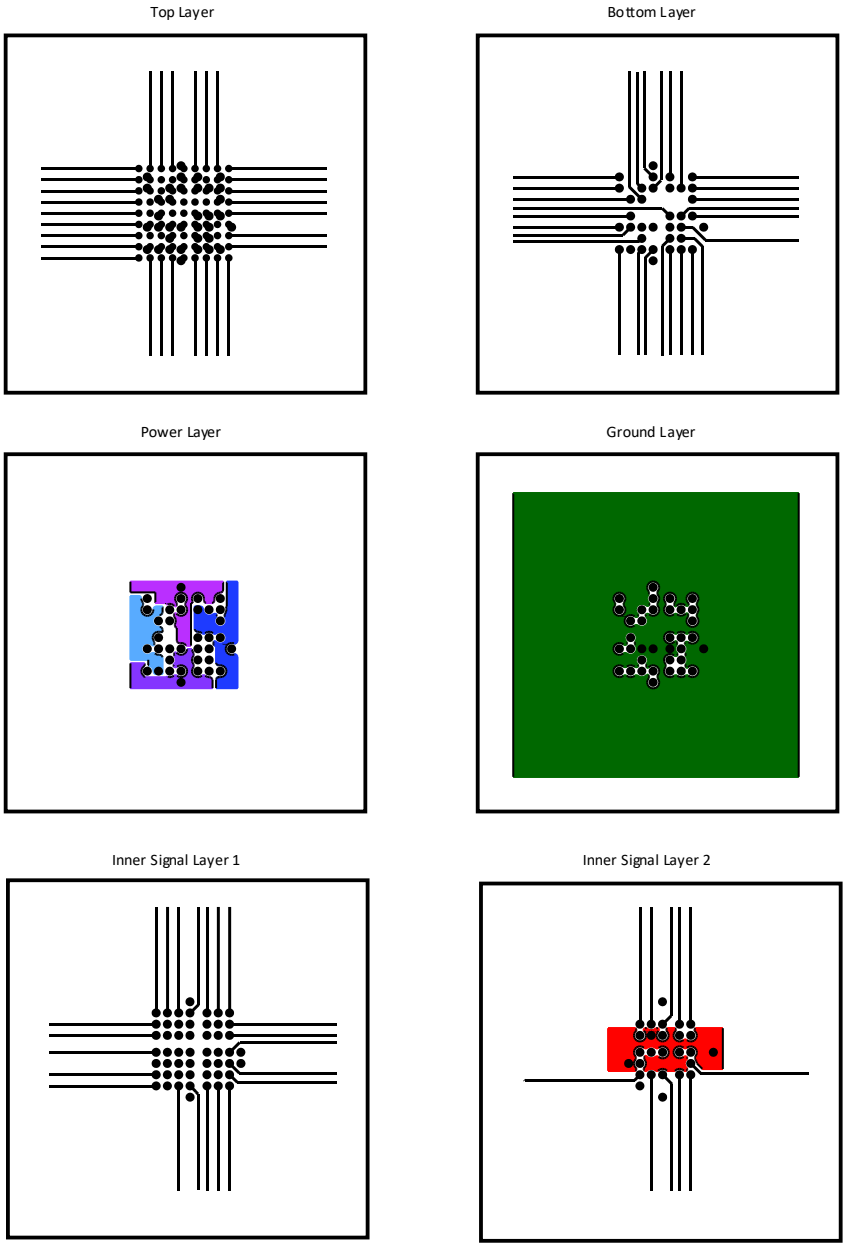


Figure 4.49. Six-Layer CM81

4.10.5. CM121 Fully-Populated Ball-Grid Array - Four Layers, 57 User I/O

The CM121 package is an 11 × 11, fully-populated array of 0.4 mm solder balls. This layout option uses just four total layers but still provides 57 user I/O, 38 less than the six-layer option.

Table 4.7. CM121, Four-Layer Layout Dimensions

Standard	Dimension	
Layers	4	
BGA Solder Pad Size	0.20 mm	7.87 mils
BGA Pad Solder Mask	0.20 mm	7.87 mils
BGA Via Size (Drill)	0.1270 mm	5 mils
BGA Via Size (Pad)	0.2540 mm	10 mils
Trace Width	0.1270 mm	5 mils
Trace Spacing	0.0889 mm	3.5 mils

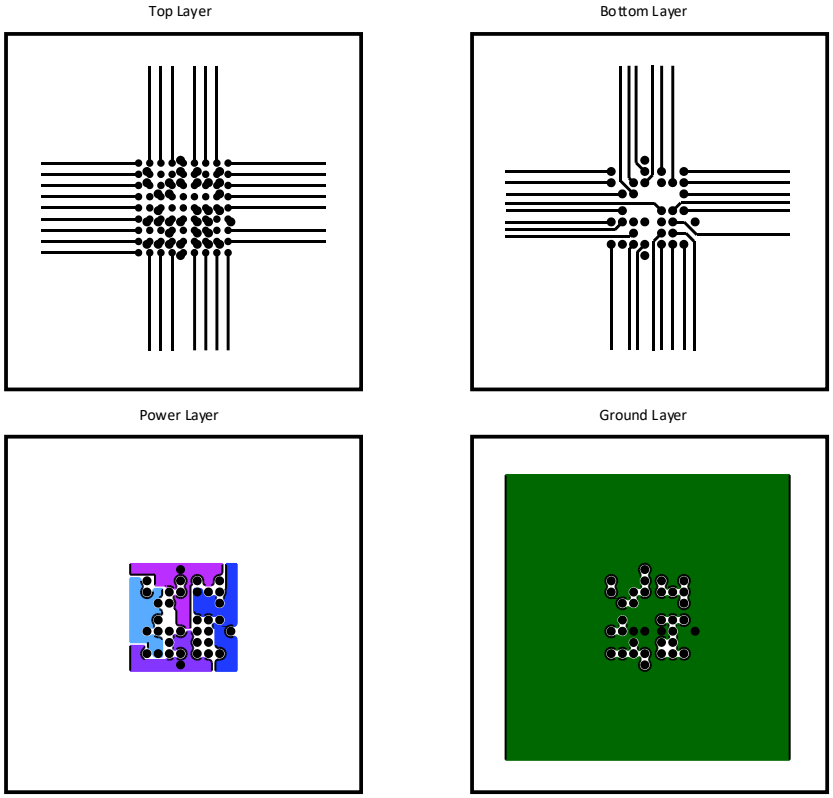


Figure 4.50. Six-Layer CM121

4.10.6. CM121 Fully-Populated Ball-Grid Array - Six Layers, All 95 User I/O

The CM121 package is an 11 × 11, fully-populated array of 0.4 mm solder balls.

Table 4.8. CM121, Six-Layer Layout Dimensions

Standard	Dimension	
Layers	6	
BGA Solder Pad Size	0.20 mm	7.847 mils
BGA Pad Solder Mask	0.34 mm	13.39 mils
BGA Via Size (Drill)	0.1270 mm	5 mils
BGA Via Size (Pad)	0.2540 mm	10 mils
Trace Width	0.1270 mm	5 mils
Trace Spacing	0.0889 mm	3.5 mils

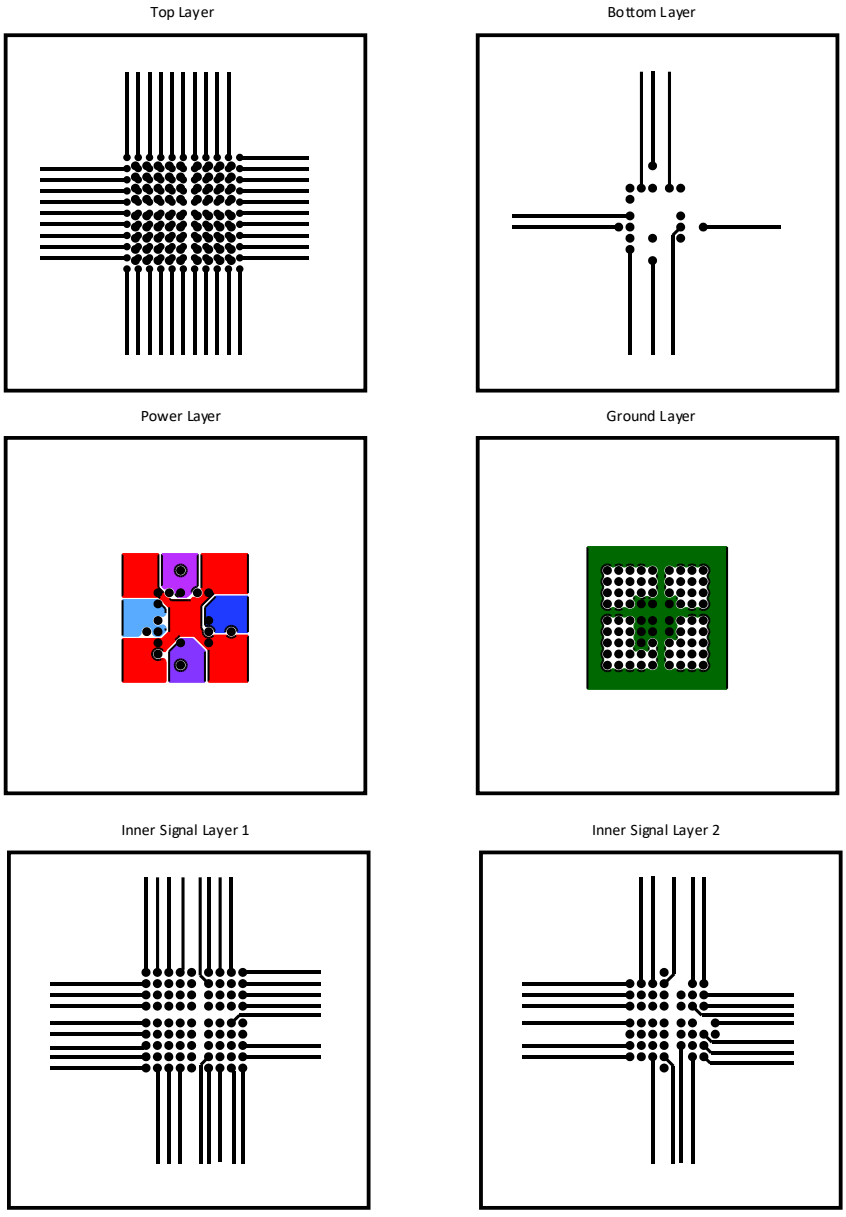


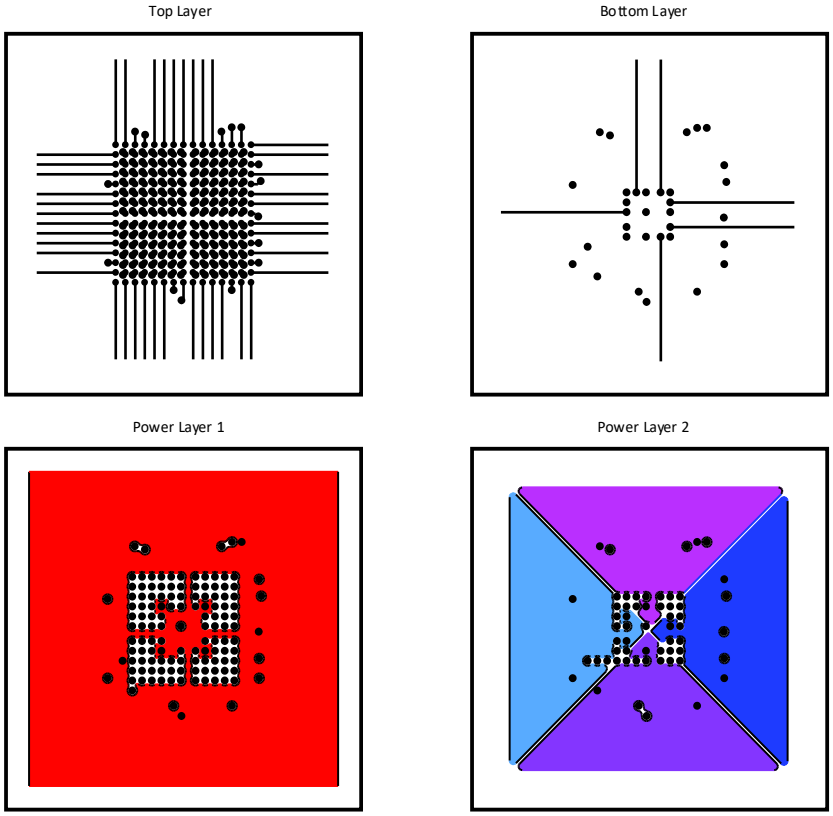
Figure 4.51. Six-Layer CM121

4.10.7. CM225 Fully-Populated Ball-Grid Array - Ten Layers, All 178 User I/O

The CM225 package is a 15 × 15, fully-populated array of 0.4 mm solder balls.

Table 4.9. CM225, Ten-Layer Layout Dimensions

Standard	Dimension	
Layers	10	
BGA Solder Pad Size	0.20 mm	7.87 mils
BGA Pad Solder Mask	0.34 mm	13.39 mils
BGA Via Size (Drill)	0.1270 mm	5 mils
BGA Via Size (Pad)	0.2540 mm	10 mils
Trace Width	0.1270 mm	5 mils
Trace Spacing	0.0889 mm	3.5 mils



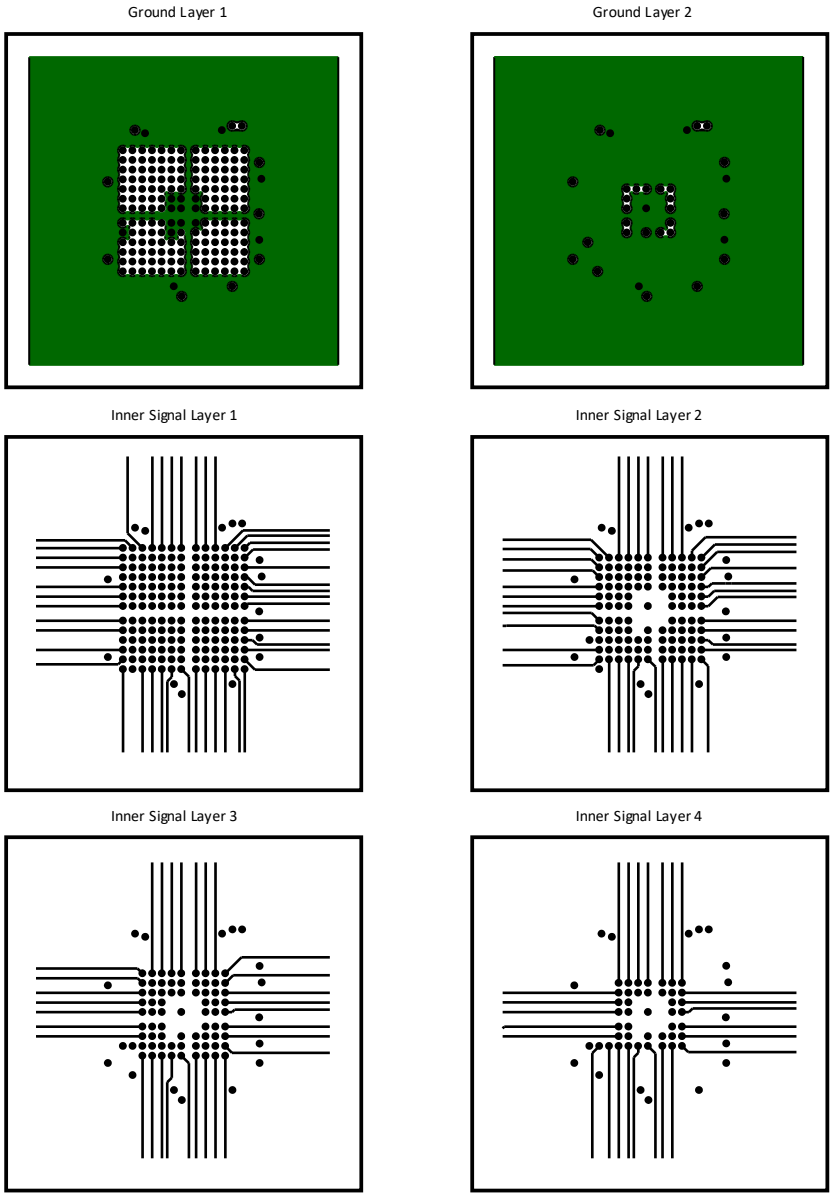


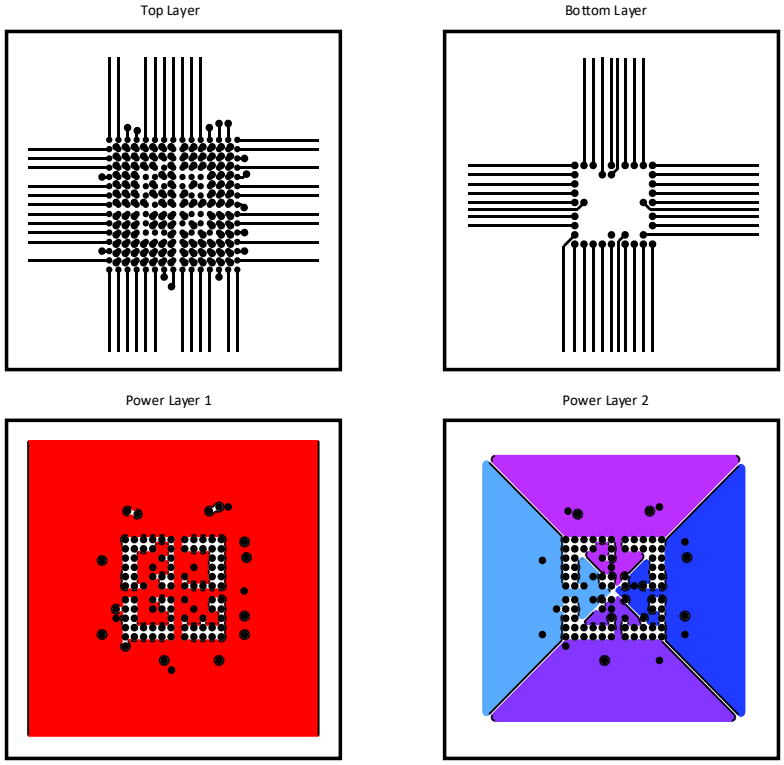
Figure 4.52. Ten-Layer CM225

4.10.8. CM225 Fully-Populated Ball-Grid Array - Eight Layers, 153 User I/O

The CM225 package is a 15 × 15, fully-populated array of 0.4 mm solder balls. This layout option uses just eight total layers but still provides 153 user I/O, 25 less PIOs than the ten-layer option. The primary advantage of this layout over the full I/O layout is that it eliminates two layers.

Table 4.10. CM225, Eight-Layer Layout Dimensions

Standard	Dimension	
Layers	10	
BGA Solder Pad Size	0.20 mm	7.87 mils
BGA Pad Solder Mask	0.20 mm	7.87 mils
BGA Via Size (Drill)	0.1270 mm	5 mils
BGA Via Size (Pad)	0.2540 mm	10 mils
Trace Width	0.1270 mm	5 mils
Trace Spacing	0.0889 mm	3.5 mils



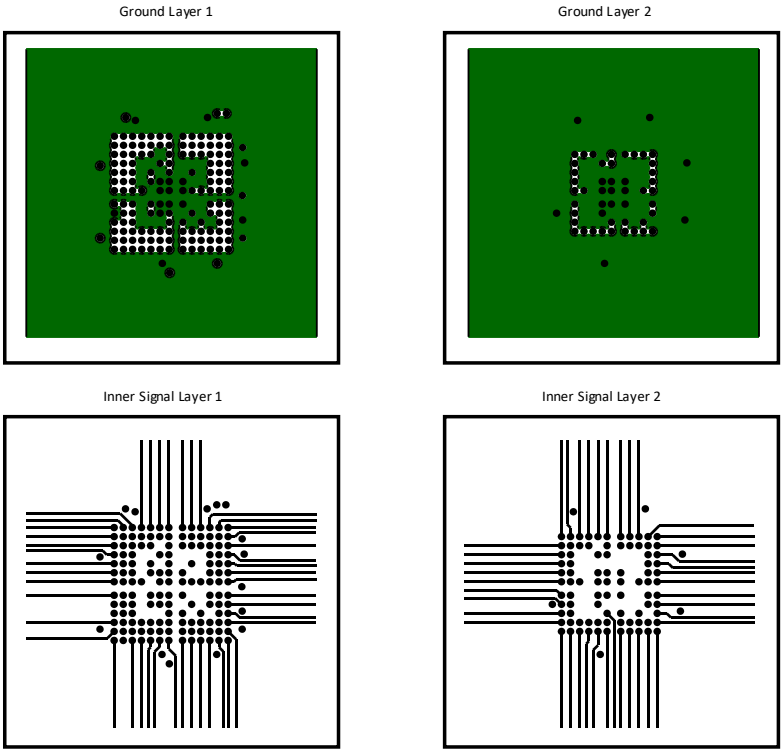


Figure 4.53. Eight-Layer CM225

4.10.9. CM225 Fully-Populated Ball-Grid Array - Six Layers, 100 User I/O

The CM225 package is a 15 mm × 15 mm, fully-populated array of 0.4 mm solder balls. This layout option uses just six total layers but still provides 100 user I/O, 78 less than the ten-layer option. This layout is marginally useful. It allows the iCE40HX8K device to use the 7 mm × 7 mm CM225 package, but uses just six PCB layers. The 8 mm × 8 mm CB132 package provides 95 user I/O but provides 95 user I/O pins.

Table 4.11. CM225, Six-Layer Layout Dimensions

Standard	Dimension	
Layers	6	
BGA Solder Pad Size	0.20 mm	7.87 mils
BGA Pad Solder Mask	0.20 mm	7.87 mils
BGA Via Size (Drill)	0.1270 mm	5 mils
BGA Via Size (Pad)	0.2540 mm	10 mils
Trace Width	0.1270 mm	5 mils
Trace Spacing	0.0889 mm	3.5 mils

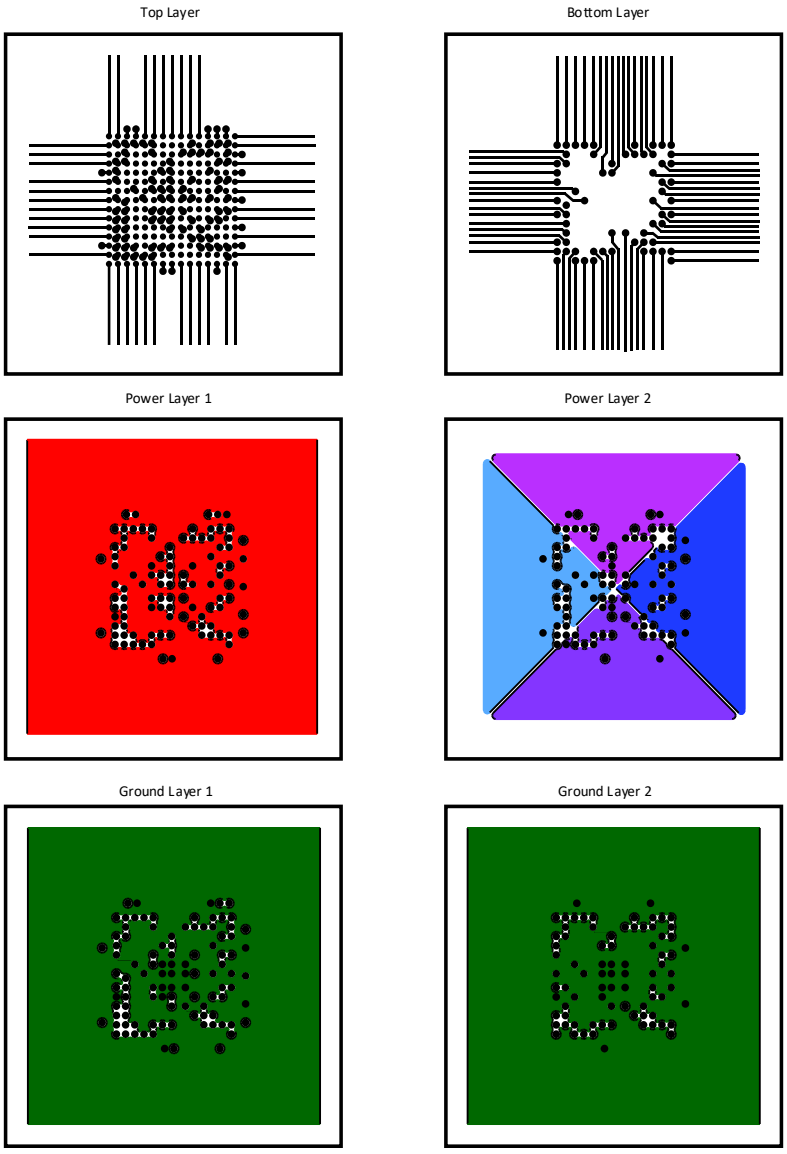


Figure 4.54. Six-Layer CM225

4.10.10. CB81 Fully-Populated Ball-Grid Array

The CB81 package is a 9 × 9, fully-populated array of 0.5 mm solder balls. The layout example here uses non solder mask defined (NSMD) design rules similar to other fully-populated ball-grid arrays.

Table 4.12. CB81, Four-Layer Layout Dimensions

Standard	Dimension	
Layers	4	
BGA Solder Pad Size	0.20 mm	7.847 mils
BGA Pad Solder Mask	0.30 mm	11.811 mils
BGA Via Size (Drill)	0.1524 mm	6 mils
BGA Via Size (Pad)	0.3048 mm	12 mils
Trace Width	0.1016 mm	4 mils
Trace Spacing	0.0889 mm	3.5 mils

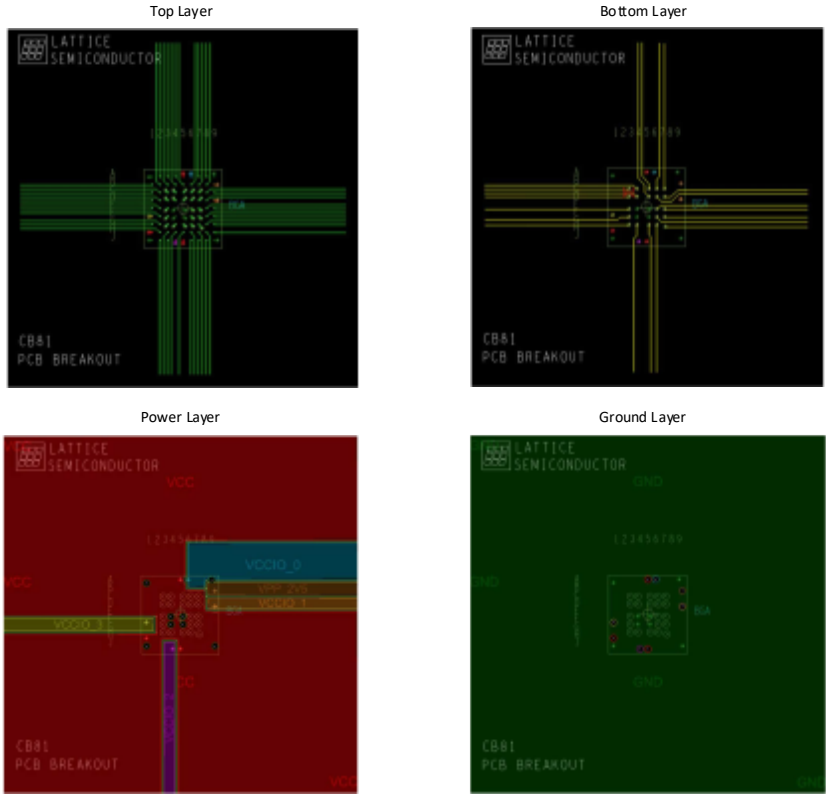


Figure 4.55. Four-Layer CB81

4.10.11. CB121 Fully-Populated Ball-Grid Array (Option 1)

The CB121 package is an 11x11, fully-populated array of 0.5 mm solder balls. The layout example here uses non solder mask defined (NSMD) design rules similar to other fully-populated ball-grid arrays.

Table 4.13. CB121, Six-Layer Layout Dimensions (Option 1)

Standard	Dimension	
Layers	4	
BGA Solder Pad Size	0.20 mm	7.847 mils
BGA Pad Solder Mask	0.30 mm	11.811 mils
BGA Via Size (Drill)	0.20 mm	8 mils
BGA Via Size (Pad)	0.20 mm	8 mils
Trace Width	0.10 mm	4 mils
Trace Spacing	0.076 mm	3 mils

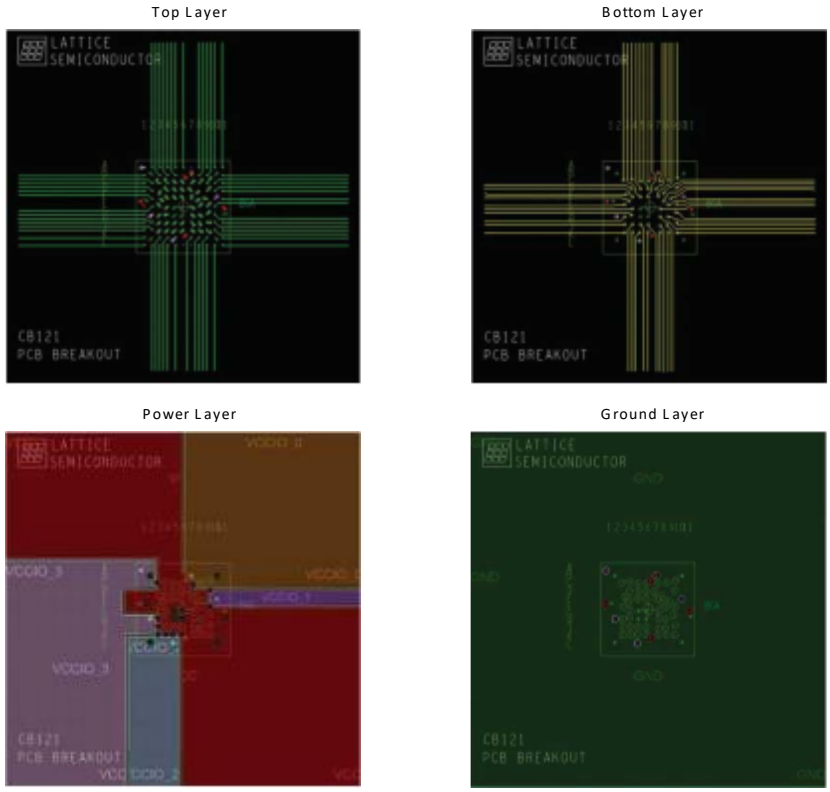


Figure 4.56. Six-Layer CB121 (Option 1)

4.10.12. CB121 Fully-Populated Ball-Grid Array (Option 2)

The CB121 package is an 11 × 11, fully-populated array of 0.5 mm solder balls. The layout example here uses non solder mask defined (NSMD) design rules similar to other fully-populated ball-grid arrays.

Table 4.14. CB121, Six-Layer Layout Dimensions (Option 2)

Standard	Dimension	
Layers	4	
BGA Solder Pad Size	0.20 mm	7.847 mils
BGA Pad Solder Mask	0.30 mm	11.811 mils
BGA Via Size (Drill)	0.20 mm	8 mils
BGA Via Size (Pad)	0.20 mm	8 mils
Trace Width	0.10 mm	4 mils
Trace Spacing	0.076 mm	3 mils

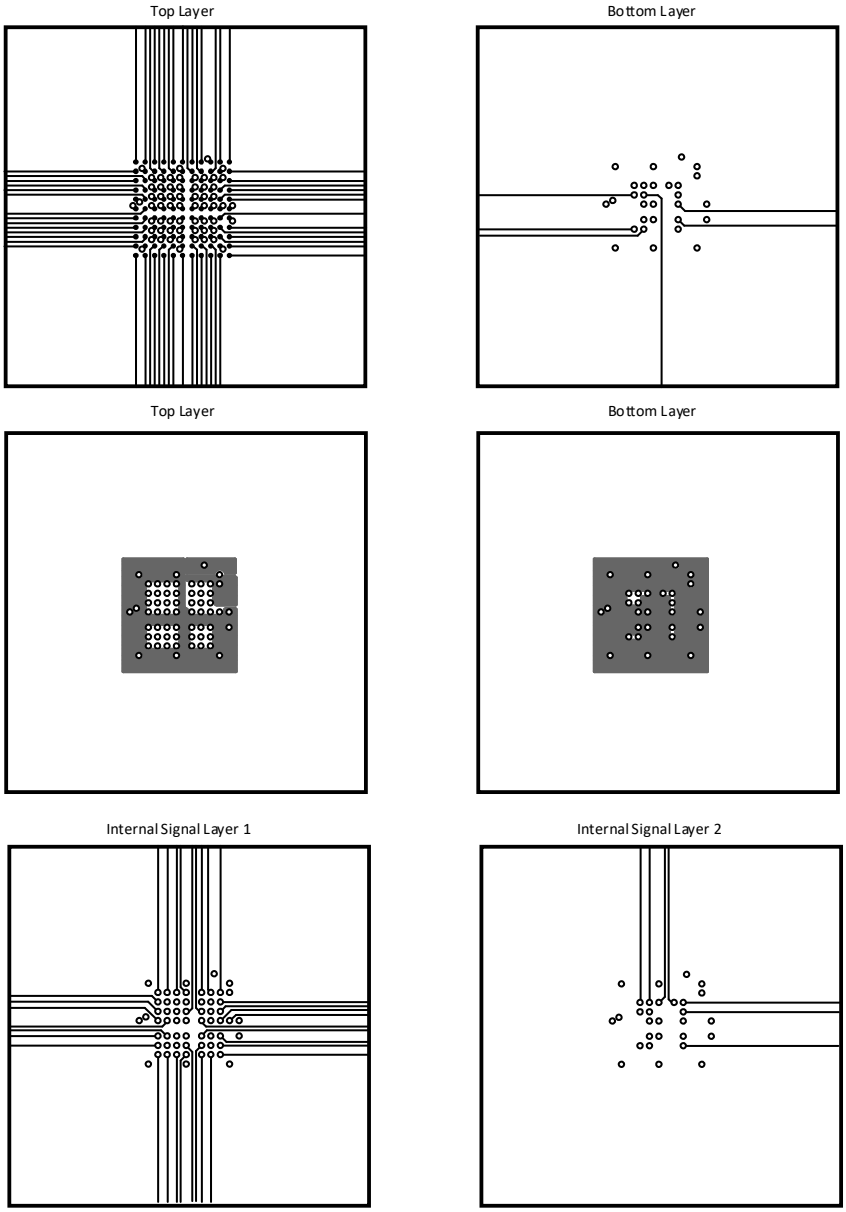


Figure 4.57. Six-Layer CB121 (Option 2)

4.10.13. CB132 Partially-Populated Ball-Grid Array - Six Layer, Non Solder Mask Defined (NSMD), 4 mil Traces

The CB132 package is chip-scale package with a partially-populated, 14 mm × 14 mm ball-grid1 array of 0.5 mm solder balls.

Table 4.15. CB132, Six-Layer Layout Dimensions, Relaxed Design Rule

Standard	Dimension	
Layers	6	
BGA Solder Pad Size	0.254 mm	10 mils
BGA Pad Solder Mask	0.4064 mm	16 mils
BGA Via Size (Drill)	0.1524 mm	6 mils
BGA Via Size (Pad)	0.3048 mm	12 mils
Trace Width	0.1016 mm	4 mils
Trace Spacing	0.1016 mm	4 mils

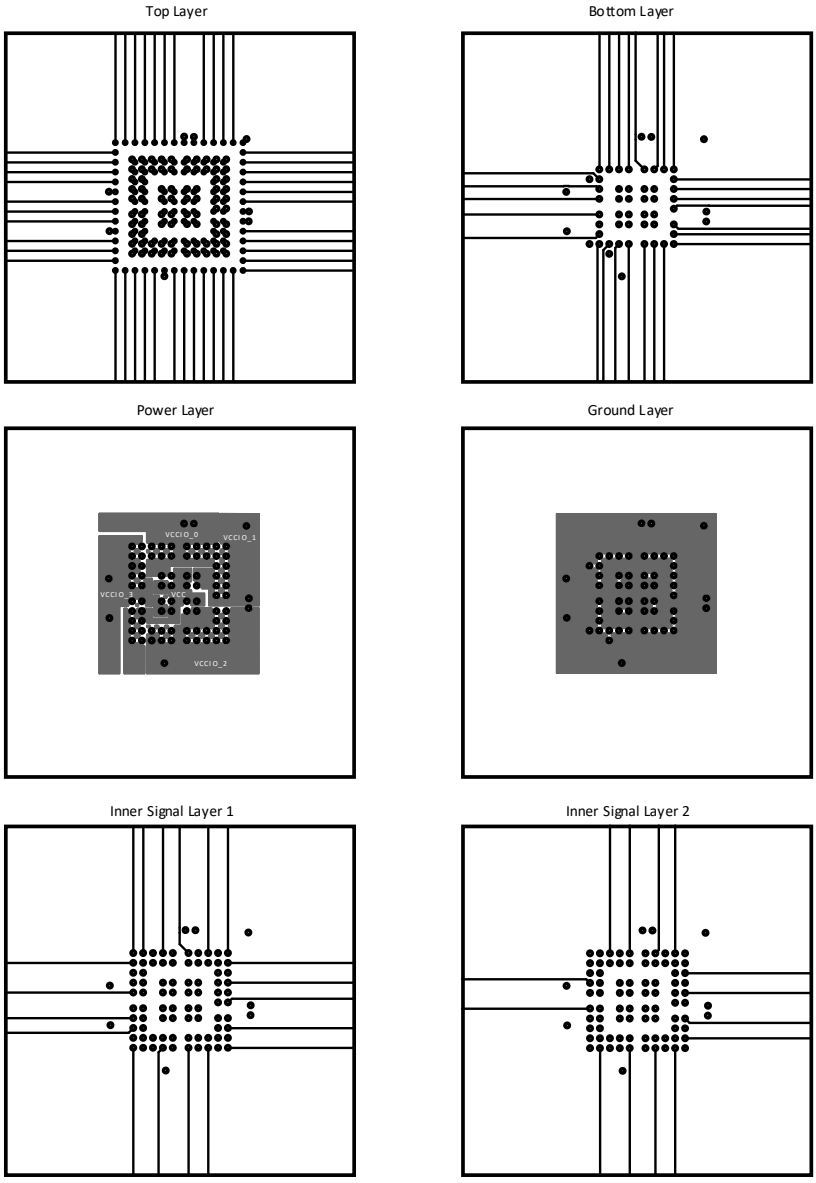


Figure 4.58. Six-Layer CB132, Relaxed Design Rule

4.10.14. CB132 Partially-Populated Ball-Grid Array - Four Layer, Non Solder Mask Defined (NSMD), 3 mil Traces

The CB132 package is chip-scale package with a partially-populated, 14 mm × 14 mm ball-grid1 array of 0.5 mm solder balls.

Table 4.16. CB132, Four-Layer Layout Dimensions

Standard	Dimension	
Layers	4	
BGA Solder Pad Size	0.254 mm	10 mils
BGA Pad Solder Mask	0.4064 mm	16 mils
BGA Via Size (Drill)	0.127 mm	5 mils
BGA Via Size (Pad)	0.254 mm	10 mils
Trace Width	0.0762 mm	3 mils
Trace Spacing	0.0762 mm	3 mils

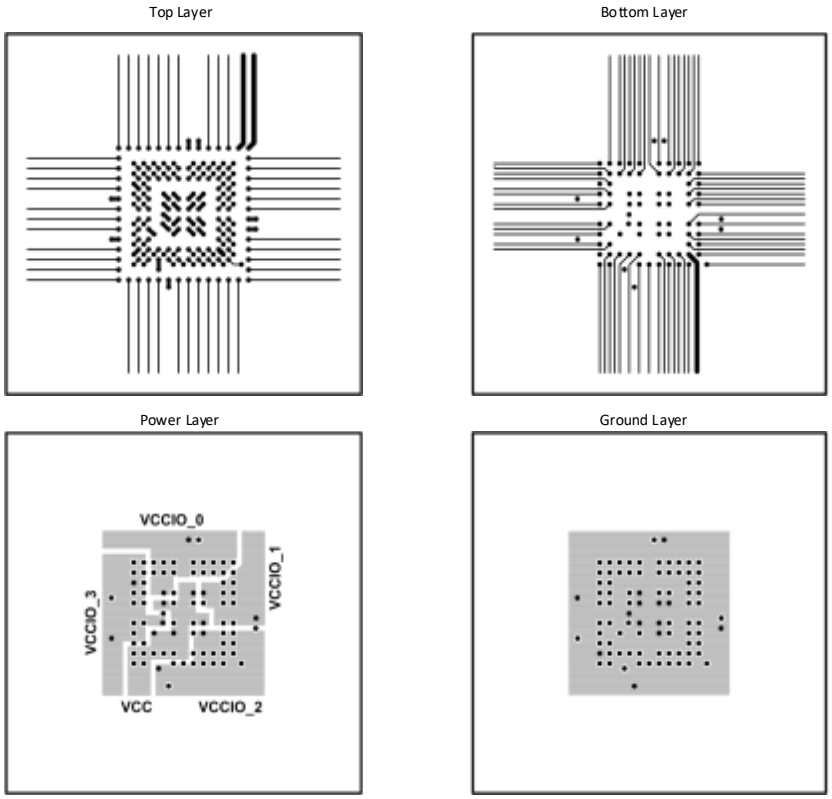


Figure 4.59. Four-Layer CB132

4.10.15. CT256 Fully-Populated Ball-Grid Array - Six Layers, All 206 User I/O

The CT256 package is a 16 mm × 16 mm, fully-populated array of 0.8 mm solder balls.

Table 4.17. CT256, Six-Layer Layout Dimensions

Standard	Dimension	
Layers	6	
BGA Solder Pad Size	0.20 mm	7.847 mils
BGA Pad Solder Mask	0.34 mm	13.39 mils
BGA Via Size (Drill)	0.1270 mm	5 mils
BGA Via Size (Pad)	0.2540 mm	10 mils
Trace Width	0.1270 mm	5 mils
Trace Spacing	0.0889 mm	3.5 mils

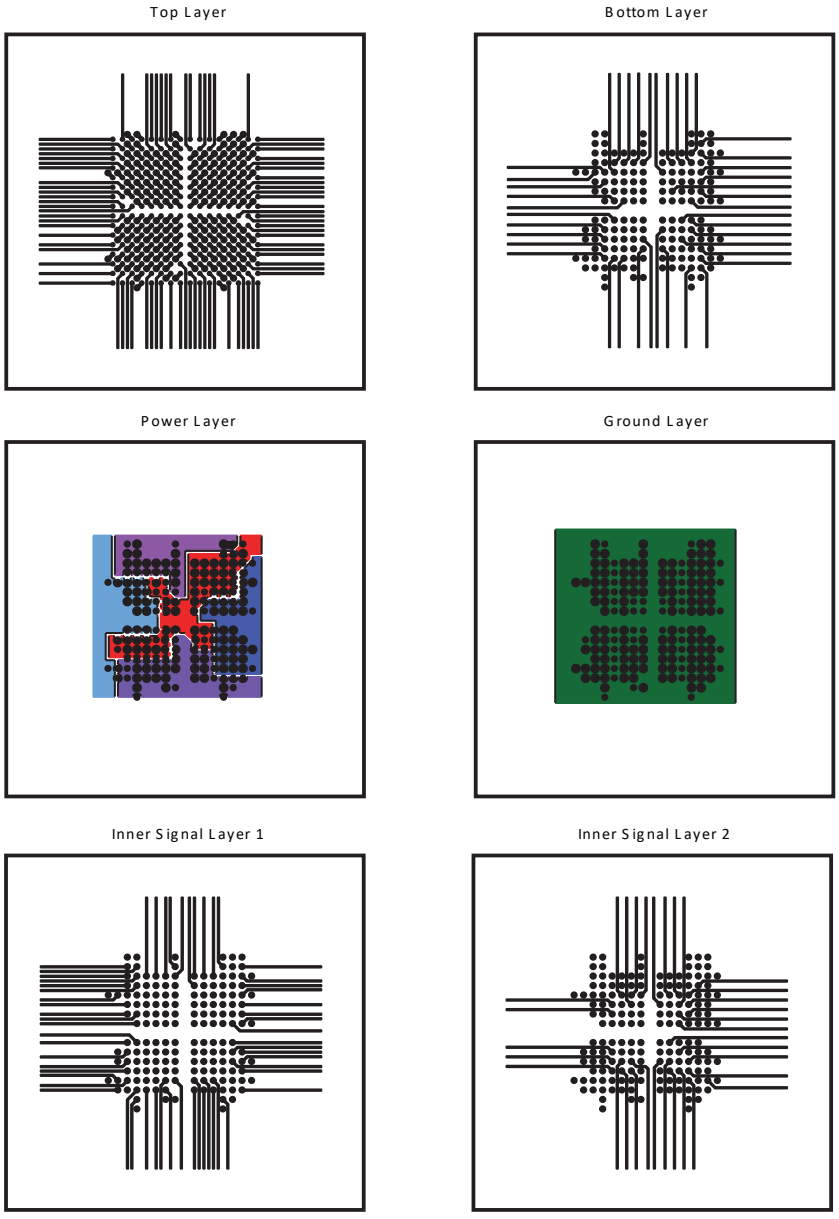


Figure 4.60. Six-Layer CT256

5. PCB Fabrication Cost and Design Rule Considerations

PCB fabrication cost is a key consideration for many electronics products. By reviewing the IC device package ball density and pitch, I/O signal requirements of your application, and the manufacturing constraints of your PCB fabrication facility you can better weigh the trade-offs between design decisions.

Choosing the best package for your application involves answering a few questions:

- What is the driving factor in the application? The smallest possible form factor or a low PCB cost?
- How many I/O signals does the application require?
- What PCB layer stack up provides the best I/O density within budget?
- What layout design rules does the printed-circuit board (PCB) vendor support?
- How many PCB layers does the budget allow?

As the ball pitch becomes smaller with each new BGA generation, new PCB fabrication techniques and signal via type have been developed to handle the complexities. Micro vias, laser vias, filled, buried and blind vias, even buried and plated over vias. Complex boards use a combination of most of these.

Stack-up types, ordered by cost, high-to-low include:

- High-Density Interconnect (HDI) build up with micro vias
- Laminated with blind and buried vias
- Laminated with through vias

6. HDI Stack-up

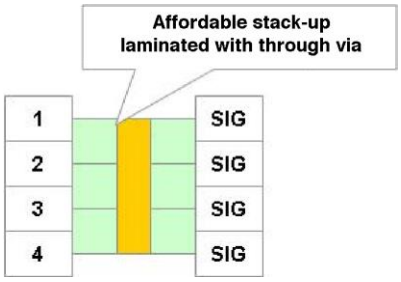


Figure 6.1. Stack-up Example

HDI is a *sandwich* with older-style larger geometry in the middle with fully drilled through holes and then a stack of fine geometry of blind, buried or mixed via, laminated both on the top and bottom of the middle stack-up. The laminated layers are thinner than traditional layers and allow finer drilling technology. Staggered micro vias allow vias within close tolerance or connected to a BGA pad to go down to the next layer or more to route away for escape routing or underneath the BGA device for further interconnect. HDI type interconnect is used on complex boards and takes extra steps in the processing flow due to special drilling, plating an laminations. It is a mix of older technology mixed with newer technology that results in a board that is highly routable.

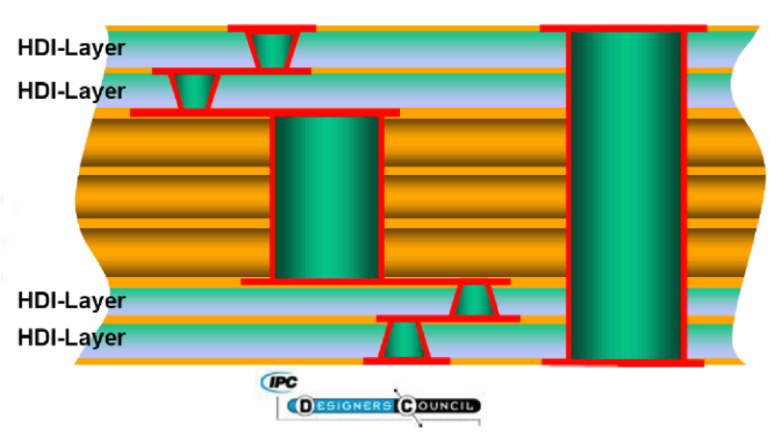


Figure 6.2. HDI Stack-up with Staggered Micro Vias

7. Advantages and Disadvantages of BGA Packaging

As pin counts increase and board space becomes more valuable, it is important to place as many circuits per square inch as possible. BGA offer the best I/O density for a given PCB area. Lattice offers a range of packages from a 4 mm × 4 mm 64-ball csBGA to a 33 mm × 33 mm 1704-ball fcBGA.

One of the greatest advantages of BGA packaging is that it can be supported with existing placement and assembly equipment. BGAs also offer significantly more misalignment tolerance and less susceptibility to co-planarity issues. Even if the solder paste is misaligned or the device is slightly offset, the BGA self-centers during the reflow process. This is due to the surface tension of the solder and flux in its molten state pulling each ball into the center of the pad.

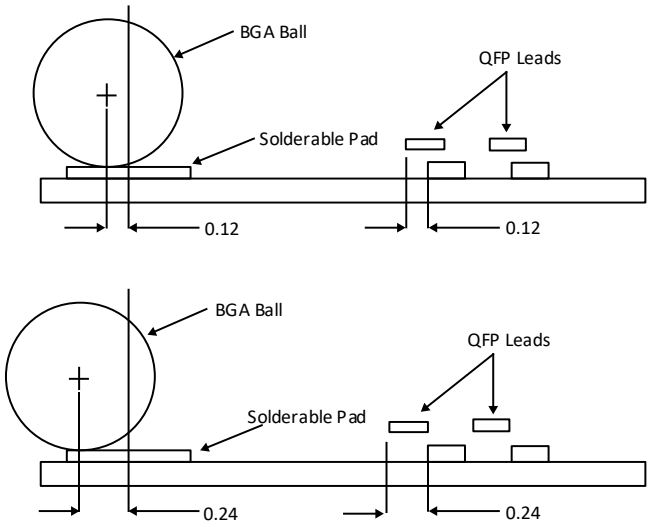


Figure 7.1. Misalignment of BGA Balls vs. QPF Leads

Controlling the oven re-flow profile is one of the most important assembly parameters for consistent and reliable BGA placement. Profiles are typically tested on a pre-run. One or two panels are run to dial in the process, then visual and X-ray inspection equipment are used for verification.

BGA packages present numerous benefits previously unobtainable in surface mount packaging technology. BGAs provide higher pin counts in a much smaller area than was previous possible. No longer is the package design limited to connections along the periphery on the outside quadrants of the package edge like a PQFP or TQFP outline. Fully populated ball grid arrays with pitches as small as 0.4 mm are available.

Some BGA devices are arranged with de-populated interconnect near or around the center. These are dependent on the die size and number of pins. The area void of interconnect in the middle of the array has some advantages, it can be used for escape routing vias or tying directly to the ground or power planes.

Although the packages can be quite complex and densely populated, all of these packages receive strict quality and reliability testing and are widely accepted today by designers and PCB fabrication/assembly houses. All of this is due to advances in equipment and technology that have allowed a smooth transition into the assembly flow.

8. BGA Package Test and Assembly

How can a pad/ball/pin be tested that cannot be seen? All connections are hidden under the substrate at the ball interconnect, making it impossible to directly probe or test. To address this limitation, Lattice programmable devices provide JTAG, BSCAN, and boundary scan cells that allow electronic test and continuity of each pin with a boundary scan tester. This can be embedded into the system itself or driven externally from a high-speed test head. The boundary scan can test the pins or board for simple continuity tests or full functional test by shifting in test patterns through the JTAG port.

For debug or prototype boards it may be necessary to place test points, open vias, or pads to have access to a given set of pins in order to drive, over-drive or observe a given set of signals. These can be very small, as many pogo pin type probes are extremely small and can handle GHz range DC frequency. Zero ohm resistors are also commonly used in first-run boards as a way to gain access to a pad or pin.

After assembly, BGA solder point quality and integrity is visually inspected with X-ray technology as part of the fabrication process. A special X-ray machine can look through the plastic package, substrate and silicon to directly view the BGA solder balls, vias, traces and pads.

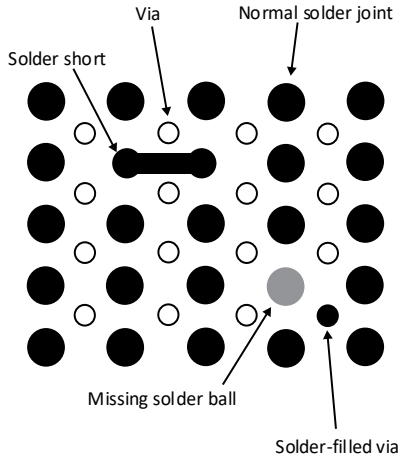


Figure 8.1. Example of How Defects May Appear in an X-Ray Image

The X-ray image in Figure 8.2 shows proper alignment; no voids or defects are noted. Balls, vias and traces are visible.

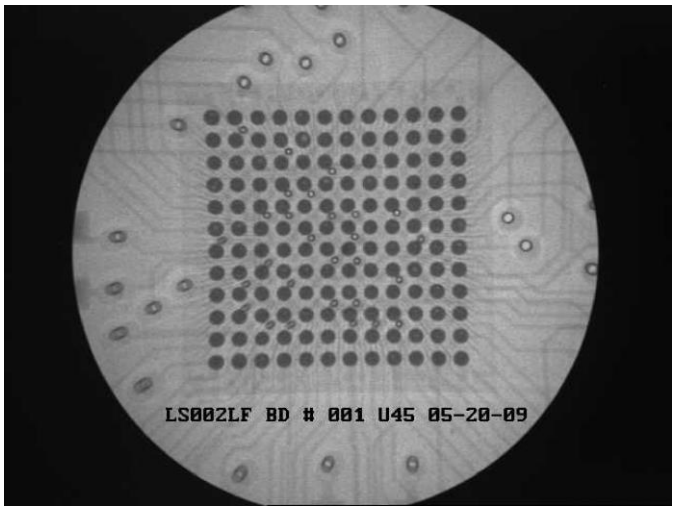


Figure 8.2. X-Ray Inspection Plot of ispMACH 4000ZE 144-Ball csBGA*

***Note**: Photo Courtesy of CEM, Ltd., www.cemltd.com

PCB cross-sectioning is another method used to verify BGA and PCB quality and reliability. After a new process has been developed or changed or when qualifying a new vendor, it is a good practice to get physical information from the vendor on their BGA reflow. When trace/space and drill or laser tolerances are nearing their limits, board yield can be as be as low as 50% for the bare board fab. Cross-sections give you a good idea if the process is correct but do not guarantee each batch or each board design behaves the same way due to layout dimensions, thermal issues, flux/paste and alignment, etc.

Figure 8.3 shows a BGA cross-section that uses a non-soldermask over bare copper-defined pad. (NSMD) pad.

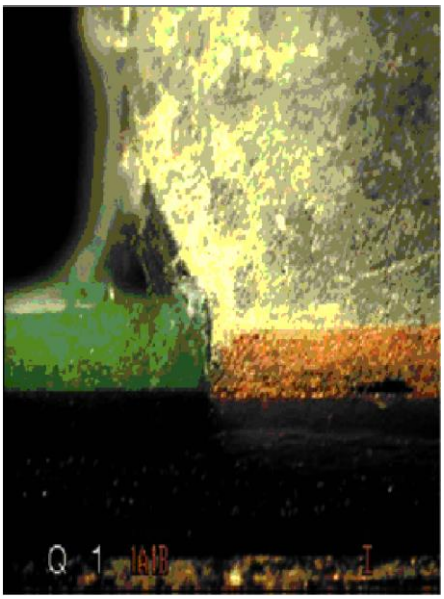


Figure 8.3. BGA Cross-Section

Figure 8.4 shows *offset* micro via stack routing between layers.

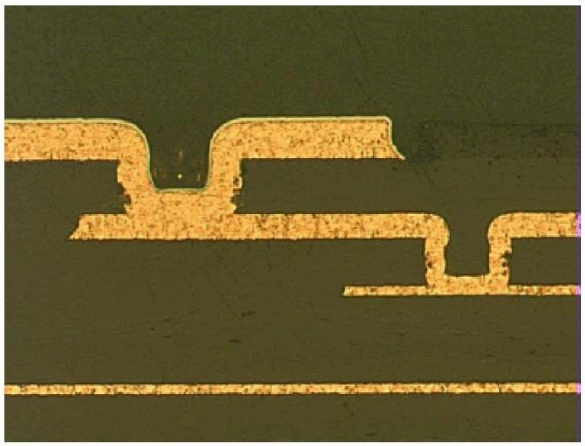


Figure 8.4. Cross-Section of Micro Vias

High-resolution video cameras are used for edge inspection to verify ball seating, distortion, solder wetting, flow, contaminates, etc. Figure 8.5 is a video view of a side/edge shot looking at BGA balls soldered down to the isp-MACH 4000ZE Pico Evaluation Board (www.latticesemi.com/4000ze-pico-kit), an FR4 4-layer PCB.

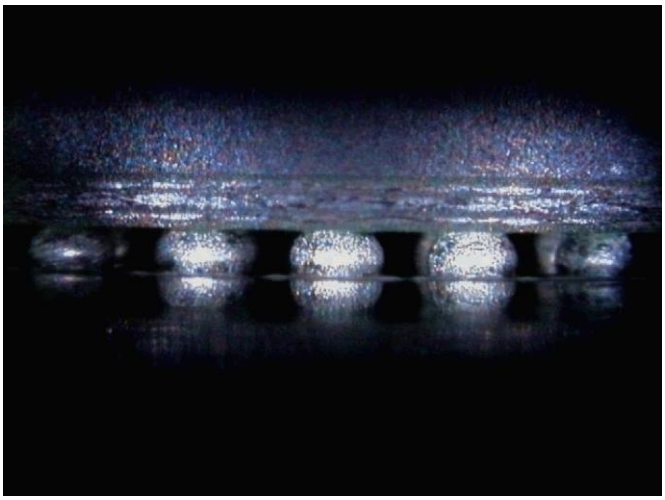


Figure 8.5. Edge View Camera Inspection

In the photos samples above, trained technicians and computer camera recognition equipment are used for inspection of the X-ray results, looking for voids, shorts, missing connections, contaminants, alignment or other gross failure mechanisms. For example, in Figure 8.5, the BGA ball connections appear to be squashed downward, with mild distortion, insuring that proper oven profile temperatures were achieved.

These technologies help in the successful placement and long term use of BGAs in the industry's latest products. Further advancements have been made in material content to conform to environmental issues, toxic materials and recycling. Another issue that relates to board design is the physical silkscreen logos and information related to recycling, lead content and other hazardous waste components, strict adherence must be paid to these requirements. Although a documentation and silkscreen issue, it can become a challenge to fit this information on the board in some cases due to component population and must be accounted for in overall board real estate.

9. PCB Design Support

Lattice provides a collection of PCB design resources at http://www.latticesemi.com/en/Products/DevelopmentBoardsAndKits including schematic libraries, PCB CAM viewers, technical notes, and BGA breakout and routing examples.

10. Use at Your Own Risk

Successful printed circuit manufacturing requires frequent communication with the printed circuit assembly house during design and layout. The examples shown here may or may not produce a successful or manufacturable design at your selected assembly house. Please review your iCE40 layout with your PCB assembly house before committing to a production run.

Technical Support Assistance

Submit a technical support case via www.latticesemi.com/techsupport.

Revision History

Revision 4.8, October 2021

Section	Change Summary
BGA Board Layout Recommendations	Updated Table 3.1. Lattice BGA Package SMD/NSMD Pad Opening. Under 0.80 mm Ball Pitch, modified the 121 caBGA Solder Mask Opening.
BGA Breakout and Routing Examples	Added 121-Ball caBGA BGA Breakout Example.

Revision 4.7, September 2021

Section	Change Summary
BGA Board Layout Recommendations	• Updated Table 3.1. Lattice BGA Package SMD/NSMD Pad Opening. Added 80 ckfBGA Under 0.65 mm Ball Pitch and updated 80 ctfBGA diameter. Added 324 caBGA under 0.80 mm Ball Pitch. • Updated Table 3.2. PCB SMD/NSMD Pad Recommendations. Added 80 ckfBGA under 0.65 mm Ball Pitch. Added 324 caBGA under 0.80 mm Ball Pitch.
BGA Breakout and Routing Examples	• Changed heading to ckfBGA/ctfBGA BGA Breakout Example and sub-heading to 80-Ball ckfBGA/ctfBGA BGA Breakout Example. Indicated specific packages for 7.0 mm × 7.0 mm and 6.5 mm × 6.5 mm.

Revision 4.6, August 2021

Section	Change Summary
Acronyms in This Document	Added FOWLCSP.
Introduction	Fixed the link to the Development Boards and Kits web page.
Lattice BGA Package Types	Added FOWLCSP.
BGA Board Layout Recommendations	• Updated Table 3.1. Lattice BGA Package SMD/NSMD Pad Opening. Added 672 fcBGA package under 1.00 mm Ball Pitch. Also combined 100 fpBGA with similar package types. Added 256 FOWLCSP package. • Added 256 FOWLCSP to Table 3.2. PCB SMD/NSMD Pad Recommendations
BGA Breakout and Routing Examples	• Added 672-Ball fcBGA Breakout Example. • Added 256-Ball FOWLCSP Breakout Example. • Fixed the link to the Development Boards and Kits web page.
PCB Design and Support	Fixed the link to the Development Boards and Kits web page.

Revision 4.5, June 2021

Section	Change Summary
BGA Board Layout Recommendations	Added 196 caBGA package to: • Table 3.1. Lattice BGA Package SMD/NSMD Pad Opening • Table 3.2. PCB SMD/NSMD Pad Recommendations.
BGA Breakout and Routing Examples	• Added 196-Ball caBGA BGA Breakout Example. • Reordered subsections.

Revision 4.4, October 2020

Section	Change Summary
BGA Board Layout Recommendations	Added 72 WLCSP package to: • Table 3.1. Lattice BGA Package SMD/NSMD Pad Opening • Table 3.2. PCB SMD/NSMD Pad Recommendations.
BGA Breakout and Routing Examples	Added 72-Bump WLCSP Breakout Example.

Revision 4.3, May 2020

Section	Change Summary
BGA Board Layout Recommendations	Added 289 csBGA package to: • Table 3.1. Lattice BGA Package SMD/NSMD Pad Opening • Table 3.2. PCB SMD/NSMD Pad Recommendations
BGA Breakout and Routing Examples	Added 289-Ball csBGA BGA Breakout Example.

Revision 4.3, May 2020

Section	Change Summary
BGA Board Layout Recommendations	Added 289 csBGA package to: • Table 3.1. Lattice BGA Package SMD/NSMD Pad Opening • Table 3.2. PCB SMD/NSMD Pad Recommendations
BGA Breakout and Routing Examples	Added 289-Ball csBGA BGA Breakout Example.

Revision 4.2, August 2019

Section	Change Summary
All	• Added Disclaimers section. • Fixed broken links. • Minor editorial changes.

Revision 4.1, March 2019

Section	Change Summary
All	Updated last page of the document.
BGA Breakout and Routing Examples	Added body size 7.0 mm × 7.0 mm in 80-Ball ctfBGA BGA Breakout Example section.

Revision 4.0, November 2018

Section	Change Summary
All	• Changed document number from TN1074 to FPGA-TN-02024. • Updated document template.
Lattice BGA Package Types	Moved this section.
BGA Board Layout Recommendations	General update
Revision History	Updated format.

Revision 3.9, March 2017

Section	Change Summary
BGA Board Layout Recommendations	Revised Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening. Added 484 caBGA under 0.8 mm Ball Pitch.
484-Ball caBGA BGA Breakout Example	Added this section.

Revision 3.8, January 2017

Section	Change Summary
BGA Board Layout Recommendations	Revised Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening. • Added 121 caBGA and 30 WLCSP under 0.4 mm Ball Pitch. • Added 400 caBGA under 0.8 mm Ball Pitch.
30-Ball WLCSP Breakout and Routing Example	Updated this section.

Revision 3.7, September 2016

Section	Change Summary
BGA Board Layout Recommendations	Revised Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening. • Changed Nominal BGA Package Solder Pad Diameter (mm) values of 0.35 mm Ball Pitch 16, 25, 36 WLCSP and 0.4 mm Ball Pitch 25 WLCSP and 36, 49, 81 WLCSP. • Added 0.65 mm Ball Pitch. • Added (Option 1) to 0.8 mm Ball Pitch 100, 256, 332 caBGA. • Added footnote 5.

Revision 3.6, May 2016

Section	Change Summary
64-Ball ucfBGA BGA Breakout and Routing Example	Added this section.

Revision 3.5, April 2016

Section	Change Summary
BGA Breakout and Routing Examples	Added the following sections: • 80-Ball ctfBGA BGA Breakout Example • 81-Ball csfBGA BGA Breakout Example • 36-Bump WLCSP Breakout Example 4

Revision 3.4, September 2016

Section	Change Summary
BGA Breakout and Routing Examples	• Added statement on capacitors at secondary layer. • Updated Figure 4.26. CAM Artwork Screen Shots, 285-Ball csfBGA.
Technical Support Assistance	Updated this section.

Revision 3.3, February 2015

Section	Change Summary
BGA Board Layout Recommendations	• Updated Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening. • Added 237 ftBGA package.
BGA Breakout and Routing Examples	• Added 237-Ball ftBGA BGA Breakout Example section. • Added breakout information for the CM36A package of the iCE40 Ultra device. • Added CM36A package to section heading. • Added CM36A package to introduction. • Added CM36A package to Table 5 caption. • Updated Figure 40 caption to Four-Layer Example Shown for CM36.

Revision 3.2, January 2015

Section	Change Summary
16-Bump WLCSP Breakout Example	Added information on iCE40 UltraLite device...

Revision 3.1, October 2014

Section	Change Summary
BGA Board Layout Recommendations	Updated Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening. Removed 20 WLCSP.
20-Bump WLCSP Breakout Example	Removed this section.

Revision 3.0, September 2014

Section	Change Summary
BGA Board Layout Recommendations	Updated Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening. Updated Figure 3.1. Device/Package (NSMD.
BGA Breakout and Routing Examples	Added the following sections: • 121-Ball csfBGA BGA Breakout Example • 256-Ball csfBGA BGA Breakout Example • 324-Ball csfBGA BGA Breakout Example • 256-Ball caBGA BGA Breakout Example • 324-Ball caBGA BGA Breakout Example • 400-Ball caBGA BGA Breakout Example • 36-Bump WLCSP Breakout Example 1 • 36-Bump WLCSP Breakout Example 2 • 49-Bump WLCSP Breakout Example 1 • 49-Bump WLCSP Breakout Example 2 • 81-Bump WLCSP Breakout Example 1 • 81-Bump WLCSP Breakout Example 2 Updated 36-Bump WLCSP Breakout Example 3 section title.

Revision 2.9, June 2014

Section	Change Summary
BGA Breakout and Routing Examples	Added the following sections: • 20-Bump WLCSP Breakout Example • 36-Bump WLCSP Breakout Example

Revision 2.8, April 2014

Section	Change Summary
BGA Board Layout Recommendations	Updated Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening. Added 0.5 mm ball pitch (285 csfBGA) and 8 mm ball pitch (756, 554,381 caBGA) packages. Updated Table 3.2. Added csfBGA package type.
BGA Breakout and Routing Examples	Added the following sections: • 285-Ball csfBGA BGA Breakout and Routing Example • 381-Ball caBGA BGA Breakout and Routing Example • 554-Ball caBGA BGA Breakout and Routing Example • 756-Ball caBGA BGA Breakout and Routing Example

Revision 2.7, February 2014

Section	Change Summary
BGA Board Layout Recommendations	Added Figure 3.1. Device/Package (NSMD.
BGA Breakout and Routing Examples	• Updated Table 4.2. iCE40 Package Layout Example Summary. • Changed “Pad Size” to “Solder Pad Size”. • Fixed typographical error (Via). • Changed “BGA Pad Size” to ““BGA Solder Pad Size” in various sections. • Updated Figure 4.50. Four-Layer CB81. • Updated Table 4.13. CB121, Six-Layer Layout Dimensions (Option 1). • Updated Figure 4.51. Six-Layer CB121 (Option 1). Deleted Internal Signal • Layer and Inner Signal Layer 2.

Revision 2.6, September 2013

Section	Change Summary
BGA Board Layout Recommendations	• Updated Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening to include 25 wlcsp and 1 6 wlcsp package options in 0.35 mm ball pitch. • Updated Table 3.2 to include 0.35 mm ball pitch for WLCSP package type.
BGA Breakout and Routing Examples	Added the following sections: • 332-Ball caBGA BGA Breakout Example • 30-Ball WLCSP Breakout and Routing Example • Layout Screen Shots, 30-Ball WLCSP, 0.40 mm Pitch • 25-Bump WLCSP Breakout and Routing Example 1 • 16-Bump WLCSP Breakout Example
Technical Support Assistance	Updated this section.

Revision 2.5, February 2013

Section	Change Summary
All	Included iCE40 product series.
BGA Board Layout Recommendations	Updated to include 184csBGA in Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening.

Revision 2.4, November 2012

Section	Change Summary
BGA Breakout and Routing Examples	Updated to include 328-Ball csBGA BGA Breakout and Routing Example.

Revision 2.3, August 2012

Section	Change Summary
BGA Breakout and Routing Examples	Updated Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening for iCE40 device support.

Revision 2.2, November 2012

Section	Change Summary
All	Updated document with new corporate logo.

Revision 2.1, October 2011

Section	Change Summary
BGA Breakout and Routing Examples	Replaced reference to 6-layer example with description of two 4-layer examples for 100-ball and 132-ball csBGA.

Revision 2.0, October 2011

Section	Change Summary
BGA Board Layout Recommendations	• Updated BGA Board Layout Recommendations text section. • Updated Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening. • Added WLCSP to Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening.

Revision 1.9, October 2011

Section	Change Summary
BGA Board Layout Recommendations	Added 64 csBGA to 0.5 mm pitch column to Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening.

Revision 1.8, August 2010

Section	Change Summary
BGA Board Layout Recommendations	Updated Table 3.1. Lattice Package SMD/NSMD Solder Pad Opening. • Specified nominal Solder Mask Opening for each Lattice BGA package • Clarified recommended Solder Mask Opening and Solder Pad Diameters • Added cautionary note.

Revision 1.7, March 2010

Section	Change Summary
Lattice BGA Package Types/ BGA Board Layout Recommendations	Replaced Lattice BGA Naming Conventions table with Lattice BGA Package Types table and SMD/NSMD Pad Recommendations table.

Revision 1.6, February 2010

Section	Change Summary
All	Edits to most sections and additional links and graphics added for each example.

Revision 1.5, May 2009

Section	Change Summary
Lattice BGA Package Types	Updated BGA Package Types table for 0.4 mm pitch ucBGA package.
BGA Board Layout Recommendations	Updated BGA Board Layout Recommendations table.

Revision 1.4, March 2008

Section	Change Summary
BGA Breakout and Routing Examples	Revised recommended Solder Mask Defined and Non Solder Mask Defined PCB solder pad dimensions to match industry standards.

Revision 1.3, September 2006

Section	Change Summary
BGA Package Types	Reformatted section in tabular format.
BGA Board Layout Recommendations	Added note to table.

Revision 1.2, June 2006

Section	Change Summary
All	Removed NSMD content.

Revision 1.1, November 2005

Section	Change Summary
All	Updated figures.

Revision 1.0, January 2005

Section	Change Summary
All	Initial release.

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