AN5307

Application note

Getting started with STM32H7A3/7B3 line and STM32H7B0 Value line microcontroller hardware development

Introduction

This application note is intended for system designers developing applications based on STM32H7A3/7B3 line and STM32H7B0 Value line microcontrollers (referred to as STM32H7A3/7B3/7B0 in this document), and provides an implementation overview of the following hardware features:

- Power supply
- Package selection
- Clock management
- Reset control
- Boot mode settings
- Debug management.

This document describes the minimum hardware resources required to develop an application based on the STM32H7A3/7B3/7B0 microcontrollers. It must be used as reference when starting a new design with these microcontroller lines.

1 General information

This document applies to the STM32H7A3/7B3/7B0 Arm®Cortex®-M7 based microcontroller lines.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Reference documents

Table 1. Referenced documents

Reference	Document title
[1]	• STM32H7A3xx, 32-bit Arm® Cortex®-M7 280 MHz MCUs, up to 2-Mbyte Flash memory, 1.4 Mbyte RAM, 46 com. and analog interfaces, SMPS. Datasheet (DS13195) • STM32H7B3xx, 32-bit Arm® Cortex®-M7 280MHz MCUs, 2-Mbyte Flash memory, 1.4-Mbyte RAM, 46 com. and analog interfaces, SMPS, crypto. Datasheet (DS13139) • STM32H7B0xx, 32-bit Arm® Cortex®-M7 280 MHz MCUs, 128-Kbyte Flash memory, 1.4-Mbyte RAM, 46 com. and analog interfaces, SMPS, crypto. Datasheet (DS13196).
[2]	STM32H7A3/B3 and STM32H7B0 Value line advanced Arm®-based 32-bit MCUs, reference manual (RM0455).
[3]	STM32H7A3xI/G, STM32H7B0xB and STM32H7B3xI device errata (ES0478).
[4]	Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs, application note (AN2867).
[5]	STM32 microcontroller system memory boot mode, application note (AN2606).
[6]	Migration guide from STM32F7 Series and STM32H743/H753 line to STM32H7A3/7B3 line devices, application note (AN5293).

2 Power supplies

2.1 Introduction

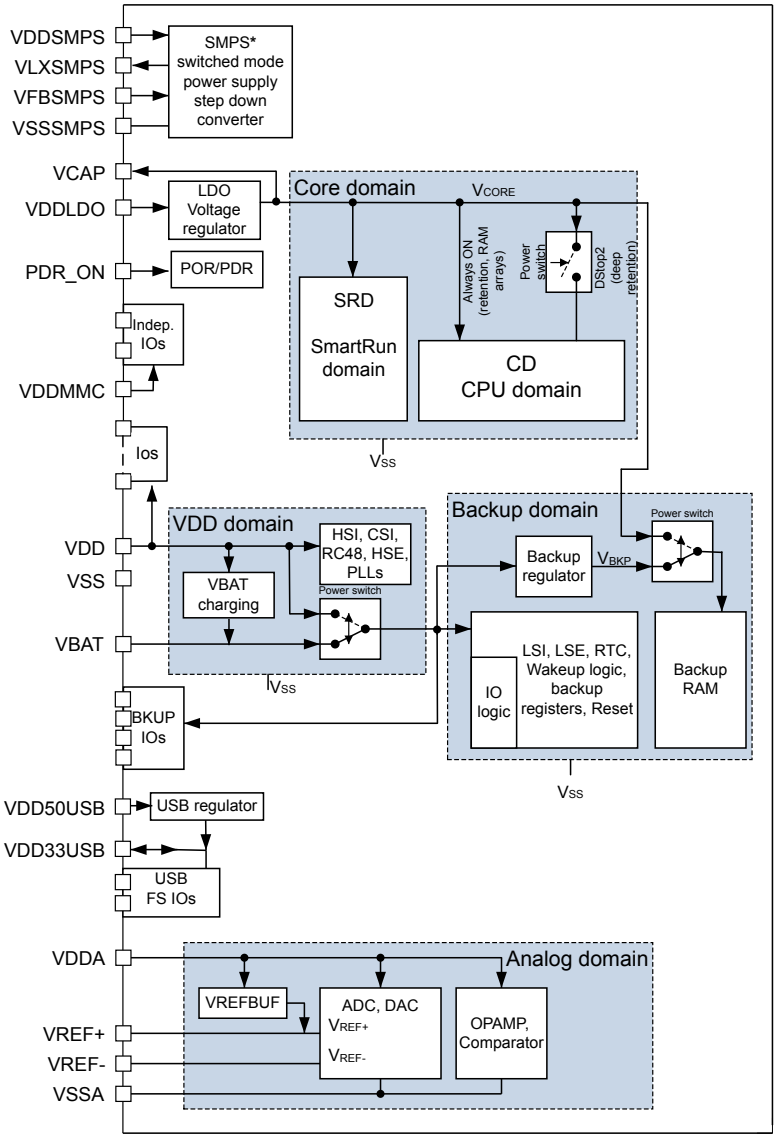
STM32H7A3/7B3/7B0 microcontrollers are a highly integrated microcontroller that combines the 32-bit Arm® Cortex®-M7 core running up to 280 MHz with up to 2 Mbytes dual-bank Flash memories and 1.4 Mbytes of RAM (including 192 Kbytes of TCM RAM, 1.18 Mbytes of user RAM and 4 Kbytes of backup SRAM).

STM32H7A3/7B3/7B0 microcontrollers require at least one single power supply to be fully operational.

Additional power supplies or voltage references are required for some use cases. The general design guidelines are explained in the following sections. The figure below illustrates the power supply layout.

In all the diagrams, the gray boxes represent power domains.

Figure 1. Power supplies



* The SMPS feature and four related pads are only available on SMT32H7A/BxxxxxQ devices.

Table 2. PWR input/output signals connected to package pins/ball

Pin name	Signal type	Description
VDD	Supply input	Main I/O and V_{DD} domain supply input.
VSS	Supply input	Main ground.
VDDA	Supply input	External analog power supply for analog peripherals.
VSSA	Supply input	Separated isolated ground for analog peripherals.
VBAT	Supply input/output	Backup battery supply: optional external supply for backup domain when V_{DD} is not present. Can also be used to charge the external battery.
VDDMMC	Supply input	Independent supply for some dedicated I/Os(1). Avoids external level shifters when these I/Os are operating at a supply level different from V_{DD}. Very useful for instance for SDCard HC and XC.
VDDSMPS	Supply input	Supply for switch mode power supply (SMPS) step down converter.
VLXSMPS	Supply output	SMPS step down converter output.
VFBSMPS	Supply regulation input	SMPS feedback voltage sense.
VSSSMPS	Supply input	Ground for SMPS step down converter.
VDDLDO	Supply input	Supply for the integrated low drop out regulator.
VCAP	Supply input/output	Figure 2. System supply configurations for devices with SMPS shows the different possible regulator supply configurations: using one, both or none. Digital Core supply input / output pin. Is either provided by the embedded regulator or from an external source.(2)
VDD50USB	Supply input	Supply for USB regulator.
VDD33USB	Supply input/output	Embedded USB regulator output or external USB supply when the internal regulator is not used.
VREF+	Supply input/output	Reference voltage for ADCs and DACs. Can be generated through the internal VREFBUF or provided by an external source.
VREF-	Supply input	Ground reference for ADCs and DACs.
PDR_ON	Digital input	Control signal to switch the integrated POR/PDR circuitry ON/OFF.

1. *PB8, PB9, PD6, PD7 and PG9 to PG14.*
2. *Refer to Figure 2. System supply configurations for devices with SMPS for the different possible configurations.*

Figure 2. System supply configurations for devices with SMPS

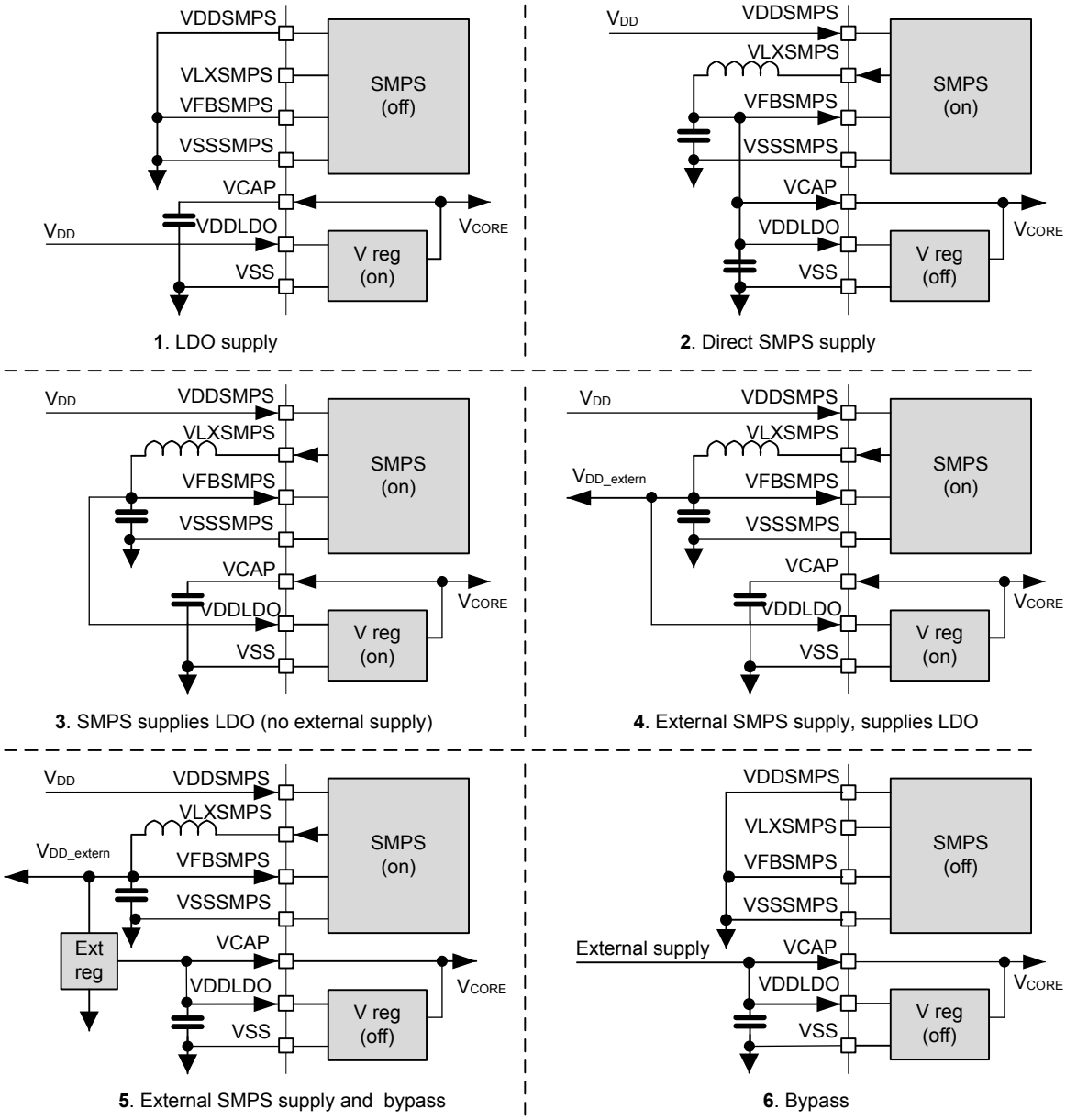
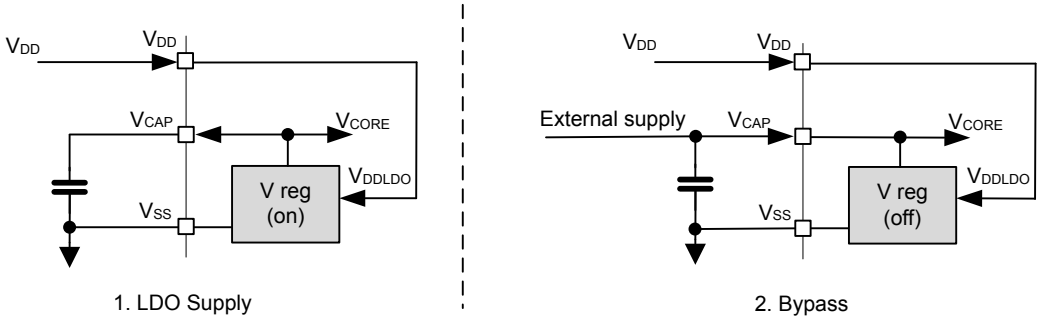


Figure 3. System supply configurations for devices without SMPS



2.1.1 External power supplies and components

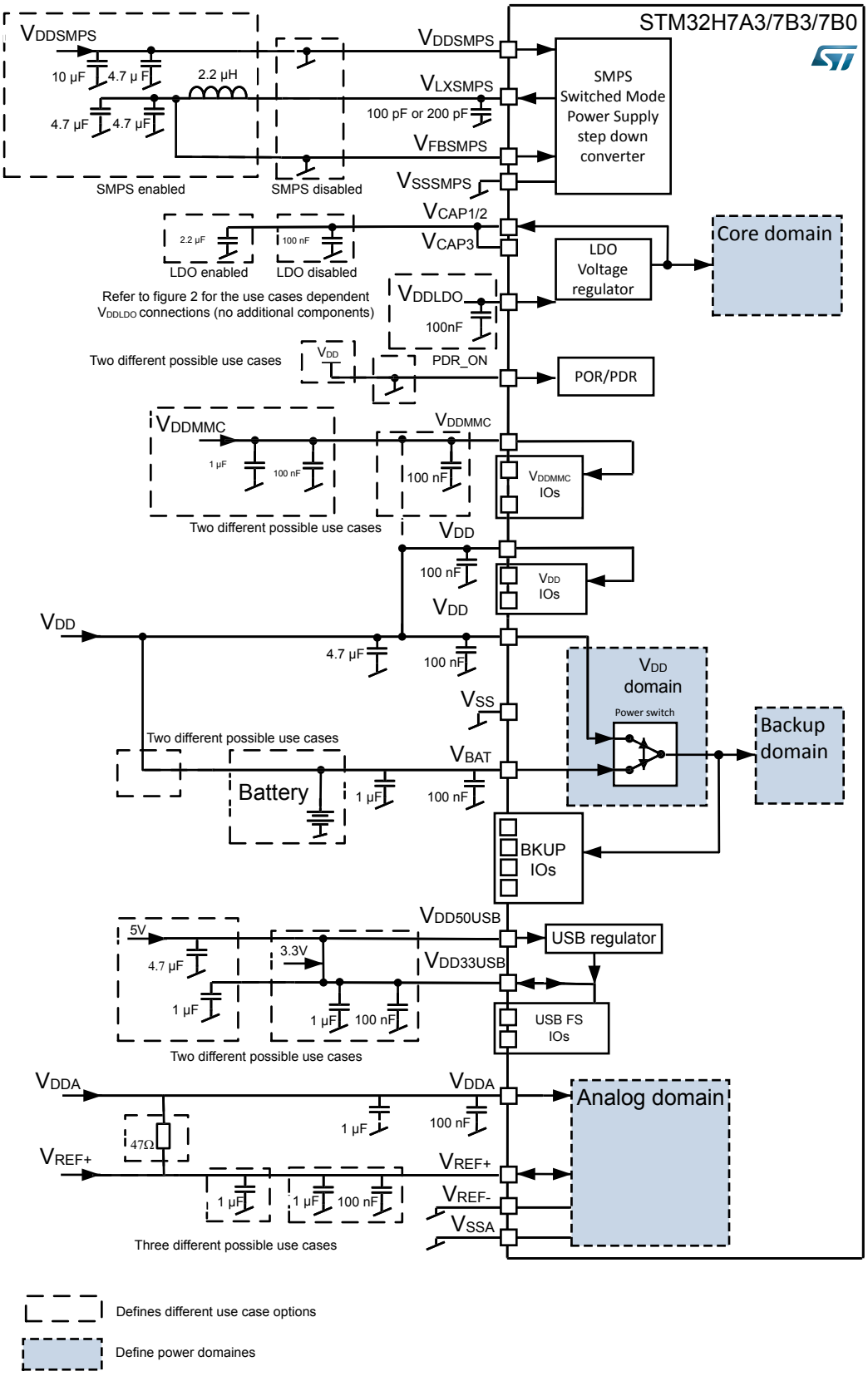
Refer to the STM32H7A3/7B3/7B0 datasheet for more details on the electrical characteristics.

Table 3. Power supply connection

Package pin/ ball	Voltage range	External components	Comments
VDD	1.62 to 3.6 V	100 nF ceramic, for each V_{DD} as close as possible to the pins. A 4.7 µF ceramic connected to one of the VDD pins.	For V_{DD} < 1.71 V the PDR must be disabled (see Section 2.2.1).
VDDA	1.62 to 3.6 V	1 µF ceramic and 100 nF as close as possible to the pin.	V_{DDA} can be connected to V_{DD} through a ferrite bead.
	1.8 to 3.6 V		Restriction if a DAC or VREFBUF is used.
	2.0 to 3.6 V		Restriction if an OPAMP used.
	0 to 3.6 V		DAC, ADC, OPAMP, COMP, VREFBUF are not used.
VBAT	1.2 to 3.6 V	1 µF ceramic and 100 nF close to the VBAT pin.	Can be connected directly to an external battery or supply. The external battery can be charged through the internal 5 kΩ or 1.5 kΩ resistor (see the reference manual RM0455 [2]. To be connected to V_{DD} when not used. When the PDR_ON pin is set to V_{SS} the VBAT pin must be connected to V_{DD} since this functionality is no longer available.
VDDMMC	1.2 to 3.6 V	1 µF ceramic and 100nF as close as possible to the pin.	Can be higher than V_{DD} supply. It should be tied to V_{DD} when this dedicated supply is not needed. Internally tied to V_{DD} when this pin is not present in a specific package. Some warnings are related to this supply, refer to Section 4 for more details.
VDDSMPS	1.62 to 3.6 V	Four different solutions advised: • 10 µF (best cost trade off), ESR 10mΩ • 2x 10 µF (best area/perf trade off) • 10 µF + 100 nF close from pin (best cost/perf trade off) • 10 µF + 4.7 µF (best perf).	VDDSMPS connected to V_{SS} when the converter is not used.
	2.3 to 3.6 V		For SMPS output regulated to 1.8 V. SMPS supplies the LDO regulator or an external regulator.
	3 to 3.6 V		For SMPS output regulated to 2.5 V. SMPS supplies the LDO regulator or an external regulator.
VLXSMPS	Vcore or 1.8 V or 2.5 V	When the SMPS is used: • 2.2 µH (DCR 110mΩ, I_{sat} 1.7 A, I_{temp} 1.4 A) as close as possible to VLXSMPS. • LQFP packages: 220 pF ceramic capacitor on VLXSMPS. • BGA package: 100 pF ceramic capacitor on VLXSMPS pin. • 2x 4.7 µF (ESR 5 mΩ) close to the inductor on VFBSMPS connection side.	Depending on the use case, the SMPS provides the digital core supply or a supply provided to another regulator (external or internal LDO). See Figure 2 for connection details.
VFBSMPS	Vcore or 1.8 V or 2.5 V	-	Refer to Figure 2 for the use case dependency of this pin.
VDDLDO	1.62 to 3.6 V	For each VDDLDOx pin: 100 nF close to the pin.	$V_{DDLDO} \leq V_{DD}$.

Package pin/ ball	Voltage range	External components	Comments
			Up to three VDDLDO pins available depending on the package specification.
VCAP	VOS0/VOS1/ VOS2/VOS3/ SVOS4/SVOS5	LDO enabled and SMPS enabled or disabled: 2.2 µF ESR < 100 mΩ for VCAP1 2.2 µF ESR < 100 mΩ for VCAP2 LDO disabled: 100 nF close to each VCAPx pin VCAPx connected together.	If the VCAP3 pin is available (depending on the package), it must be connected to the other VCAP pins but no additional capacitance is required. In bypass mode the Vcore supply is externally provided through the VCAPx pins.
VDD50USB	4.0 to 5.5 V	4.7 µF ceramic.	Connected to an external supply or USB VBUS for an internal USB regulator use case. Connected to VDD33USB when the internal USB regulator is not used (for packages having this pin available).
VDD33USB	3.0 V to 3.6 V	1 µF ceramic and 100 nF ceramic (USB reg not used) 1 µF max ESR 600 mΩ (USB reg used).	The VDD33USB supply can be provided externally or through the internal USB regulator. When the regulator is enabled its output is provided directly to the VDD33USB through the internal connection. This pin is internally tied to V_{DD} when it is not present in some specific packages. In consequence, the V_{DD} supply level must be compliant with VDD33 if the USB is used for these packages.
	0 V to 3.6 V	-	When USB is not used.
VREF+	1.62 V to ≤ VDDA	1 µF ceramic and 100 nF ceramic close to the pin or connected to VDDA through a resistor (typically 47 Ω).	VREF+ is provided externally. In some packages, the VREF+ pin is not available (internally connected to V_{DDA}).
	2 V to ≤ VDDA		External VREF+ with V_{DDA}>2 V and ADC used.
	VREFBUF spec	1 µF	VREF+ is provided by the embedded VREFBUF regulator. Important do not activate the internal VREFBUF when VREF+ is provided externally.
VREF-	VSSA	Tied to VSSA	Only available in some packages Internally tied to V_{SSA} when this pin is not present.
PDR_ON	VDD or VSS	Tied to VDD	Power-on reset (POR) and power-down reset (PDR) circuit switched ON Internally tied to V_{DD} when this pin is not present in a specific package. V_{DD}: 1.71 to 3.6 V.
		Tied to VSS	POR and PDR circuit switched off V_{DD}: 1.62 to 3.6 V.

Figure 4. Power supply component layout



2.1.2 Digital circuit core supply (V_{CORE})

As shown in Figure 2. System supply configurations for devices with SMPS, the digital power can be supplied either by the internal linear voltage regulator, the embedded SMPS step down converter or directly by an external supply voltage (regulator bypass). The SMPS step down converter can also be cascaded with the linear voltage regulator.

This digital core voltage can be set dynamically to the required performance (voltage scaling VOS0 to VOS3).

In system stop mode, the digital core voltage can be reduced to improve the power consumption (voltage scaling SVOS3 to SVOS5). Further optimization can be achieved by switching off the unused SRAM instances.

The DStop2 is a new mode for the digital core in the CPU domain. In this mode, part of the core domain is switched off but the content is kept. This includes memory and register settings (see switch in Figure 1. Power supplies).

For a detailed definition on the available power modes please read the power control (PWR) chapter of the STM32H7A3/7B3/7B0 reference manual [2].

2.1.3 Independent analog supply and reference voltage

To improve analog peripheral performance, the analog peripherals feature an independent power supply which can be separately filtered and shielded from noise on the PCB:

- the analog supply voltage input is available on a separate VDDA pin
- An isolated ground connection is provided on the VSSA pin.

To ensure better ADC and DAC accuracy, the reference voltage can be provided externally through the VREF+ pin, this however is not available in all packages.

The VREF– pin is available on some packages to improve the ground noise immunity.

The V_{DDA} minimum value (V_{DDA_MIN}) depends on the analog peripheral and on whether a reference voltage is provided or not, refer to Table 3 for more details.

2.1.4 Independent USB transceiver power supply

There are different ways to supply the USB transceivers, depending on $V_{DD33USB}$ and $V_{DD50USB}$ availability.

When the VDD50USB pin is available, it can be used to supply an internal regulator dedicated to the USB transceivers. In this case:

- Either the USB VBUS or an external power supply can be used to provide the required voltage.
- The internal regulator output supply is connected to the USB FS PHY and is also available on the VDD33USB pin (see Figure 1. Power supplies).
- The $V_{DD50USB}$ voltage can rise either before or after the V_{DD} power supply (see Figure 7. VDD50USB power supply).
- An external capacitor must be connected to VDD33USB (see Table 2. PWR input/output signals connected to package pins/ball).

When the VDD33USB pin is available, it can be used to supply the internal transceiver. In this case:

- The VDD33USB pin should receive a voltage ranging between 3.0 to 3.6 V. If the VDD50USB pin is available and the internal USB regulator is not used, $V_{DD50USB}$ must be connected with the VDD33USB pin. For example, when the device is powered at 1.8 V, an independent 3.3 V power supply can be applied to $V_{DD33USB}$.
- When $V_{DD33USB}$ is connected to a separate power supply, it is independent from V_{DD} and V_{DDA}. In this case, it must be the last supply to be turned on and the first supply to be switched off. The following conditions must be respected (see Figure 6. VDD33USB connected to external power supply):
  - During the power-on and power-down phases (V_{DD} < V_{DD} minimum value), $V_{DD33USB}$ should always be lower than V_{DD}.
  - $V_{DD33USB}$ rising and falling time specifications must be adhered to (refer to table power-up/power-down operating conditions for regulator on and table power-up/power-down operating conditions for regulator off provided in theSTM32H7A3/7B3/7B0 datasheets [1]).
- In operating mode, $V_{DD33USB}$ can be either lower or higher than V_{DD}.
- If a USB interface is used (USB OTG_HS / OTG_FS), the associated GPIOs powered by $V_{DD33USB}$ operate between $V_{DD33USB\_MIN}$ and $V_{DD33USB\_MAX}$. (See Figure 6.)

On some packages neither the VDD33USB pin, nor the VDD50USB pin are available, it is the VDD pin which supplies the $V_{DD33USB}$ through an internal connection. In this case, V_{DD} is constrained by $V_{DD33USB}$ and must range between 3.0 V and 3.6 V.

Figure 5. VDD33USB connected to V_{DD} power supply

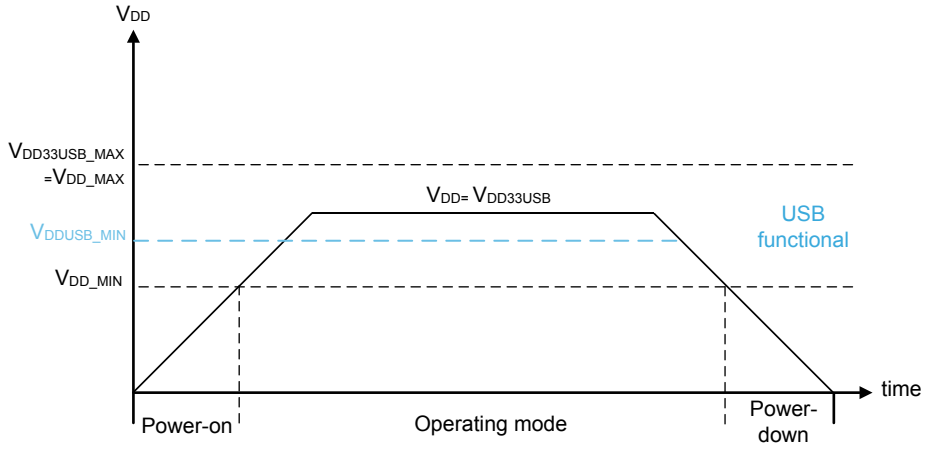


Figure 6. VDD33USB connected to external power supply

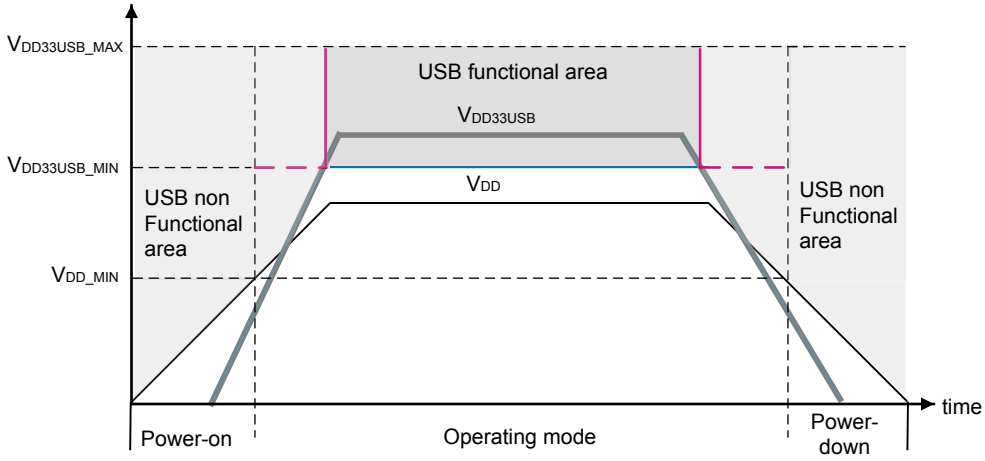
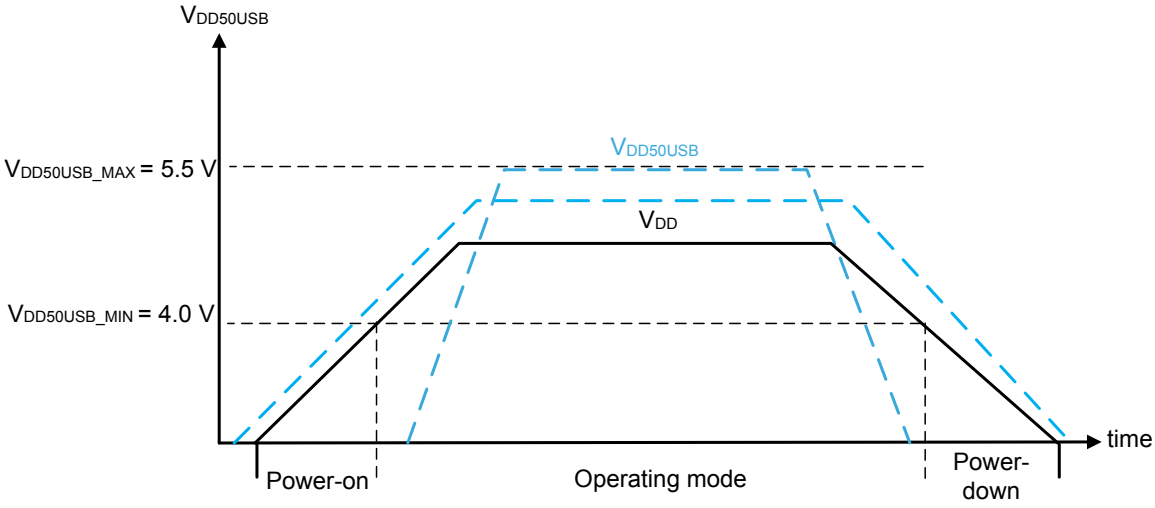


Figure 7. VDD50USB power supply



2.1.5 Battery backup domain

Backup domain description

To retain the content of the RTC backup registers, Backup SRAM, and supply the RTC when V_{DD} is turned off, the VBAT pin can be connected to an optional 1.2 to 3.6 V standby voltage supplied by a battery. Otherwise, VBAT must be connected to another source, such as V_{DD}.

When the Backup domain is supplied by V_{BAT} (analog switch connected to V_{BAT} since V_{DD} is not present), the following functions are available:

- PC14 and PC15 can be used for the LSE pins only
- PC13 can be used as tamper pin (TAMP1)
- PI8 can be used as tamper pin (TAMP2)
- PC1 can be used as tamper pin (TAMP3).

During $t_{RSTTEMPO}$ (delay at V_{DD} start-up) or after a Power-Down Reset (PDR) is detected, the power switch between V_{BAT} and V_{DD} remains connected to VBAT.

During the start-up phase, if V_{DD} is established during $t_{RSTTEMPO}$ and is greater than V_{BAT} + 0.6 V, a current may be injected into the VBAT pin through an internal diode connected between V_{DD} and the power switch (V_{BAT}). If the power supply/battery connected to the VBAT pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the VBAT pin.

Refer to the relevant STM32H7A3/7B3/7B0 datasheet [1] for the actual value of $t_{RSTTEMPO}$.

Battery charging

When V_{DD} is present, the external battery connected to VBAT can be charged through an internal resistance. This operation can be performed either through an internal 5 kΩ or 1.5 kΩ resistor. The resistor value can be configured by software.

Battery charging is automatically disabled in V_{BAT} mode.

2.1.6 LDO voltage regulator

The low drop out (LDO) voltage regulator is always enabled after reset. For system supply configurations where this regulator is not needed, it is switched OFF by the user software after system start-up.

For the configuration where V_{CORE} is supplied by the LDO, the default output level is set to 1.0 V (VOS3). Refer to Figure 2. System supply configurations for devices with SMPS for more details.

The LDO can be set to one of four different modes depending on the application's operating modes:

- Switched OFF:
  - V_{CORE} is supplied externally through the VCAP pin (bypass mode).
  - Or V_{CORE} is supplied through the SMPS step down converter (see Section 2.1.7 SMPS step down converter).
- In Run mode:
  - The LDO regulator supplies the core and the backup domains.
  - The LDO regulator output voltage can be dynamically scaled by programming the voltage scaling (VOS0 to VOS3) depending on the required performance (see the STM32H7A3/7B3/7B0 reference manual [2]).
- In Stop mode :
  - The LDO regulator output level is reduced to the state programmed before entering stop mode (SVOS3 to SVOS5). The register and the SRAM content is kept.
  - For SVOS3, further power reduction can be achieved by setting the regulator in low power deep sleep mode (for SVO4 and SVOS5 the low power deep sleep mode is set automatically).
- In Standby mode:
  - The regulator is powered down. The registers and SRAM content are lost except for those related to the standby circuitry and the backup domain.

2.1.7 SMPS step down converter

The embedded switch mode power supply (SMPS) step down converter has a higher efficiency than the embedded LDO regulator.

By using the SMPS, the overall system power consumption is improved for all power modes at the extra cost of two additional external components (Inductor and low ESR capacitor).

Refer to the relevant STM32H7A3/7B3/7B0[1] datasheet to compare power efficiencies.

See Figure 2. System supply configurations for devices with SMPS for the possible configurations.

The SMPS step down converter is always enabled after reset when it's power supply is provided on the VDDSMPS pin.

The regulated output at start-up is 1.2 V.

The three main SMPS configurations are:

- The SMPS is used but the V_{CORE} supply is provided by the internal LDO regulator.

  After start-up the SMPS can be set by software to provide a regulated output of 1.8V or 2.5 V.
- The SMPS is used but the V_{CORE} supply is provided by an external regulator.

  After start-up the SMPS can be set by software to provide a regulated output of 1.8 V or 2.5 V. The external regulator must ensure the correct voltage scaling for the run and stop modes (VOSx and SVOSx).
- The SMPS is directly connected to the VCAP pin and provides the regulated supply to V_{CORE}.

  In this configuration, the SMPS runs in one of the following modes:
  - Run mode:
    - The converter can be dynamically scaled by programming the voltage scaling (VOS0 to VOS3) to the required performance (see the STM32H7A3/7B3/7B0 reference manual [2]).
  - In Stop mode:
    - The converter output level is reduced to the state programmed before entering stop mode (SVOS3 to SVOS5). The register and SRAM content is kept
    - For SVOS3, a further power reduction can be achieved by setting the converter in low power mode (for SVO4 and SVOS5 the low-power mode is always set automatically).
  - In Standby mode:
    - The converter is powered down. Both the register and SRAM content is lost except for the content related to the standby circuitry and the backup domain.

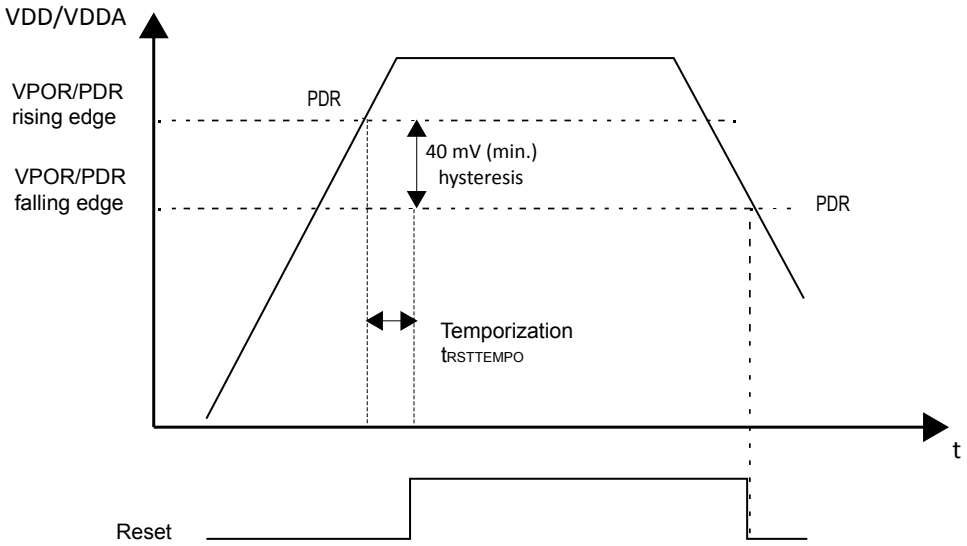
2.2 Reset and power supply supervisor

2.2.1 Power-on reset (POR)/power-down reset (PDR)

The devices have an integrated POR/PDR circuitry which ensures correct operational start-up from 1.71 V.

The device remains in reset mode while V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit as illustrated in Figure 8. For more details concerning the POR/PDR threshold, refer to the electrical characteristics the applicable STM32H7A3/7B3/7B0 datasheet [1].

Figure 8. Power on reset/power down reset waveform



For the $t_{RSTTEMPO}$ and V_{POR}/V_{PDR} threshold value refer to the *Reset and power control block characteristics* table in the applicable STM32H7A3/7B3/7B0 datasheet [1].

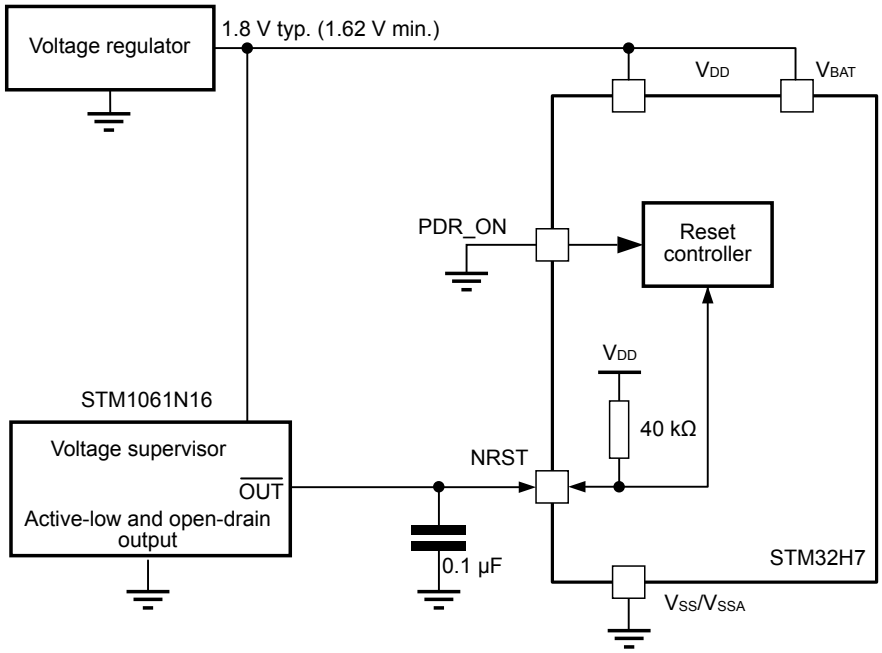
For packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On other packages, the power supply supervisor is always enabled.

The power supply supervisor is switched off by connecting the PDR_ON pin to V_{SS}, required to run the devices at V_{DD} < 1.71 V.

In this case, an external power supply supervisor has to monitor V_{DD} and control the NRST pin.

The device must be maintained in reset mode as long as V_{DD} is below 1.62 V. The implemented circuit is illustrated in Figure 9. Power supply supervisor interconnection with internal reset OFF.

Figure 9. Power supply supervisor interconnection with internal reset OFF



The supply ranges which never go below the 1.71 V are managed more effectively using the internal circuitry (no additional components are needed, thanks to the fully embedded reset controller).

When the embedded power supply supervisor is off, the following integrated features are no longer supported:

- the brown out reset (BOR) circuitry must be disabled
- the embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no longer available and VBAT pin must be connected to V_{DD}.

2.2.2 Brownout reset (BOR)

If enabled through the option bytes, the BOR keeps the system under reset until the V_{DD} supply voltage reaches the selected V_{BOR} threshold (also selected through option bytes, see the STM32H7A3/7B3/7B0 reference manual [2]).

Three BOR levels are possible (2.1 V, 2.4 V, 2.7 V). See the applicable STM32H7A3/7B3/7B0 dataseet [1] for the electrical characteristics.

2.2.3 Programmable voltage detector (PVD)

The PVD can be used to monitor the V_{DD} power supply by comparing it to a threshold selected by the `PLS[2:0]` bits in the PWR power control register (PWR_CR1).

The PVD is enabled by setting the PVDE bit.

The selectable threshold is between 1.95 V and 2.85 V (see the STM32H7A3/7B3/7B0 reference manual [2]).

A PVDO flag is available in the PWR power control/status register (PWR_CSR1), to indicate if V_{DD} is higher or lower than the PVD threshold. This event is internally connected to the EXTI line16 and can generate an interrupt if enabled through the EXTI registers.

The PVD output interrupt can be generated when V_{DD} drops below the PVD threshold and/or when V_{DD} rises above the PVD threshold depending on EXTI line16 rising/falling edge configuration. As an example, the service routine could perform emergency shutdown tasks.

2.2.4 Analog voltage detector (AVD)

The AVD can be used to monitor V_{DDA} power supply by comparing it to a threshold selected through the ALS[1:0] bits of the PWR power control register (PWR_CR1). The threshold value can be configured to 1.7, 2.1, 2.5 or 2.8 V (refer to the relevant STM32H7A3/7B3/7B0 datasheet [1] for the actual values).

The AVD is enabled by setting the AVDEN bit in PWR_CR1 register. An interrupt can be raised when V_{DDA} goes above or below the configured threshold.

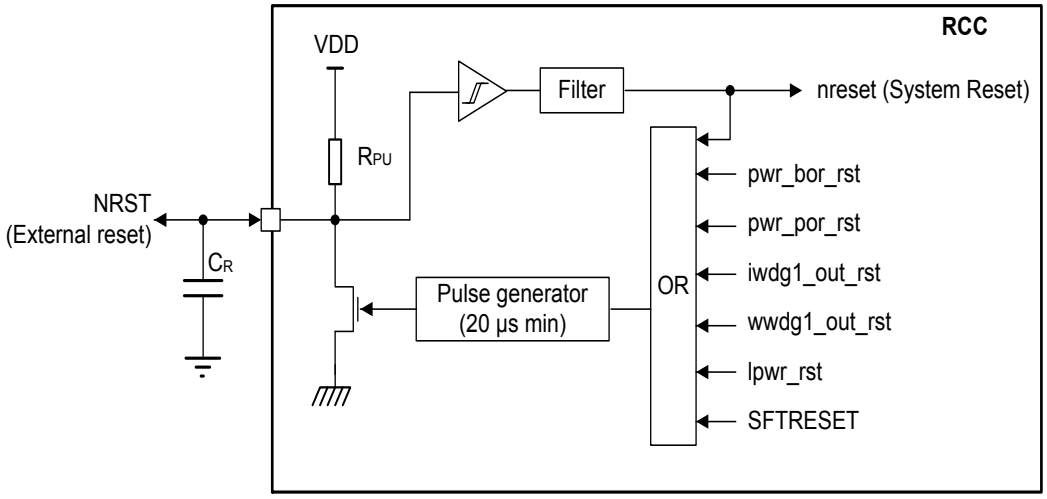
2.2.5 System reset

A system reset sets all the registers to their default values except the reset flags in the clock controller RCC_RSR register and the registers in the backup domain (see Figure 10).

A system reset is generated when one of the following events occurs:

1. A low level on the NRST pin (external reset)
2. Window watchdog end of count condition (WWDG reset)
3. Independent watchdog end of count condition (IWDG reset)
4. A software reset (Software reset)
5. A low-power management reset.

Figure 10. Reset circuit



2.2.6 Bypass mode

The power management unit is configurable by software with the option to bypass. When bypassed, the core power supply should be provided through VCAPx pins connected together.

In Bypass mode, the internal voltage scaling is not managed internally, and the external voltage value (1.0 to 1.3 V) must be consistent with the targeted maximum frequency (see the applicable STM32H7A3/7B3/7B0 datasheet [1] for the actual VOS level).

In Stop mode, it can be lowered to between 0.74 and 1.0 V (see datasheet for the actual SVOS level).

In Standby mode, the external source is switched off and the V_{CORE} domains powered down. The external source is switched on when exiting Standby mode.

In Bypass mode, the external voltage must be present before or at the same time as V_{DD}. To avoid conflict with the LDO, the external voltage must be kept above 1.15 V until the LDO is disabled by software.

3 Clocks

3.1 Introduction

STM32H7A3/7B3/7B0 microcontrollers support several possible clock sources:

- Two external oscillators (this requires external components):
  - High-speed external oscillator (HSE)
  - Low-speed external oscillator (LSE).
- Four internal oscillators:
  - High-speed internal oscillator (HSI)
  - High-speed internal 48 MHz oscillator (HSI48)
  - Low-power internal oscillator (CSI)
  - Low speed internal oscillator (LSI).
- Three embedded PLLs can be used to generate the high frequency clocks for the system and peripherals.

For both the HSE and LSE, the clock can also be provided from an external source using the OCS_IN and OSC32_IN pins (HSE bypass and LSE bypass modes).

The Figure 11. Clock generation and clock tree schematic shows the clock generation and clock tree architecture.

For detail explanation refer to the STM32H7A3/7B3/7B0 reference manual [2].

The choice of clocks depends strongly on the application use case .

Refer to the applicable STM32H7A3/7B3/7B0 datasheet [1] for the electrical characteristics (range and accuracy).

Figure 11. Clock generation and clock tree

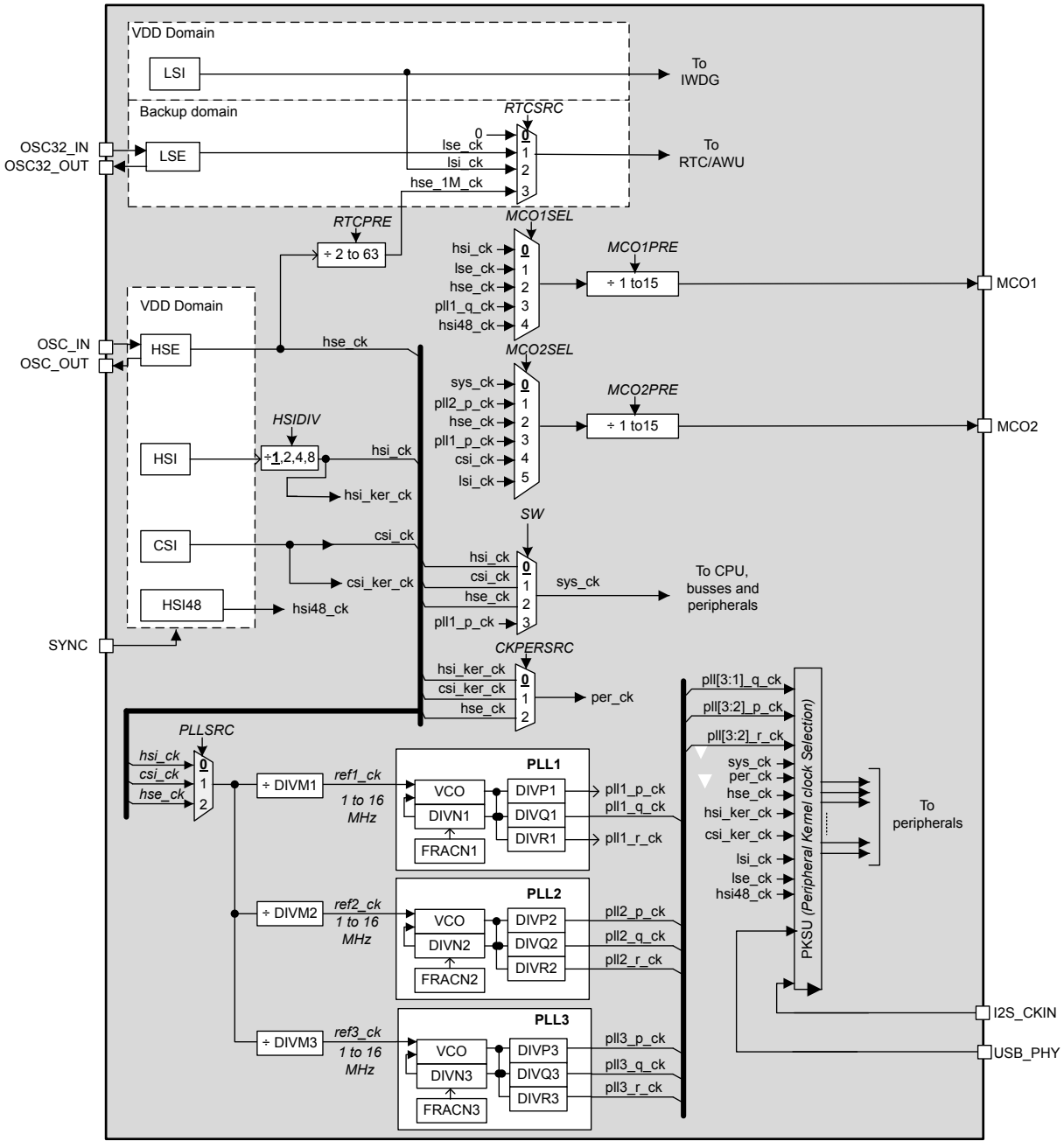


Table 4. Clock connections

Pin	External Component	Comment
OSC32_IN	External clock input[1][2]	LSE oscillator input (see Figure 12. HSE/LSE clock source). LSE bypass input f ≤ 1 MHz.
OSC32_OUT	LSE oscillator output[1][2]. Unconnected in Bypass mode.	The external capacitor must be tuned because it is strongly dependent on the PCB design. Not used in Bypass mode.
OSC_IN	External clock input[2][3]	HSE oscillator input (see Figure 12. HSE/LSE clock source). HSE bypass input 4 MHz ≤ f ≤ 50 MHz.
OSC_OUT	HSE oscillator output[2][3]. Unconnected in Bypass mode.	HSE oscillator output. The external cap must be tuned because it is strongly dependent on the PCB design. Not used in Bypass mode.
I2S_CKIN	External clock input	External kernel clock input for audio interface SAI, DFSDM, I2S. When an external clock reference is needed.
USB_PHY	External clock input	USB clock provided by the external PHY. The embedded PHY supports FS. For HS an external PHY needs to be used.
MCO1	Internal clock output	Some internal clocks can be provided to MCO1 pin. An embedded divider allows frequency reduction. See Figure 11. Clock generation and clock tree.
MCO2	Internal clock output	Some internal clocks can be provided to MCO2 pin. An embedded divider allows frequency reduction. See Figure 11. Clock generation and clock tree.
SYNC	External sync signal	Synchronization source for the HSI48MHz embedded oscillator clock recovery system (CRS). One of the three possible sync signal, see the STM32H7A3/7B3/7B0 reference manual [2].

1. *Typical example: (LSE), crystal: 32.768 kHz (6 pF, 50 kΩ), capacitor: 2 x 1.5 pF. All components to be placed as close as possible from the pins.*
2. *See application note, AN2867[4].*
3. *Typical example: (HSE), crystal: 24 MHz (6 pF, 80 Ω), capacitor: 2 x 33 pF. All components to be placed as close as possible from the pins.*

Figure 12. **HSE/LSE clock source**

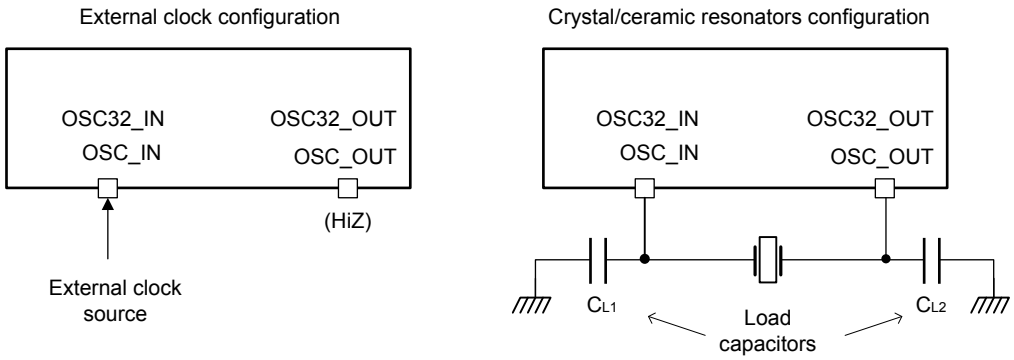


Table 5. **Clock source generation**

Source	frequency range	external component	Comments
HSE	4 to 50 MHz	Yes	High-speed external clock. Used when a very accurate high speed clock is needed.
LSE	32.768 kHz (max 1 MHz)	Yes	Low-speed external clock. Used when a very accurate low speed clock is needed, for instance for the real time clock (RTC).
HSI	8/16/32/64 MHz	No	High-speed internal clock. Default system clock after a reset.
HSI48	48 MHz	No	High-speed internal 48 MHz clock. Kernel clock for some peripherals. High-precision clock for USB with clock-recovery system, which can use the USB SOF signal.
CSI	4 MHz	No	Low-power internal oscillator. Faster start-up time than HIS. Can be used for wake-up from Stop mode
LSI	32 kHz	No	Low-speed internal clock, for independent watchdog (IWDG), RTC and auto-wakeup unit (AWU). This clock can run in Stop or Standby modes.
PLL	2 to 16 MHz input	No	Wide-range mode
	1 to 2 MHz input		Low-range mode. Some specific frequencies obtained with integer ratio, which may be needed for some application (for example audio).
	192 to 836 MHz VCO output		Integer or fractional ratios supported for all PLLs.

To optimize power consumption, each clock source can be switched on or off independently when it is not used.

Refer to the STM32H7A3/7B3/7B0 reference manual [2] for a detailed description of the clock tree. This document provides a complete view of clock usage by peripheral is provided in the Kernel clock distribution overview.

- **HSE and LSE bypass (external user clock)**

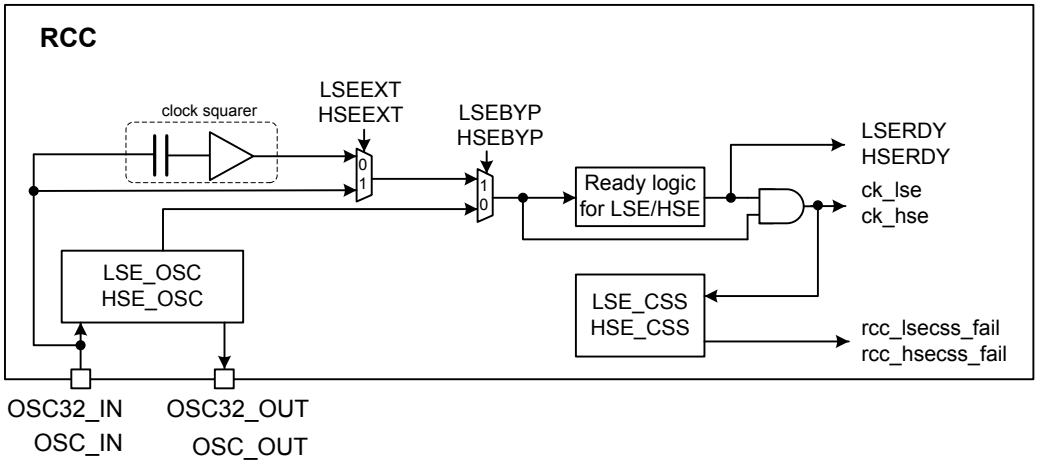
  In this mode, an external clock source must be provided to OSC_IN/OSC32_IN pins. The external clock can be either low swing (analog) or digital.

  The clock squarer is required for low swing clocks.

  Figure 13 shows the three solutions for the HSE/LSE:

  - External crystal (HSE_OSC/ LSE_OSC)
  - Bypass with external digital clock, directly taken from the pin without clock squarer
  - Bypass with external low swing clock, directly taken from the pin with clock squarer.

Figure 13. HSE/LSE bypass



- **External crystal/ceramic resonator (HSE crystal)**

  The external oscillator has the advantage of producing a very accurate main clock.

  Using a 25 MHz oscillator is a good choice for accurate USB OTG high-speed peripheral, I2S and SAI.

  The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize the output distortion and start-up stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

  For CL1 and CL2, use high-quality ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high-frequency applications and selected to meet the requirements of the crystal or resonator. CL1 and CL2 are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of CL1 and CL2. The PCB and MCU pin capacitances must be included when sizing CL1 and CL2 (10 pF can be used as a rough estimate for the combined pin and board capacitance).

  The HSERDY flag in the RCC clock control register (RCC_CR) indicates if the high-speed external oscillator is stable or not. At start-up, the clock is not provided until this bit is set by hardware. An interrupt can be generated if enabled in the RCC clock interrupt register (RCC_CIR).

  If it is not used as clock source, the HSE oscillator can be switched off by means of the HSEON bit in the RCC clock control register (RCC_CR).

3.2 LSE oscillator clock

The advantage of using an external oscillator, it provides a low-power highly accurate clock source needed for real-time clock (RTC), clock/calendar and other timing functions.

The LSE crystal oscillator has a configurable driving capability. This capability is chosen according to the external resonator component to insure stable oscillation

The driving capability is set through the LSEDRV [1:0] in RCC_BDCR register:

- 00: Low drive
- 10: Medium low drive
- 01: Medium high drive
- 11: High drive.

The LSERDY flag in the RCC backup domain control register (RCC_BDCR) indicates whether the LSE crystal is stable or not. At start-up, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the RCC clock interrupt register (RCC_CIER).

The LSE oscillator is switched on and off by programming the LSEON bit in RCC backup domain control register (RCC_BDCR).

3.3 Clock security system (CSS)

The device provides two clock security systems (CSS), one for HSE oscillator and one for LSE oscillator. They can be independently enabled by software.

When the clock security system on HSE is enabled, the clock detector is activated after the HSE oscillator start-up delay, and disabled when this oscillator is stopped:

- If the HSE oscillator is used directly or indirectly as the system clock. Indirectly meaning that it is used as PLL input clock, and the PLL clock is the system clock. When failure is detected, the system clock switches to the HSI oscillator and the HSE oscillator is disabled.
- If a failure is detected on the HSE clock, this oscillator is automatically disabled, a clock failure event is sent to the break inputs of the advanced-control timers TIM1, TIM8, TIM15, TIM16, and TIM17 and a non-maskable interrupt is generated to inform the software of the failure (clock security system interrupt rcc_hsecss_it), allowing the MCU to perform the rescue operations needed. The rcc_hsecss_it is linked to the Arm® Cortex®-M7 NMI (non-maskable interrupt) exception vector.
- If the HSE oscillator clock was used as PLL clock source, the PLL is also disabled when the HSE fails.

The clock security system on LSE must be enabled only when the LSE is enabled and ready, and after the RTC clock has been selected through the RTCSRC[1:0] bits of RCC_BDCR register.

When an LSE failure is detected, the CSS on the LSE wakes the device up from all low-power modes except V_{BAT}. If the failure occurred in V_{BAT} mode, the software can check the failure detection bit when the device is powered on again. In all cases the software can select the best behavior to adopt (including disabling the CSS on LSE which is not automatic).

3.4 Clock recovery system (CRS)

The clock recovery system (CRS) is dedicated to the internal HSI48 RC oscillator.

The CRS is an advanced digital controller acting on the internal fine-granularity trim resulting in a very precise 48 MHz clock.

The CRS is ideally suited to provide a precise clock for the USB peripheral.

The CRS requires a synchronization signal.

Three possible sources are selectable with programmable pre-scaler and polarity:

- SYNC external signal provided through pin
- LSE oscillator output
- USB SOF packet reception.

For more details refer to theSTM32H7A3/7B3/7B0 reference manual [2] .

4 Alternate function mapping to pins

To effectively explore the alternate peripheral function pin mapping refer to the STM32CubeMX tool available on www.st.com.

4.1 I/O speed at low voltage

At low VDD voltages, maximum I/O performance can only be obtained by programming the HSLVx bit (see the STM32H7A3/7B3/7B0 reference manual [2] and the applicable datasheets [1]).

This must only be used only for VDD < 2.7 V, and only when necessary for the required performance.

The frequency of the selected feature (communication interface, memory interface and so on) and the I/O output characteristics need to be compared to datasheet values to determine whether HSLVx bit programming is necessary.

Which of the HSLV bits to program depends on the I/O, and can be found in the pin/ball definition table in the datasheet and reference manuals (_h0 to _h3 correspond to HSLV0 to HSLV3 bits).

Before programming the HSLVx bit in the SYSCFG_CCCSR register, the option bytes VDDIO_HSLV and/or VDDMMC_HSLV must be set (see the reference manual).

No speed optimization at low voltage is available for: PA0, PA2, PA4, PA[9:15], PB[6:7], PB[10:11], PC0, PC[2:4], PC[13:15], PF[0:1], PH[0:1], PH[4:7], PI8, PI11, PI15, PJ0, PJ[3:15], PK[0:2], and PK7.

This must be taken into account for the package pad selection when high interface frequencies are required (for example Octo-SPI).

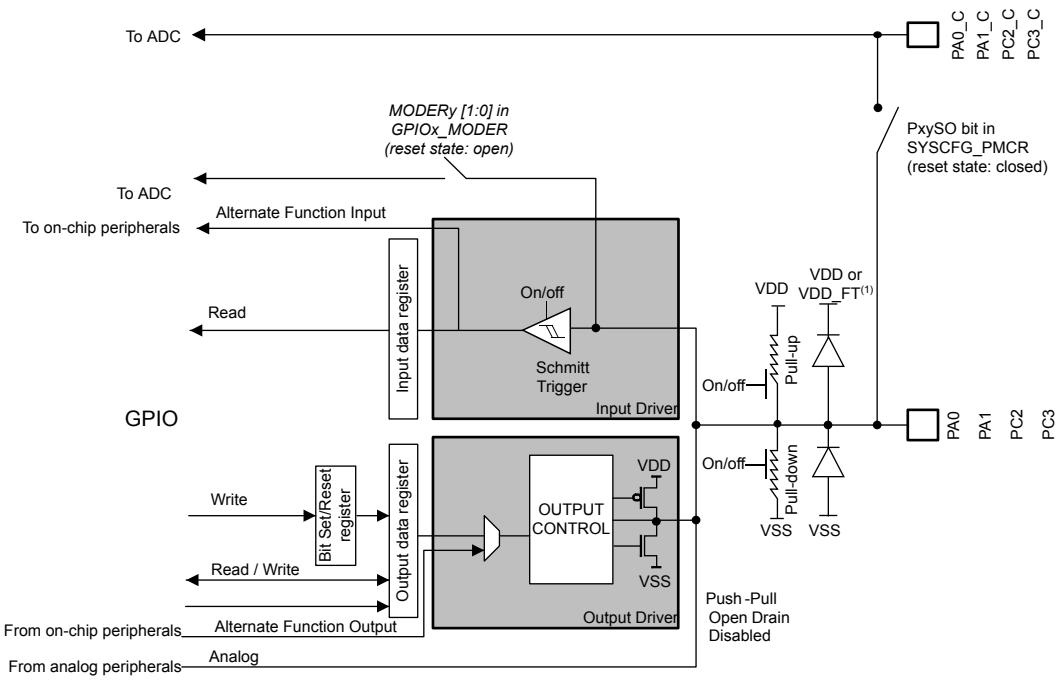
4.2 Analog inputs for ADC1 and ADC2

The STM32H7A3/7B3/7B0 microcontroller embeds four pads with a direct connection to the ADC (PA0_C, PA1_C, PC2_C, and PC3_C).

It avoids the parasitic impedances of a conventional pad and thereby enhancing the ADC performance.

Figure 14 shows the pad schematic (also available in the STM32H7A3/7B3/7B0 datasheets [1]).

Figure 14. Analog inputs for ADC1 and ADC2



Each ADC has 6 inputs optimized for high performance INP0 to INP5 and INN0 to INN5 (fast channels).Refer to the ADC connectivity figure in the STM32H7A3/7B3/7B0 reference manual [2].

The other 14 channels have lower performance (slow channels)

STM32CubeMX and the *Pin/ball definition* table in the applicable STM32H7A3/7B3/7B0 datasheet [1] show the availability of the Pxy_C and Pxy depending on the package.

4.2.1 Packages with Pxy_C and Pxy pads available

This section references the STM32H7A3/7B3/7B0 datasheets [1].

Pxy_C pads

The Pxy_C pads are routed with a direct connection to the ADC fast input channels. For these packages, use the Pxy_C inputs for the ADC to get the best performance (see the datasheet ADC characteristic table *Sampling rate for Direct channels*).

Pxy standard pads connected to ADC fast channels

The performance of Pxy standard pads connected to the ADC fast channels is described in the datasheet ADC characteristic table *Sampling rate for Fast channels*.

Pxy standard pads connected to ADC slow channels

The performance of Pxy standard pads connected to the ADC slow channels is described in the datasheet ADC characteristic table *Sampling rate for Fast channels*.

4.2.2 Packages having Pxy_C but not the peer Pxy

On some packages only the peer Pxy_C, and not the Pxy, pads are available. As indicated in Section 4.2.1 these pads give the best ADC performance (due to their direct connection to the ADC fast input channels).

To access to all the alternate functions of the conventional pad, the internal switch between the two peer pads needs to be closed (by means of the PxySO bit).

All the functionalities of the Pxy pad are then available on the Pxy_C pad. However there is an additional serial impedance due to this switch (300 Ω to 550 Ω) and additional parasitic capacitance (2.5 pF) which may impact timing-sensitive signals.

STM32CubeMX and the table *Port A and Port C alternate function* of the STM32H7A3/7B3/7B0 datasheet [1] indicate the functions available on the Pxy_C pads by closing the switch between the two pads.

4.2.3 Package having Pxy available but not the peer Pxy_C

Closing the switch in the pad (GPIOx_MODER bit) connects an ADC slow input to the Pxy pad (See the figure *ADC connectivity* in the STM32H7A3/7B3/7B0 reference manual [2]). Refer also to the ADC characteristic table *Sampling rate for Slow channels* in the appicable datasheet [1].

Another solution is to close the switch between the two peer pads (PxySO bit) instead of closing the switch in the pad. In this way, an ADC fast input is connected to the Pxy pad. The performance is improved but is not however as high as for a package having a direct input from a Pxy_C pad. (See the datasheet *Sampling rate for Medium speed channels* ADC characteristic table.)

4.3 Pads supplied with VDDMMC

On some packages, several pads are supplied with a dedicated power pad (see VDDMMC in Table 2. PWR input/output signals connected to package pins/ball and Table 3) and the table *Features and peripheral counts* in the applicable datasheet [1] to see which packages embed this feature.

When available the VDDMMC supply pad can be connected together with V_{DD} or used to provide another supply level to this set of pads. In this case, this complete set of pads work at the V_{DDMMC} supply level.

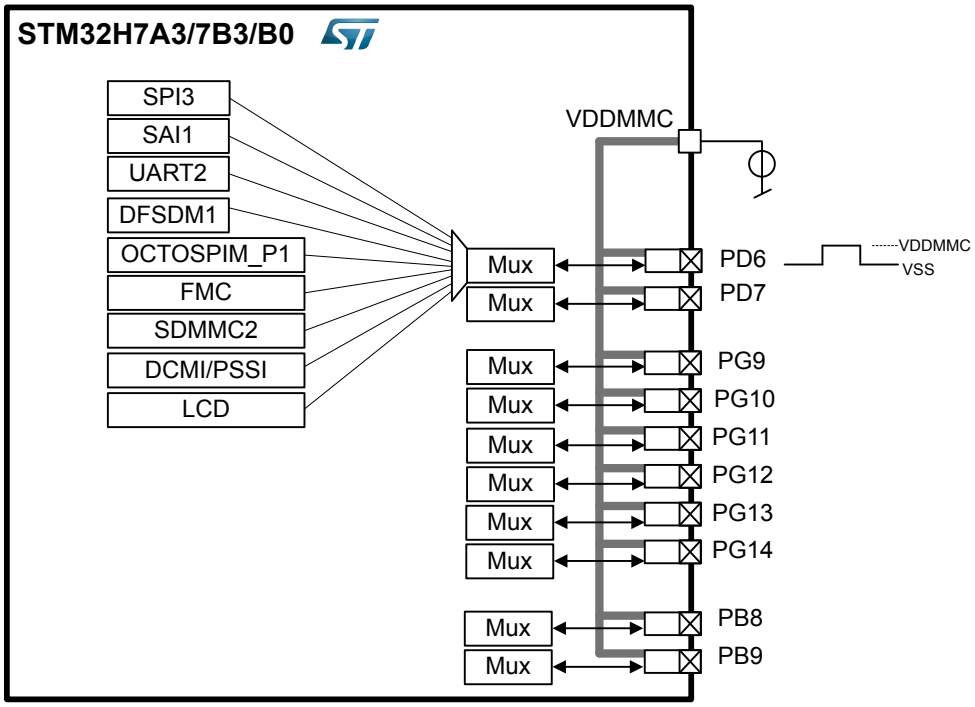
The VDDMMC pin is not available in some packages and for these cases the supply pad is connected internally to V_{DD}. See Figure 26. eMMC interconnection example for an application example. The set of pads supplied with V_{DDMMC} for STM32H7A3/7B3/7B0 microcontrollers is shown in Figure 15. VDDMMC supplied pads.

As mentioned above this complete set of pads interfaces externally at a signal level defined by V_{DDMMC}.

Figure 15 also shows an example of the GPIO PD6 and the different peripherals having one signal mapped to this pad through an alternate function.

Care must be taken for the chosen peripheral not to mix pads supplied with two different supply domains.

Figure 15. **VDDMMC supplied pads**



5 Boot configuration

5.1 Boot mode selection

In STM32H7A3/7B3/7B0 microcontrollers, two different boot spaces can be selected through the BOOT pin and the boot base address programmed in the BOOT_ADD0 or BOOT_ADD1 option bytes as shown in the Table 6.

Table 6. Boot modes

Boot mode selection		Boot space
BOOT pin	Boot address option bytes	
0	BOOT_ADD0 [15:0]	Boot address defined by BOOT_ADD0[15:0] user option byte. Default factory programmed value: User Flash memory starting at 0x0800 0000.
1	BOOT_ADD1 [15:0]	Boot address defined by BOOT_ADD1[15:0] user option byte. Default factory programmed value: System Flash memory starting at 0x1FF0 0000.

The BOOT_ADD0 and BOOT_ADD1 address option bytes allow the boot to be programmed to any boot memory address from 0x0000 0000 to 0x3FFF 0000 which includes:

- all the Flash memory address space mapped on the AXIM interface
- all the RAM address space: ITCM, DTCM RAMs and SRAMs mapped on the AXIM interface
- the system memory bootloader.

The BOOT_ADD0/BOOT_ADD1 option bytes can be modified after the reset in order to boot from any other boot address after the next reset.

If the programmed boot memory address is out of the memory mapped area or a reserved area, the default boot fetch address is programmed as follows:

- Boot address 0: Flash memory at 0x0800 0000
- Boot address 1: ITCM-RAM at 0x0000 0000

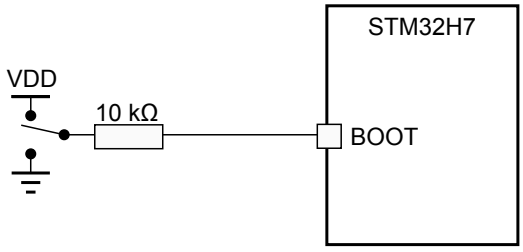
When the Flash level 2 protection is enabled, only boot from Flash memory is available. If the boot address programmed in the BOOT_ADD0 / BOOT_ADD1 option bytes is out of the memory range or belongs to the RAM address range, the default fetch is forced to the Flash memory at address 0x0800 0000.

Note: When the secure access mode is enabled through option bytes, the boot behavior differs from the above description (refer to section Root secure services of the product reference manual).

5.2 Boot pin connection

Figure 16 shows the external connection required to select the boot memory of STM32H7A3/7B3/7B0 microcontrollers.

Figure 16. Boot mode selection implementation example



Resistor values are given only as a typical example.

5.3 System bootloader mode

The embedded bootloader code is located in the system memory. It is programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces.

Table 7 shows the supported communication peripherals by the system bootloader.

Table 7. STM32H7A3/7B3/7B0 microcontroller bootloader communication peripherals

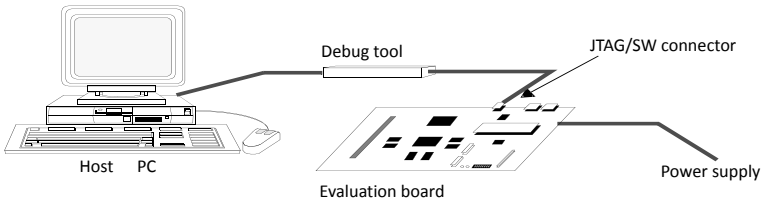
Bootloader peripherals	Bootloader pins
DFU	USB OTG FS (PA11/PA12) in device mode
USART1	PA9/PA10
USART2	PA2/PA3
USART3	PB10/PB11 or PD8/PD9
CAN2	PH13/PH14 or PD0/PD1
I2C1	PB6/PB9
I2C2	PF0/PF1
I2C3	PA8/PC9
SPI1	PA4/PA5/PA6/PA7
SPI2	PI0/PI1/PI2/PI3
SPI3	PA15/PC10/PC11/PC12
SPI4	PE11 / PE12 / PE13 / PE14
USB OTG_FS in Host mode (MSC)	PA11/PA12

6 Debug management

6.1 Introduction

The host / target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG or SW connector and a cable connecting the host to the debug tool. Figure 17 illustrates the connection of the host to the evaluation board.

Figure 17. Host to board connection



6.2 SWJ debug port (serial wire and JTAG)

The core of STM32H7A3/7B3/7B0 microcontrollers integrates the serial wire / JTAG debug port (SWJ-DP). It is an Arm standard debug port that combines a 5-pin JTAG-DP interface and a 2-pin SW-DP interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port.
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port.

In the SWJ-DP, the two SW-DP JTAG pins the are multiplexed with some of the JTAG-DP five JTAG pins.

For more details on the SWJ debug port refer to the STM32H7A3/7B3/7B0 reference manual [2]*SWJ debug port* section (serial wire and JTAG).

6.2.1 TPIU trace port

The TPIU trace port comprises four data outputs plus one clock output. The number of data outputs can be configured by software and unused signals can be reused as GPIOs. If the trace port is not required, all the signals can be used as GPIOs. By default, the trace port is disabled.

The trace data and clock can operate at up to 133 MHz. As a result, care must be taken with the layout of these signals: the trace connector should be located as close as possible to the STM32H7A3/7B3/7B0 microcontroller, while still allowing enough space to attach the trace port analyzer probe.

Refer to Table 8 for a summary of trace pins and GPIO assignment.

Table 8. TPIU trace pins

Trace pin name	Type	Description	Pin assignment
TRACED0	Output	Trace synchronous data out 0	PC1 or PE3 or PG13
TRACED1	Output	Trace synchronous data out 1	PC8 or PE4 or PG14
TRACED2	Output	Trace synchronous data out 2	PD2 or PE5
TRACED3	Output	Trace synchronous data out 3	PC12 or PE6
TRACECLK	Output	Trace clock	PE2

6.2.2 External debug trigger

The TRGIN and TRGOUT pins are available on some packages. On smaller packages, they are replaced by a bidirectional TRGIO signal, which is configured as TRGIN or TRGOUT by software.

Refer to Table 9 for a summary of trigger pins and GPIO assignment.

Table 9. External debug trigger pins

Trigger pin name	Type	Description	Pin assignment
TRGIN	I	External trigger input	PJ7
TRGOUT	O	External trigger output	PJ12
TRGIO	IO	External trigger bi-directional	PC7

6.3 Pinout and debug port pins

STM32H7A3/7B3/7B0 microcontrollers are available in various packages with differing number of pins. As a result, some functionality is related to the pin availability (TPIU parallel output interface) and differs between the packages.

6.3.1 SWJ debug port pins

Five pins are used as outputs from the STM32H7A3/7B3/7B0 microcontrollers for the SWJ-DP as alternate general-purpose I/O functions. These pins are available on all packages and detailed in Table 10.

Table 10. SWJ debug port pins

SWJ-DP pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Debug assignment	
JTMS/SWDIO	I	JTAG test mode selection	IO	Serial wire data input/output	PA13
JTCK/SWCLK	I	JTAG test clock	I	Serial wire clock	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO/TRACESWO	O	JTAG test data output	-	TRACESWO if asynchronous trace is enabled	PB3
NJTRST	I	JTAG test nReset	-	-	PB4

6.3.2 Flexible SWJ-DP pin assignment

After RESET (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins immediately available to the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, STM32H7A3/7B3/7B0 microcontrollers offer the possibility of disabling some or all of the SWJ-DP ports, so freeing the associated pins for general-purpose IO (GPIO) use.

Table 11 shows the different possibilities to release some pins.

Table 11. Flexible SWJ-DP assignment

Available debug ports	SWJ IO pins assigned				
	PA13/JTMS/SWDIO	PA14/JTCK/SWCLK	PA15/JTDI	PB3/JTDO	PB4/NJTRST
Full SWJ (JTAG-DP + SW-DP) - reset state	X	X	X	X	X
Full SWJ (JTAG-DP + SW-DP) but without NJTRST	X	X	X	X	-
JTAG-DP disabled and SW-DP enabled	X	X	-		
JTAG-DP disabled and SW-DP disabled	Released				

For more details on how to disable SWJ-DP port pins, refer to the STM32H7A3/7B3/7B0 reference manual [2] I/O pin alternate function multiplexer and mapping section.

6.3.3 Internal pull-up and pull-down on JTAG pins

The devices embed internal pull-ups and pull-downs to guarantee a correct JTAG behavior. Consequently, the pins are not left floating during reset and they are configured as follows until the user software takes control of them:

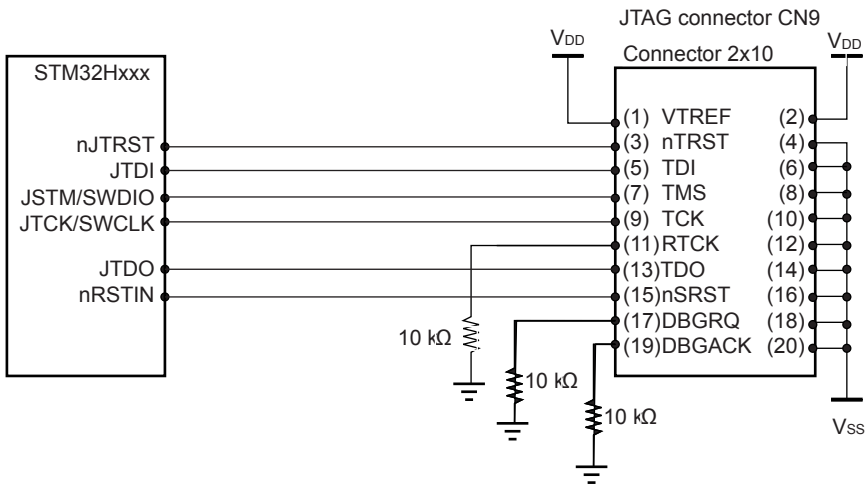
- NJTRST: internal pull-up.
- JTDI: internal pull-up.
- JTMS/SWDIO: internal pull-up.
- JTCK/SWCLK: internal pull-down.
- JTDO: floating state (tristate).

If these I/Os are externally connected to a different voltage, a leakage current flows during and after reset, until they are reconfigured by software. Special care must be taken with the TCK/SWCLK pin, which is directly connected to some of the clock flip-flops, since it should not toggle before the JTAG I/O is released by the user software.

6.3.4 SWJ debug port connection with standard JTAG connector

Figure 18 shows the connection between STM32H7A3/7B3/7B0 microcontrollers and a standard JTAG connector.

Figure 18. JTAG connector implementation



7 Recommendations

7.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to the ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides both good decoupling and good shielding effect. For many applications, cost reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for the ground and the power supply.

7.2 Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution in order to reduce the cross-coupling on the PCB, that is noisy, high-current circuits, low-voltage circuits, and digital components.

7.3 Ground and power supply (V_{SS}, V_{DD})

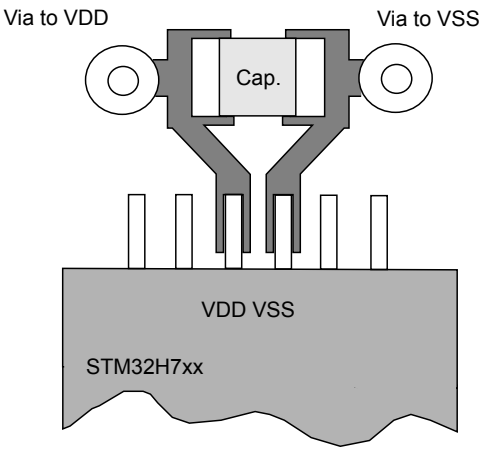
Every block (noisy, low-level sensitive, digital, etcetera) should be grounded individually and all ground returns should be to a single point. Loops must be avoided or have a minimum area. The power supply should be implemented close to the ground line to minimize the supply loop area. This is due to the fact that the supply loop acts as an antenna, and it therefore becomes the EMI main transmitter and receiver. All component-free PCB areas must be filled with additional grounding to create adequate shielding (especially when using single-layer PCBs).

7.4 Decoupling

All the power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have lowest possible impedance. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors (100 nF) and one single ceramic capacitor (minimum 4.7 µF) connected in parallel. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but the exact values depends on the application needs. Figure 19 shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 19. Typical layout for V_{DD}/V_{SS} pair



7.5 Other signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (the case of interrupts and handshaking strobe signals, and not the case for LED commands). For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve the EMC performance. For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (for example clocks).
- Sensitive signals (for example high-impedance).

7.6 Unused I/Os and features

All the microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources. To increase the EMC performance, unused clocks, counters or I/Os, should not be left free, e.g. I/Os should be set to 0 or 1 (pull-up or pull-down to the unused I/O pins.) and unused features should be frozen or disabled.

8 Reference design

The Evaluation board (STM32H7B3I-EVAL), Discovery kit (STM32H7B3I-DK) and Nucleo board (NUCLEO-H7A3ZI-Q) are proven designs and must be used as foundations for specific application development.

All the board details are available on www.st.com

9 Recommended PCB routing guidelines for STM32H7A3/7B3/7B0 microcontrollers

9.1 PCB stack-up

In order to reduce the reflections on high speed signals, the impedance between the source, sink and transmission lines have to be matched. The impedance of a signal trace depends on its geometry and its position with respect to any reference plane.

The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which addresses all the impedance requirements .

The minimum configuration that can be used is 4 or 6 layers stack-up. An 8 layers boards may be required for a very dense PCBs that have multiple SDRAM/SRAM/NOR/LCD components.

The following stack-ups (Figure 20 and Figure 21) are examples that can be used as guidelines for stack-up evaluation and selection. These stack-up configurations place the GND plane adjacent to the power plane to increase the capacitance and reduce the physical gap between GND and the power plane. High speed signals on the top layer have a solid GND reference plane which helps reduce the EMC emissions. Having a GND reference for each PCB signal layer in the stack further improves the radiated EMC performance.

Figure 20. Four layer PCB stack-up example

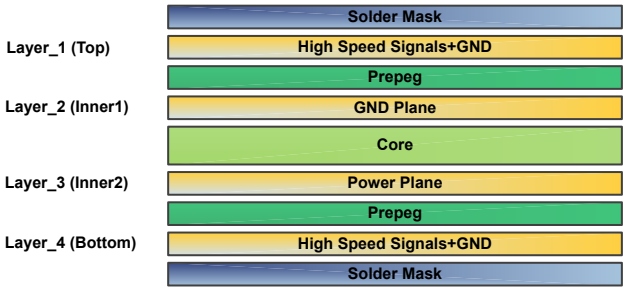
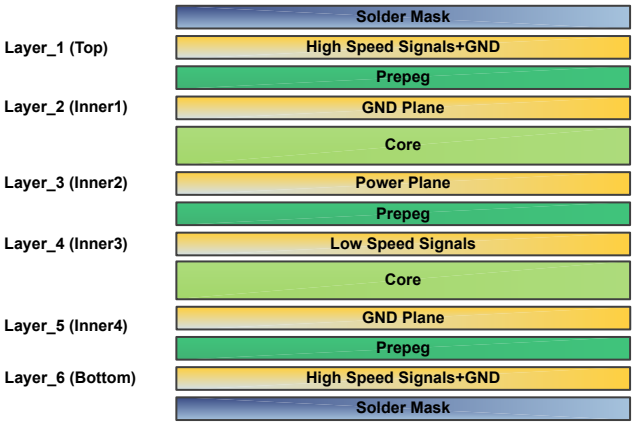


Figure 21. Six layer PCB stack-up example



9.2 Crystal oscillator

Use the application note: *Oscillator design guide for STM8S, STM8A and STM32 microcontrollers*[4], for further guidance on how to layout and route crystal oscillator circuits.

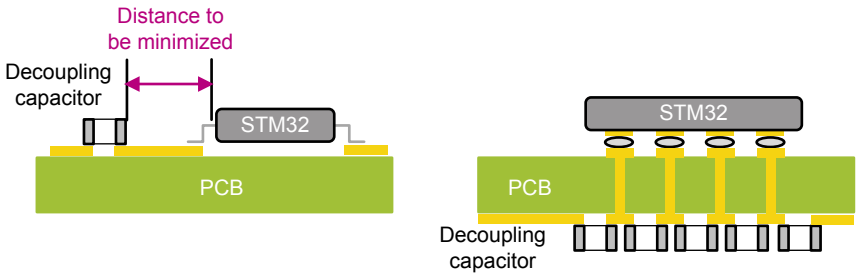
9.3 Power supply decoupling

An adequate power decoupling for the STM32H7A3/7B3/7B0 microcontroller is necessary to prevent excessive power and ground bounce noise. Refer to Section 2 Power supplies

The following recommendations shall be followed:

- Place the decoupling capacitors as close as possible to the power and ground pins of the MCU. For BGA packages, it is recommended to place the decoupling capacitors on the opposing side of the PCB (see Figure 22).
- Add the recommended decoupling capacitors to as many V_{DD}/V_{SS} pairs as possible.
- Connect the decoupling capacitor pad to the power and ground plane with a wide and short trace/via. This reduces the series inductance, maximizes the current flow and minimizes the transient voltage drops from the power plane and in turn reduces the ground bounce occurrence.

Figure 22. Decoupling capacitor placement depending on package type

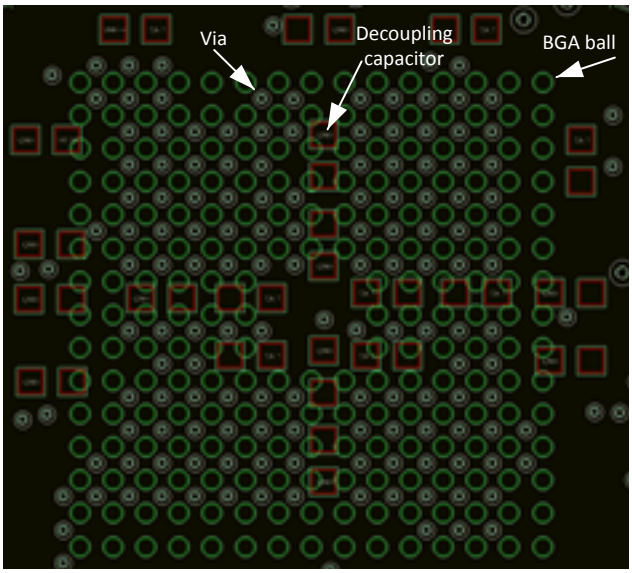


Decoupling capacitor and STM32 MCU on the same side of the package (all packages except BGA)

Decoupling capacitor and STM32 MCU on the opposite sides of the package (BGA package)

Figure 23 shows an example of decoupling capacitor placement underneath STM32H7A3/7B3/7B0 microcontroller, closer to the pins and with less vias.

Figure 23. **Example of decoupling capacitor placed underneath**



9.4 High speed signal layout

9.4.1 SDMMC bus interface

Interface connectivity

The SD/SDIO MMC card host interface (SDMMC) provides an interface between the AHB peripheral bus and Multi Media Cards (MMCs), SD memory cards and SDIO cards. The SDMMC interface is a serial data bus interface, that consists of a clock (CK), command signal (CMD) and 8 data lines (D[0:7]).

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10 nF switching cap between PWR and GND).
- Trace impedance: 50 Ω ± 10%.
- All clock and data lines should have equal lengths to minimize any skew.
- The maximum skew between data and clock should be less than 250 ps at 10 mm.
- The maximum trace length should be less than 120 mm. If the signal trace exceeds this trace-length/speed criteria, then a termination should be used.
- The trace capacitance should not exceed 20 pF at 3.3 V and 15 pF at 1.8 V.
- The maximum signal trace inductance should be less than 16 nH.
- Use the recommended pull-up resistance for CMD and data signals to prevent the bus from floating.
- The mismatch within data bus, data and CK or CK and CMD should be below 10mm.
- All data signals must have the same number of vias.

Note: The total capacitance of the SD memory card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line. The total bus capacitance is $C_L = C_{Host} + C_{Bus} + N*C_{Card}$ where the host is an STM32H7A3/7B3/7B0 microcontroller, the bus is all the signals and Card is SD card.

Figure 24, Figure 25 and Figure 26 show different typical use cases.

Figure 24. **µSDCard interconnection example**

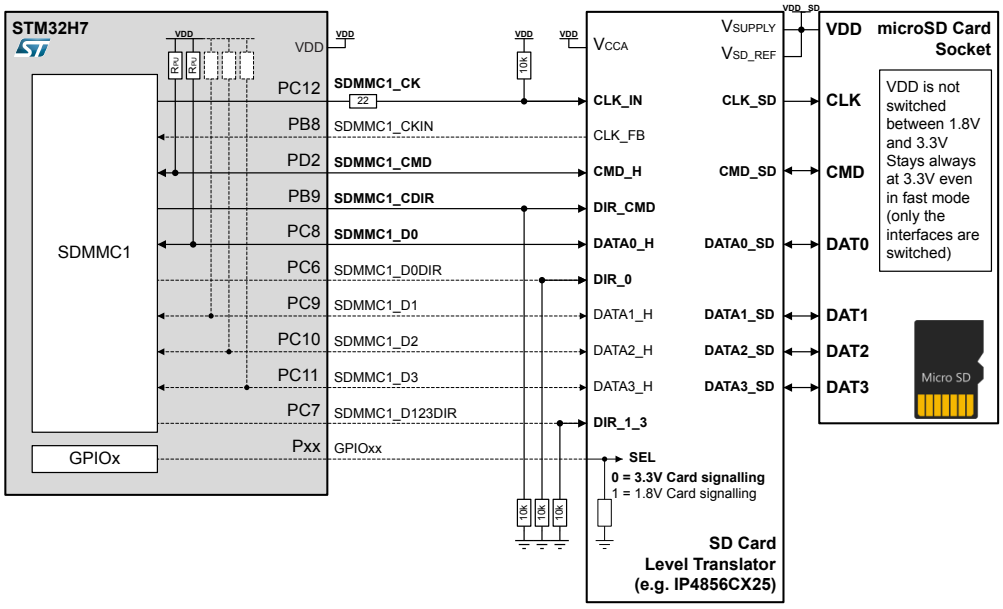


Figure 25. **SDCard interconnection example**

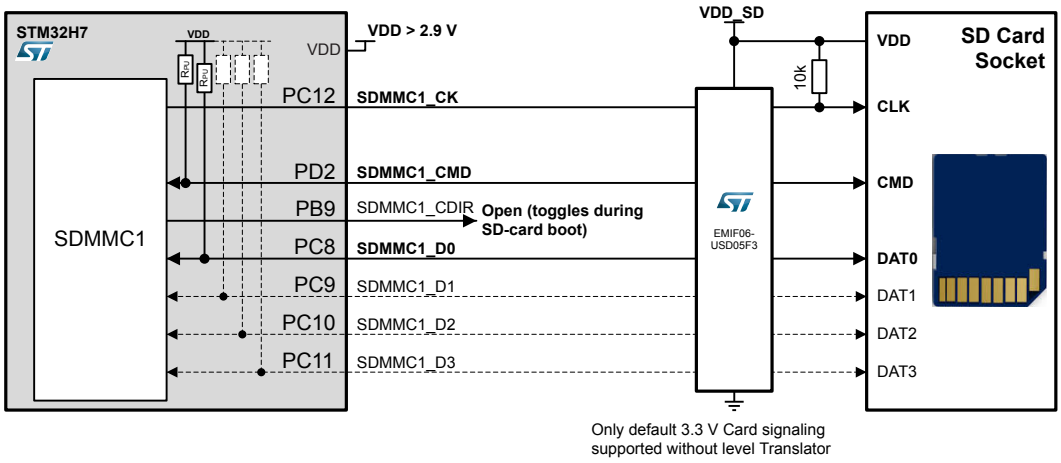
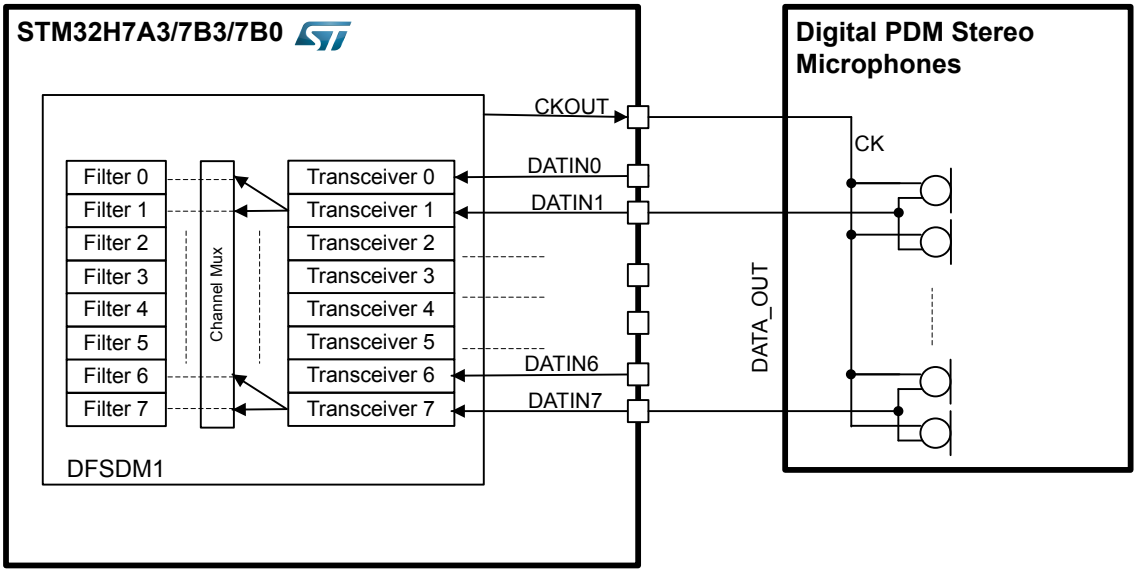


Figure 26. **eMMC interconnection example**



The VDD_MMC pad can supply the SDIO2 I/Os with a dedicated voltage level which can be dynamically switched, for instance from 3.3 V to 1.8 V (valid only for the SDMMC2 I/Os listed in this schematic (see also Table 2. PWR input/output signals connected to package pins/ball).

9.4.2 Flexible memory controller (FMC) interface

Interface connectivity

The FMC controller and in particular SDRAM memory controller are composed of many signals, most of them have a similar functionality and work together. The controller I/O signals could be split in four groups as follow:

- An address group which consists of row/column address and bank address.
- A command group which includes the row address strobe (NRAS), the column address strobe (NCAS), and the write enable (SDWE).
- A control group which includes a chip select bank1 and bank2 (SDNE0/1), a clock enable bank1 and bank2 (SDCKE0/1), and an output byte mask for the write access (DQM).
- A data group/lane which contains 8 signals.

Note: This is depends on the memory specification: SDRAM with x8 bus widths have only one data group, while x16 and x32 bus-width SDRAM have two and four lanes, respectively.

Interface signal layout guidelines

- For reference the plane using GND or PWR (if PWR), add 10 nF stitching cap between PWR and GND.
- Trace impedance: 50 Ω ± 10%.
- The maximum trace length should not exceed 120mm. If the signal trace exceeds this trace-length / speed criteria, then a termination should be used.
- To reduce the crosstalk, it is strongly recommended to place data tracks on the different layers to the address and control lanes. However, when the data and address / control tracks coexist on the same layer they must be separated from each other by at least 5 mm.
- Match the trace lengths for the data group within ± 10 mm of each other to reduce any excessive skew. Serpentine traces (this is an “S” pattern to increase trace length) can be used to match the lengths.
- Placing the clock (SDCLK) signal on an internal layer, minimizes the noise (EMI). Route the clock signal at least three times the width of the trace away from others signals. To avoid unnecessary impedance changes and reflection, avoid the use of vias as much as possible. Serpentine routing is to be avoided also.
- Match the clock traces to the data/address group traces length to within ±10 mm.
- Match the clock traces length to each signal trace in the address and command groups to within ±10 mm (with maximum of ≤ 20 mm).
- Trace capacitances:
  - At 3.3 V keep the trace capacitance within 20 pF with overall capacitive loading (including Data, Address, SDCLK and Control) no more than 30 pF.
  - At 1.8 V keep the trace capacitance within 15 pF with overall capacitive loading (including Data, Address, SDCLK and Control) no more than 20 pF.

9.4.3 Octo-SPI interface

Interface connectivity

The Octo-SPI is a specialized communication interface targeting single, dual, quad and octal communication. Refer to the STM32H7A3/7B3/7B0 reference manual [2] for details, and to the applicable STM32H7A3/7B3/7B0 datasheet [1] for the full electrical characteristics.

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10 nF stitching cap between PWR and GND
- Trace impedance: 50 Ω for single-ended and 100 Ω for differential pairs (CLK/NCLK)
- The maximum trace length should be less than120 mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- Avoid using multiple signal layers for the data signal routing.
- Route the clock signal at least three times the width of the trace away from other signals. To avoid unnecessary impedance changes and reflection, avoid the use of vias as much as possible. Serpentine routing is to be avoided also.

- Match the trace lengths for the data group within ± 10 mm of each other to reduce any excessive skew. Serpentine traces (this is an “S” shape pattern to increase trace length) can be used to match the lengths.
- Avoid using a serpentine routing for the clock signal and use via(s) as little as possible for the whole path. A via alters the impedance and adds a reflection to the signal.
- Avoid discontinuities on high speed traces (vias, SMD components).
- If the interface runs below 2.7 V, special care has to be taken when choosing the package pads (see Section 4.1 I/O speed at low voltage).

Figure 27 and Figure 28 illustrate possible interconnection examples.

If SMD components are needed, place these components symmetrically to ensure good signal quality.

Figure 27. Octo-SPI interconnection example

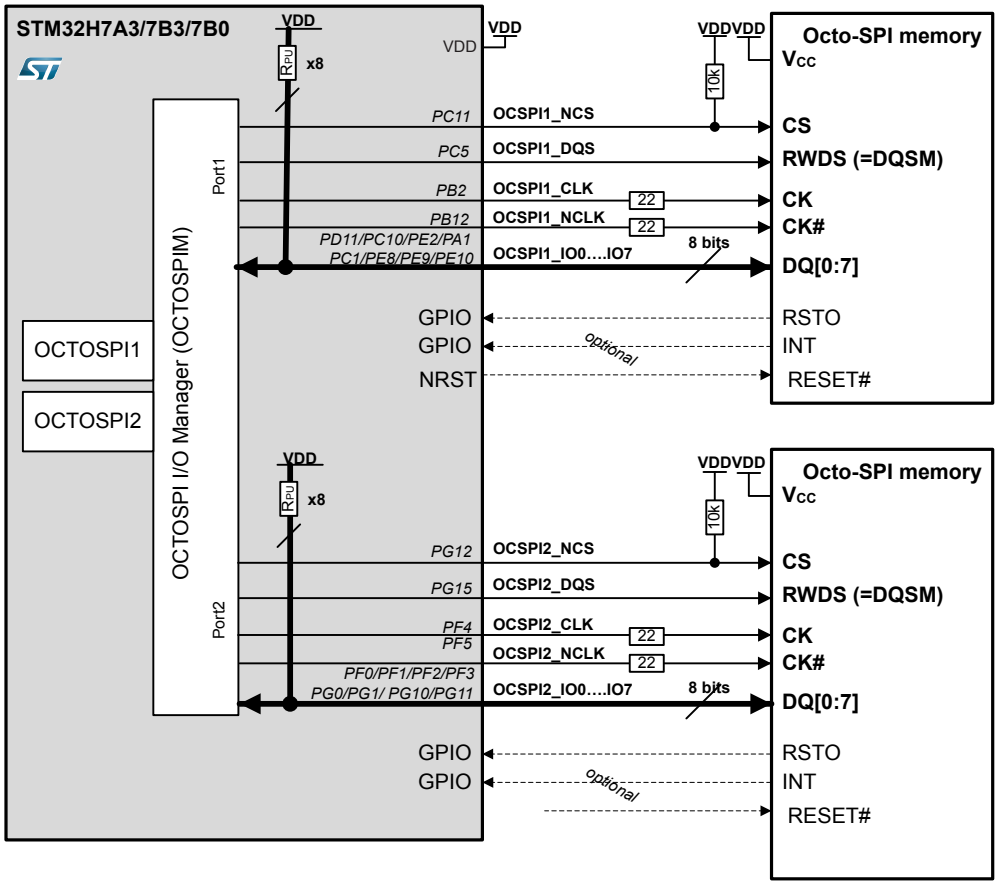
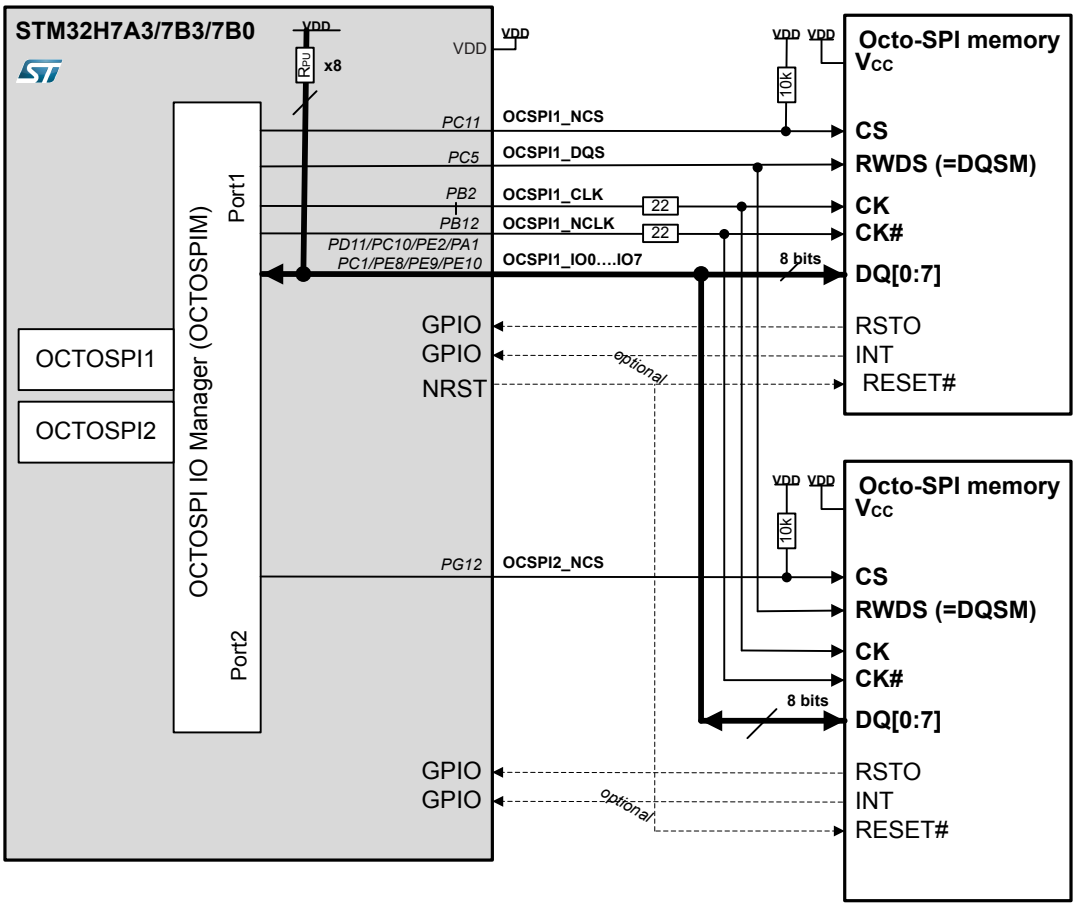


Figure 28. **Octo-SPI multiplexed interconnection example**



In multiplexed mode, the same bus can be shared between two external Octo-SPI memories. The multiplexed mode must be configured to avoid unwanted transactions when the OCTOSPIs are disabled.

Note: The multiplexed mode can be very useful for some packages where the port2 is not mapped.

Caution: PG12 is not available in all packages.

9.4.4 DFSDM interface

The digital filter for the sigma delta modulator (DFSDM) is dedicated to the external sigma-delta modulator's interface (refer to the reference manual STM32H7A3/7B3/7B0[2] for details). It can, for instance, handle data stream issued from sensors or pulse density modulation (PDM) microphones.

Two DFSDMs are embedded in the STM32H7A3/7B3/7B0 microcontroller:

- The CPU power domain (CD) DFSDM is composed of eight filters
- The smart run domain (SRD) DFSDM is composed of one filter.

(See the associated migration guide application note [6] and the STM32H7A3/7B3/7B0 reference manual [2]).

For CKOUT and DATIN1 it is possible to choose one pin mapping that shares the same pins between DFSDM1 and DFSDM2.

The SRD domain can run autonomously while the CD domain is in low power mode.

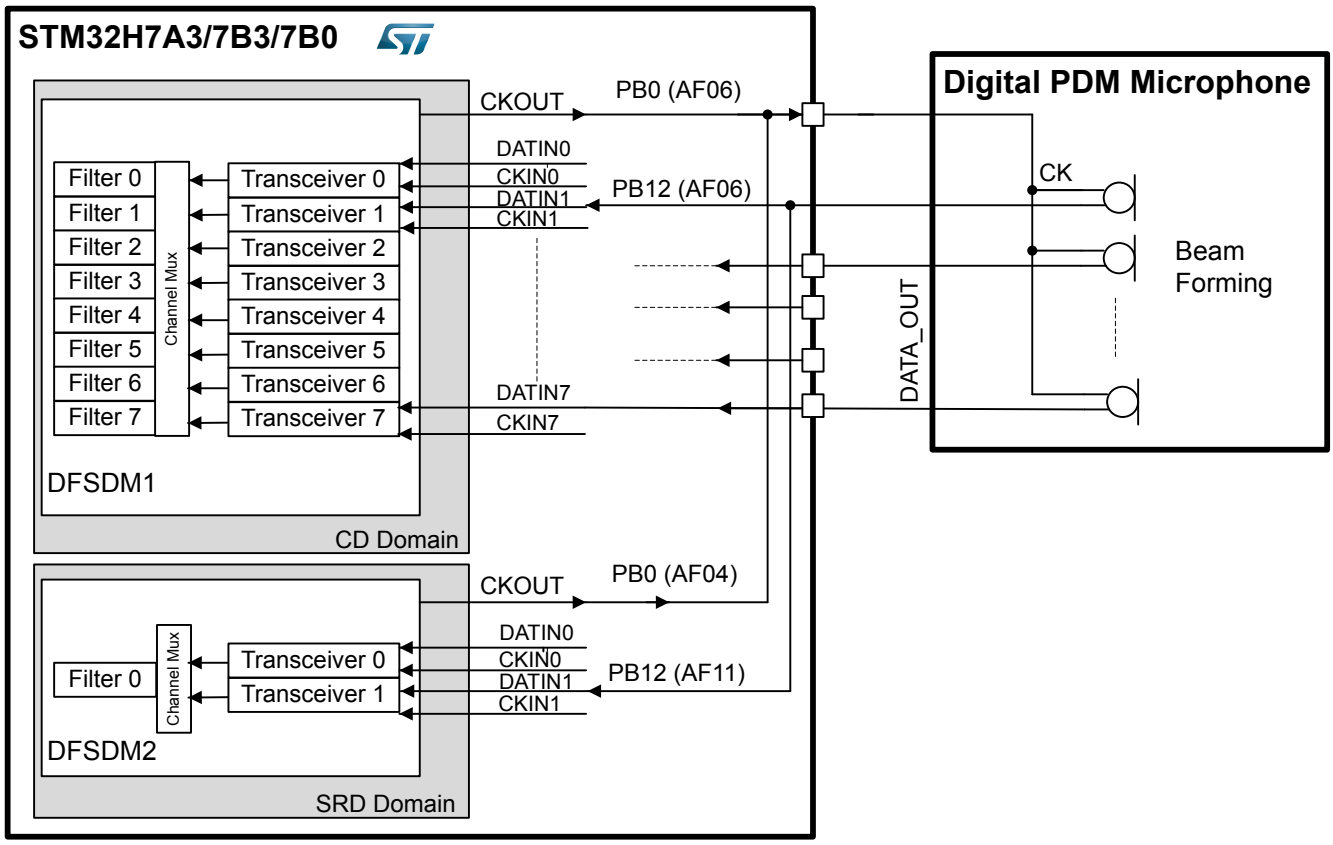
This specific pin mapping allows, for instance, DFSDM2 to be used to wake up the CD domain. The used pin is then reallocated to DFSDM1 by programming another alternate function (AF).

Figure 29. DSFDM interconnection example shows an example of a PDM microphone connected to the DFSDM2 and used for "voice activity detection". When a sound is detected the analog watchdog included in the DFSDM2 triggers an interrupt which wakes up the CD domain and the CPU.

This single microphone is then reallocated to DFSDM1. The set of PDM microphones connected to the DFSDM1 can for instance perform beam forming and voice recognition.

This example can be transposed to any other kind of external sensors.

Figure 29. DSFDM interconnection example



PDM stereo microphones can use both clock edges for data sampling. One edge for the left channel and the other for the right channel.

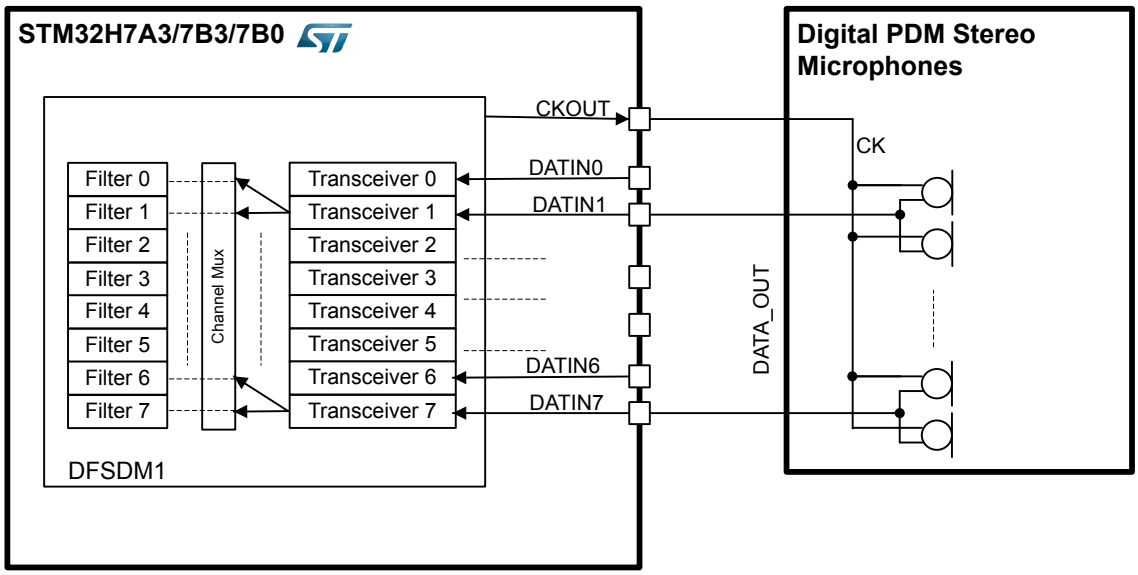
Two DFSDM filters share the same DATIN input.

Two consecutive DATINx inputs cannot be used in such a case (refer to the STM32H7A3/7B3/7B0 reference manual [2] for details).

Figure 30. Stereo microphone interconnection shows an example of a stereo microphone interconnection.

This example can be transposed to other kinds of external sensors.

Figure 30. **Stereo microphone interconnection**



9.4.5 Embedded trace macrocell (ETM)

Interface connectivity

The ETM enables the reconstruction of the program execution. The data is traced using the data watchpoint and trace (DWT) component or the instruction trace macrocell (ITM) whereas instructions are traced using the embedded trace macrocell (ETM). The ETM interface is synchronous with the four data bus lines D[0:3] and the clock signal CLK.

Interface signals layout guidelines

- Reference the plane using GND or PWR (if PWR, add a 10 nF stitching capacitor between PWR and GND.
- Trace impedance: 50 Ω ± 10%.
- All the data trace should be as short as possible (≤25 mm).
- Trace the lines which should run on the same layer with a solid ground plane underneath it without vias.
- Trace the clock, which should have only point-to-point connection. Any stubs should be avoided.
- It is strongly recommended also for other (data) lines to be point-to-point only. If any stubs are needed, they should be as short as possible. If long stubs are required, it should be made possible to optionally disconnect them (for example by jumpers).

10 Use case examples

STM32CubeMX must be used to determine the most appropriate package for a given use case.

Table 12 gives some typical use case examples. It defines the package which supports a specific use case and identifies the peripherals that are available. All the examples below are also supported on larger packages.

Table 12. Use case examples

Package	Use Case	Peripheral	Comment
LQFP64	SDMMC	SDMMC1	External memory
		USB-FS	-
		SPI1	Communication interface
		GPIO	Available GPIO or possible to add peripherals
LQFP64	Display	LCD	RGB TFT Display up to 6/6/6
		I2C4	Touch screen or communication FM+
		QuadSPI1	External memory
		UART2	Communication and/or bootloader
		CAN2 or UART5	Communication interface
		SPI6 or I2S6	Communication interface
		SW-DP	Debug port 3 wires
LQFP64	Motor control	ADC	Motor phase A current+ Motor phase B current+ Motor phase C current+ Motor phase ΩA current+
		ADC	Motor heatsink Temp
			Motor bus voltage
			Motor PFC ind. curr
			Motor PFC VAC
		TIM2 CH1	Motor encoder A
		TIM2 CH2	Motor encoder B
		TIM2 CH3	Motor encoder index
		TIM15 CH2	Motor PFC PWM
		TIM1 BKIN	Motor emergency stop
		TIM1 CH1N	Motor PWM_1L
		TIM1 CH2N	Motor PWM_2L
		TIM1 CH3N	Motor PWM_3L
		DAC1 OUT1	Debug or output to external comparator
		DAC2 OUT1	Debug or output to external comparator
		USART3	Communication interface
		USART6	Communication interface
		SPI3	SPI display data
		I2C1	Bootloader or display touch

Package	Use Case	Peripheral	Comment
LQFP64	Motor control	I2C4	External memory
		GPIO	Motor ICL shutdown
		GPIO	Motor dissipative brake
		GPIO	SPI display backlight control
		GPIO	SPI display Data/Com
		GPIO	SPI display reset
		SWD/C	Serial wire debug port
LQFP100 (non SMPS)	Display and µSD	LCD	RGB TFT Display 8/8/8
		I2C	Communication interface
		SDMMC2	µSD
		GPIO	SD card detection
		USB-FS	-
		USART3	Communication interface
		SPI3	Communication interface
		GPIO	remaining GPIO available
LQFP100 (non SMPS)	Display and OCTOSPI	LCD	RGB TFT display 8/8/8
		I2C1	Touch screen or communication interface
		OCTOSPIM_P1	External memory
		USART2	Communication interface
		SPI1	Communication interface
		USB-FS	-
		GPIO	Remaining GPIO available
LQFP100 (non SMPS)	Audio beam forming and VAD Display External memory or Wi-Fi module	FMC	Memory interface used to drive a display (up to 16 bit parallel)
		I2C4	Touch screen or communication interface
		DFSDM2	Digital microphone interface for voice activity detection (VAD), shared with DFSDM1 (see Section 9.4.4).
		DFSDM1	Digital microphone interface (up to 8) Beam forming
		SDMMC	To interface WIFI module or memory
		SPI1	Communication interface
		USB-FS	-
LQFP100	Camera, Display and µSD	FMC	Memory interface used to drive a display (up to 14 bit parallel)
		I2C2	Touch screen or communication interface
		DCMI	14 bit parallel camera interface
		USB-FS	-
		SDMMC2	µSD (4 bit mode)
		GPIO	µSD detection
WLCSP132	Camera, Display, OCTOSPI and µSD	FMC	Memory interface used to drive a display (up to 16 bit parallel)
		I2C2	Touch screen or communication interface

Package	Use Case	Peripheral	Comment
WLCSP132	Camera, Display, OCTOSPI and µSD	DCMI	14 bit parallel camera interface
		OCTOSPIM_P1	External memory
		UART1	Communication interface
		UART2	Communication interface
		USB-FS	-
WLCSP132	Camera, Display, QuadSPI, RF module	LCD	RGB TFT Display 8/8/8
		I2C4	Touch screen or communication interface
		DCMI	14 bit parallel camera interface
		OCTOSPIM_P1	QuadSPI mode for external memory
		SDMMC2	4 data bits, RF module or external memory
		UART1	Communication interface
WLCSP132	PSRAM Combo, Display, RF module	LCD	RGB TFT display 8/8/8
		FMC	PSRAM 16 bit
		GPIO	Combo hardware reset pin
		GPIO	Combo prog acceleration pin
		SDMMC2	4 data bits, RF module or external memory
		SPI2	Communication interface
		USB-FS	-
WLCSP132	Display, OCTOSPI, eMMC with dedicated supply, DFSDM	LCD	RGB TFT display 8/8/8
		I2C3	Touch screen or communication interface
		OCTOSPIM_P1	External Octo-SPI memory
		SDMMC2	eMMC with separate VDDMMC supply (see Figure 26. eMMC interconnection example)
		DFSDM	3 inputs, for instance for sensors or microphones
		SPI2	Communication interface
		LPUART1	Communication interface, CTS RTS included

Revision history

Table 13. **Document revision history**

Date	Version	Changes
21-May-2019	1	Initial release.
03-Jun-2019	2	Updated Section Introduction and Section 1 General information.
31-Jan-2020	3	Changed document classification to public.
15-May-2020	4	Extended document scope to include STM32H7B0 Value line microcontrollers. Updated: • Figure 1. Power supplies • title of Figure 2. System supply configurations for devices with SMPS • Interface signal layout guidelines • Section 2.2.1 Power-on reset (POR)/power-down reset (PDR) and Figure 8. Power on reset/power down reset waveform • Table 7. STM32H7A3/7B3/7B0 microcontroller bootloader communication peripherals. Added: • Figure 3. System supply configurations for devices without SMPS • Section 4.1 I/O speed at low voltage. Removed FDCAN2 block from Figure 15. VDDMMC supplied pads.
09-Sep-2020	5	Reinstated Section 2.1.1 External power supplies and components including: • Table 3. Power supply connection • Figure 4. Power supply component layout.

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