



1. Description

1.1. Project

Project Name	H7L3ABaseProject
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	04/20/2021

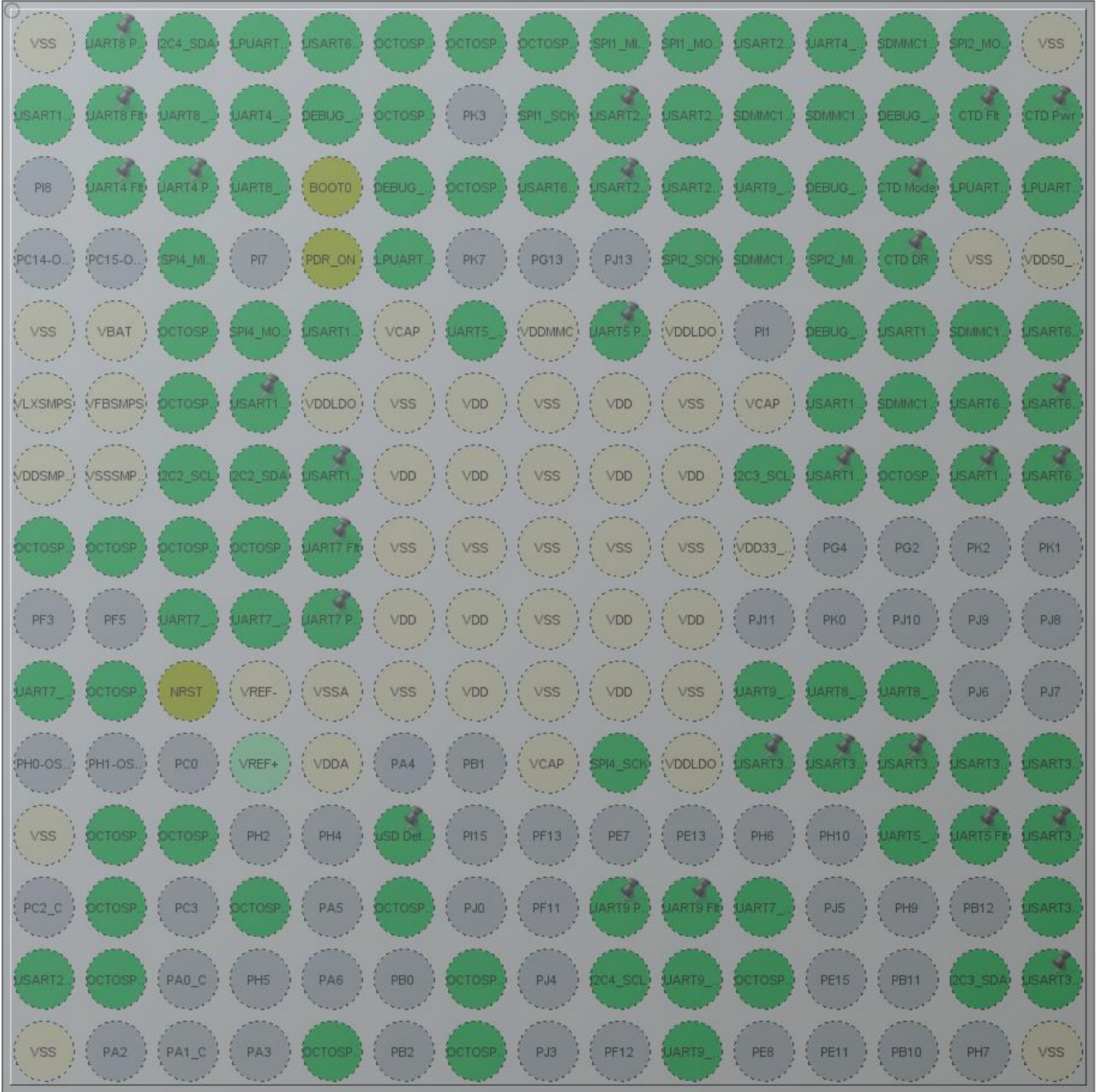
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H7A3/7B3
MCU name	STM32H7A3LIHxQ
MCU Package	TFBGA225
MCU Pin number	225

1.3. Core(s) information

Core(s)	Arm Cortex-M7
---------	---------------

2. Pinout Configuration



TFBGA225 (Top view)

3. Pins Configuration

Pin Number TFBGA225	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PI4 *	I/O	GPIO_Output	UART8 Pwr
A3	PB9	I/O	I2C4_SDA	
A4	PB6	I/O	LPUART1_TX	
A5	PG15	I/O	USART6_CTS	
A6	PK5	I/O	OCTOSPIM_P2_NCS	
A7	PG14	I/O	OCTOSPIM_P1_IO7	
A8	PG10	I/O	OCTOSPIM_P2_IO6	
A9	PG9	I/O	SPI1_MISO	
A10	PD7	I/O	SPI1_MOSI	
A11	PD4	I/O	USART2_RTS	
A12	PD1	I/O	UART4_TX	
A13	PC10	I/O	SDMMC1_D2	
A14	PI3	I/O	SPI2_MOSI	
A15	VSS	Power		
B1	PE3	I/O	USART10_TX	
B2	PI5 *	I/O	GPIO_Input	UART8 Flt
B3	PE0	I/O	UART8_RX	
B4	PB8	I/O	UART4_RX	
B5	PB4	I/O	DEBUG_JTRST	
B6	PK6	I/O	OCTOSPIM_P2_DQS	
B8	PG11	I/O	SPI1_SCK	
B9	PJ15 *	I/O	GPIO_Output	USART2 Pwr
B10	PD6	I/O	USART2_RX	
B11	PD2	I/O	SDMMC1_CMD	
B12	PC12	I/O	SDMMC1_CK	
B13	PA14	I/O	DEBUG_JTCK-SWCLK	
B14	PH15 *	I/O	GPIO_Input	CTD Flt
B15	PH14 *	I/O	GPIO_Output	CTD Pwr
C2	PE4 *	I/O	GPIO_Input	UART4 Flt
C3	PI6 *	I/O	GPIO_Output	UART4 Pwr
C4	PE1	I/O	UART8_TX	
C5	BOOT0	Boot		
C6	PB3	I/O	DEBUG_JTDO-SWO	
C7	PK4	I/O	OCTOSPIM_P2_IO7	
C8	PG12	I/O	USART6_RTS	

Pin Number TFBGA225	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
C9	PJ14 *	I/O	GPIO_Input	USART2 Flt
C10	PD5	I/O	USART2_TX	
C11	PD0	I/O	UART9_CTS	
C12	PA15	I/O	DEBUG_JTDI	
C13	PI0 *	I/O	GPIO_Output	CTD Mode
C14	PA12	I/O	LPUART1_RTS	
C15	PA11	I/O	LPUART1_CTS	
D3	PE5	I/O	SPI4_MISO	
D5	PDR_ON	Reset		
D6	PB7	I/O	LPUART1_RX	
D10	PD3	I/O	SPI2_SCK	
D11	PC11	I/O	SDMMC1_D3	
D12	PI2	I/O	SPI2_MISO	
D13	PH13 *	I/O	GPIO_Output	CTD DR
D14	VSS	Power		
D15	VDD50_USB	Power		
E1	VSS	Power		
E2	VBAT	Power		
E3	PI9	I/O	OCTOSPIM_P2_IO0	
E4	PE6	I/O	SPI4_MOSI	
E5	PE2	I/O	USART10_RX	
E6	VCAP	Power		
E7	PB5	I/O	UART5_RX	
E8	VDDMMC	Power		
E9	PJ12 *	I/O	GPIO_Output	UART5 Pwr
E10	VDDLDO	Power		
E12	PA13	I/O	DEBUG_JTMS-SWDIO	
E13	PA10	I/O	USART1_RX	
E14	PC9	I/O	SDMMC1_D1	
E15	PC7	I/O	USART6_RX	
F1	VLXSMPS	Power		
F2	VFBSMPS	Power		
F3	PI10	I/O	OCTOSPIM_P2_IO1	
F4	PC13 *	I/O	GPIO_Input	USART10 Flt
F5	VDDLDO	Power		
F6	VSS	Power		
F7	VDD	Power		
F8	VSS	Power		
F9	VDD	Power		

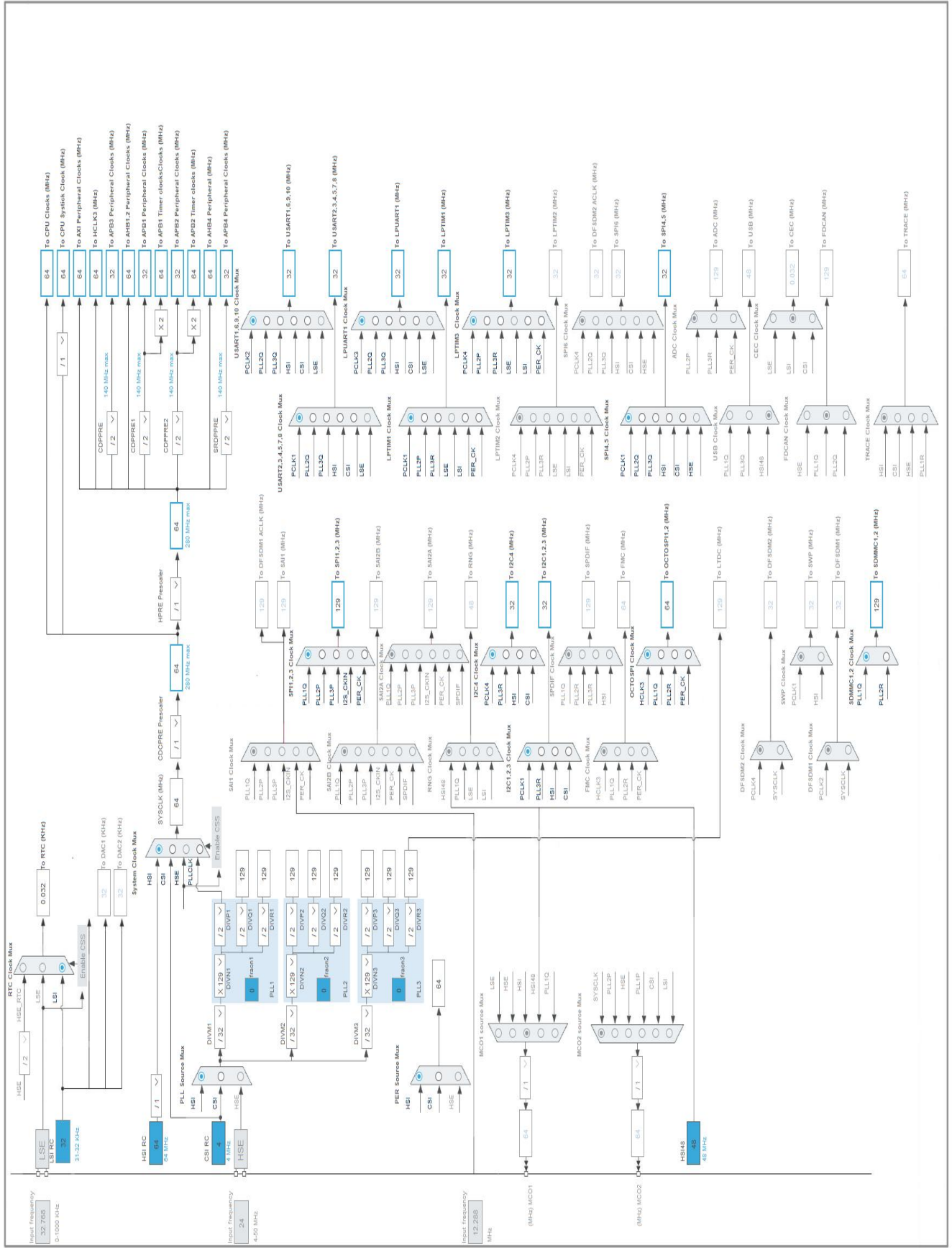
Pin Number TFBGA225	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F10	VSS	Power		
F11	VCAP	Power		
F12	PA9	I/O	USART1_TX	
F13	PC8	I/O	SDMMC1_D0	
F14	PC6	I/O	USART6_TX	
F15	PG8 *	I/O	GPIO_Output	USART6 Pwr
G1	VDDSMPS	Power		
G2	VSSSMPS	Power		
G3	PF1	I/O	I2C2_SCL	
G4	PF0	I/O	I2C2_SDA	
G5	PI11 *	I/O	GPIO_Output	USART10 Pwr
G6	VDD	Power		
G7	VDD	Power		
G8	VSS	Power		
G9	VDD	Power		
G10	VDD	Power		
G11	PA8	I/O	I2C3_SCL	
G12	PG7 *	I/O	GPIO_Output	USART1 Pwr
G13	PG6	I/O	OCTOSPIM_P1_NCS	
G14	PG5 *	I/O	GPIO_Input	USART1 Flt
G15	PG3 *	I/O	GPIO_Input	USART6 Flt
H1	PF2	I/O	OCTOSPIM_P2_IO2	
H2	PI12	I/O	OCTOSPIM_P2_IO3	
H3	PF4	I/O	OCTOSPIM_P2_CLK	
H4	PI14	I/O	OCTOSPIM_P2_NCLK	
H5	PI13 *	I/O	GPIO_Input	UART7 Flt
H6	VSS	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H11	VDD33_USB	Power		
J3	PF6	I/O	UART7_RX	
J4	PF7	I/O	UART7_TX	
J5	PC2 *	I/O	GPIO_Output	UART7 Pwr
J6	VDD	Power		
J7	VDD	Power		
J8	VSS	Power		
J9	VDD	Power		

Pin Number TFBGA225	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J10	VDD	Power		
K1	PF8	I/O	UART7_RTS	
K2	PF9	I/O	OCTOSPIM_P1_IO1	
K3	NRST	Reset		
K4	VREF-	Power		
K5	VSSA	Power		
K6	VSS	Power		
K7	VDD	Power		
K8	VSS	Power		
K9	VDD	Power		
K10	VSS	Power		
K11	PD13	I/O	UART9_RTS	
K12	PD14	I/O	UART8_CTS	
K13	PD15	I/O	UART8_RTS	
L5	VDDA	Power		
L8	VCAP	Power		
L9	PE12	I/O	SPI4_SCK	
L10	VDDLDO	Power		
L11	PH12 *	I/O	GPIO_Output	USART3 Pwr
L12	PD8	I/O	USART3_TX	
L13	PD10 *	I/O	GPIO_Input	USART3 Flt
L14	PD11	I/O	USART3_CTS	
L15	PD12	I/O	USART3_RTS	
M1	VSS	Power		
M2	PC1	I/O	OCTOSPIM_P1_IO4	
M3	PF10	I/O	OCTOSPIM_P1_CLK	
M6	PC4 *	I/O	GPIO_Input	uSD Detec
M13	PB13	I/O	UART5_TX	
M14	PB14 *	I/O	GPIO_Input	UART5 Flt
M15	PB15 *	I/O	GPIO_Output	USART3 Pwer
N2	PC3_C	I/O	OCTOSPIM_P1_IO0	
N4	PH3	I/O	OCTOSPIM_P1_IO5	
N6	PC5	I/O	OCTOSPIM_P1_DQS	
N9	PF15 *	I/O	GPIO_Output	UART9 Pwr
N10	PE14 *	I/O	GPIO_Input	UART9 Flt
N11	PE10	I/O	UART7_CTS	
N15	PD9	I/O	USART3_RX	
P1	PA0	I/O	USART2_CTS	
P2	PA1	I/O	OCTOSPIM_P1_IO3	

Pin Number TFBGA225	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
P7	PJ1	I/O	OCTOSPIM_P2_IO4	
P9	PF14	I/O	I2C4_SCL	
P10	PG1	I/O	UART9_TX	
P11	PE9	I/O	OCTOSPIM_P1_IO6	
P14	PH8	I/O	I2C3_SDA	
P15	PH11 *	I/O	GPIO_Input	USART3 Flt
R1	VSS	Power		
R5	PA7	I/O	OCTOSPIM_P1_IO2	
R7	PJ2	I/O	OCTOSPIM_P2_IO5	
R10	PG0	I/O	UART9_RX	
R15	VSS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	H7L3ABaseProject
Project Folder	C:\Users\gene\Documents\CPF\ElecEngr\STM32H7A3_SOM\H7L3ABaseProject
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_USART1_UART_Init	USART1
5	MX_USART2_UART_Init	USART2
6	MX_I2C2_Init	I2C2
7	MX_I2C3_Init	I2C3
8	MX_I2C4_Init	I2C4
9	MX_IWDG1_Init	IWDG1
10	MX_LPTIM1_Init	LPTIM1
11	MX_LPTIM3_Init	LPTIM3

Rank	Function Name	Peripheral Instance Name
12	MX_LPUART1_UART_Init	LPUART1
13	MX_UART4_Init	UART4
14	MX_UART7_Init	UART7
15	MX_UART8_Init	UART8
16	MX_UART9_Init	UART9
17	MX_USART6_UART_Init	USART6
18	MX_USART10_UART_Init	USART10
19	MX_OCTOSPI1_Init	OCTOSPI1
20	MX_OCTOSPI2_Init	OCTOSPI2
21	MX_RTC_Init	RTC
22	MX_SPI1_Init	SPI1
23	MX_SPI2_Init	SPI2
24	MX_WWDG1_Init	WWDG1
25	MX_FATFS_Init	FATFS
26	MX_SDMMC1_SD_Init	SDMMC1
27	MX_SPI4_Init	SPI4
28	MX_UART5_Init	UART5
29	MX_USART3_UART_Init	USART3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7A3/7B3
MCU	STM32H7A3LIHxQ
Datasheet	DS13139 Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

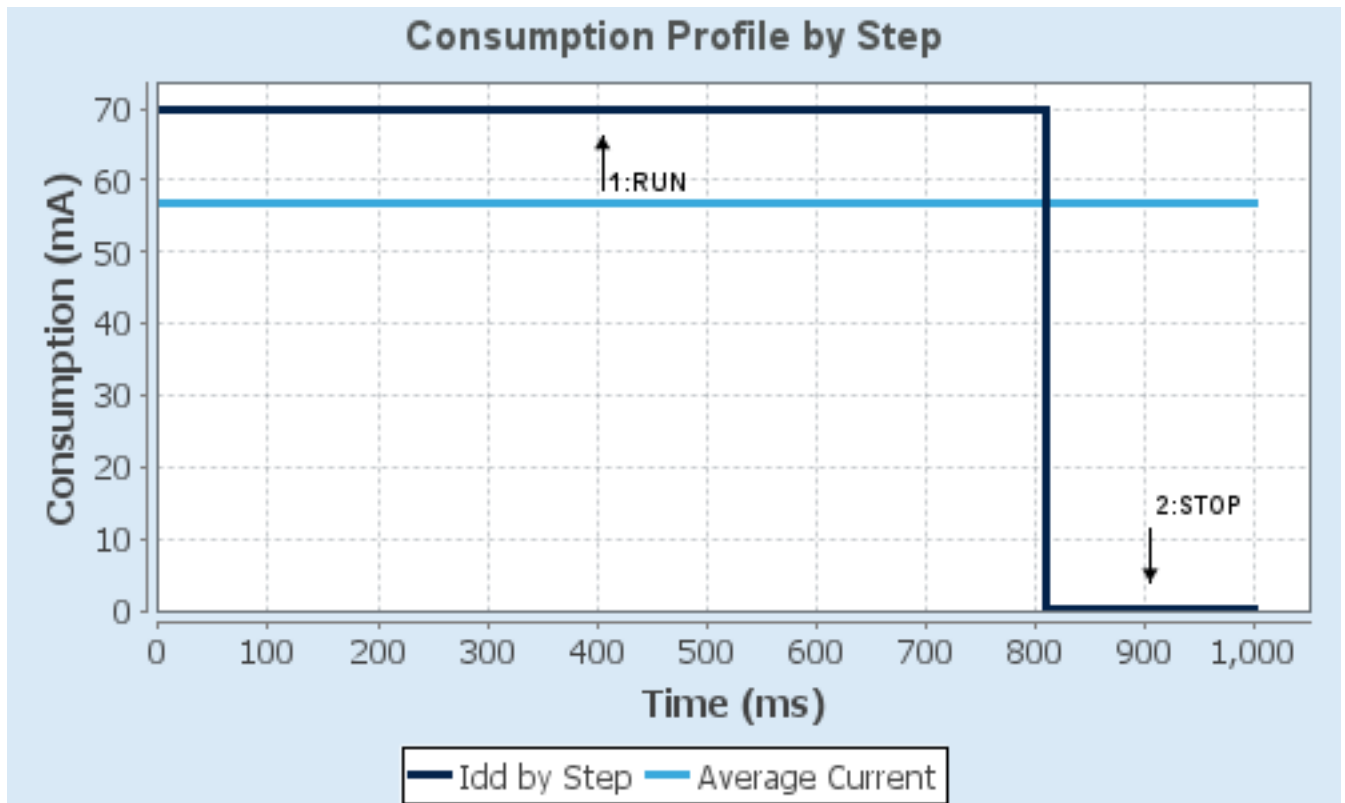
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0	SVOS5
SRDomain	DRUN	DSTOP
n/a	SRDRUN	SRDSTOP
Fetch Type	ITCM/DTCM/Cache	NA
CPU Frequency	280 MHz	64 MHz
Clock Configuration	HSE PLL	HSI Flash-ON
Clock Source Frequency	16 MHz	64 MHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	69.92 mA	263.82 μ A
Duration	810 ms	190 ms
DMIPS	599.0	0.0
Ta Max	115.56	124.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 s	Average Current	56.69 mA
Battery Life	2 days, 11 hours	Average DMIPS	599.2 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. DEBUG

Debug: JTAG (5 pins)

7.2. I2C2

I2C: I2C

7.2.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00707CBB *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.3. I2C3

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00707CBB *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. I2C4

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00707CBB *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.5. IWDG1

mode: Activated

7.5.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	4
IWDG window value	4095
IWDG down-counter reload value	4095

7.6. LPTIM1

Mode: Counts internal clock events

7.6.1. Parameter Settings:

Clock:

Clock Prescaler	Prescaler Div1
-----------------	----------------

Preload:

Update Mode	Update Immediate
-------------	------------------

Trigger:

Trigger Source	Software Trigger
----------------	------------------

7.7. LPTIM3

mode: Mode

7.7.1. Parameter Settings:

Clock:

Clock Prescaler	Prescaler Div1
-----------------	----------------

Preload:

Update Mode	Update Immediate
-------------	------------------

Trigger:

Trigger Source	Software Trigger
----------------	------------------

7.8. LPUART1

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	209700
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable

ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.9. OCTOSPI1

Mode: Octo SPI

Clock: Port1 CLK

Chip Select: Port1 NCS

Data Strobe: Port1 DQS (RWDS)

Data [3:0]: Port1 IO[3:0]

Data [7:4]: Port1 IO[7:4]

7.9.1. Parameter Settings:

Generic:

Fifo Threshold	1
Dual Quad mode	Disable
Memory Type	Micron
Device Size	32
Chip Select High Time	1
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	1
Sample Shifting	None
Delay Hold Quarter Cycle	Disable
Chip Select Boundary	1
Clock Chip Select High Time	0
Delay Block	Disable
Maximum Transfer	0
Refresh Rate	0

7.10. OCTOSPI2

Mode: HyperBus(TM)

Clock: Port2 CLK

HyperBus(TM) 1.8V Inverted Clock: Port2 NCLK

Chip Select: Port2 NCS

Data Strobe: Port2 DQS (RWDS)

Data [3:0]: Port2 IO[3:0]

Data [7:4]: Port2 IO[7:4]

7.10.1. Parameter Settings:

Generic:

Fifo Threshold	1
Dual Quad mode	Disable
Memory Type	HyperBus(TM)
Device Size	32
Chip Select High Time	1
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	1
Sample Shifting	None
Delay Hold Quarter Cycle	Disable
Chip Select Boundary	1
Clock Chip Select High Time	0
Delay Block	Disable
Maximum Transfer	0
Refresh Rate	0

HyperBus(TM):

RW Recovery Time	0
Access Time	0
Write Access Latency	Disable
Latency Mode	Variable

7.11. RCC

7.11.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 2 and 4 MHz
PLL1 clock Output range	Wide VCO range

7.12. RTC

mode: Activate Clock Source

mode: Activate Calendar

7.12.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

7.13. SDMMC1

Mode: SD 4 bits Wide bus

7.13.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0
Is external transceiver present ?	no

7.14. SPI1

Mode: Full-Duplex Master

7.14.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	64.5 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.15. SPI2

Mode: Full-Duplex Master

7.15.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	64.5 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.16. SPI4

Mode: Full-Duplex Master

7.16.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	16.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
Advanced Parameters:	
CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.17. SYS

Timebase Source: SysTick

7.18. UART4

Mode: Asynchronous

7.18.1. Parameter Settings:

Basic Parameters:	
Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1
Advanced Parameters:	
Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration
Advanced Features:	

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.19. UART5

Mode: Asynchronous

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.20. UART7

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.21. UART8

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.21.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
----------------	----------------------

Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.22. UART9

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.22.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable

Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.23. USART1

Mode: Asynchronous

7.23.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.24. USART2

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.24.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
-----------	--------

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.25. USART3

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.25.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.26. USART6

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.26.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.27. USART10

Mode: Asynchronous

7.27.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.28. WWDG1

mode: Activated

7.28.1. Parameter Settings:

Watchdog Clocking:

WWDG counter clock prescaler	1
WWDG window value	64
WWDG free-running downcounter value	64

Watchdog Interrupt:

Early wakeup interrupt	Disable
------------------------	---------

7.29. FATFS

mode: SD Card

7.29.1. Set Defines:

Version:

FATFS version R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
FS_LOCK (Number of files opened simultaneously)	2

7.29.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance	SDMMC1
Use dma template	Disabled
BSP code for SD	Generic

7.29.3. Platform Settings:

Detect_SDIO	PC4
-------------	-----

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PB4	DEBUG_JTRST	n/a	n/a	n/a	
	PA14	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	DEBUG_JTDO-SWO	n/a	n/a	n/a	
	PA15	DEBUG_JTDI	n/a	n/a	n/a	
	PA13	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
I2C2	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C3	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PH8	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C4	PB9	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF14	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
LPUART1	PB6	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	LPUART1_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	LPUART1_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
OCTOSPI1	PG14	OCTOSPI1_P1_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG6	OCTOSPI1_P1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF9	OCTOSPI1_P1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC1	OCTOSPI1_P1_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF10	OCTOSPI1_P1_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3_C	OCTOSPI1_P1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH3	OCTOSPI1_P1_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC5	OCTOSPI1_P1_DQS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA1	OCTOSPIM_P1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	OCTOSPIM_P1_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA7	OCTOSPIM_P1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
OCTOSPI2	PK5	OCTOSPIM_P2_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG10	OCTOSPIM_P2_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PK6	OCTOSPIM_P2_DQS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PK4	OCTOSPIM_P2_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI9	OCTOSPIM_P2_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI10	OCTOSPIM_P2_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	OCTOSPIM_P2_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI12	OCTOSPIM_P2_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	OCTOSPIM_P2_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI14	OCTOSPIM_P2_NCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PJ1	OCTOSPIM_P2_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PJ2	OCTOSPIM_P2_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SDMMC1	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PG9	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PI3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI4	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE12	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PD1	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART5	PB5	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART7	PF6	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF7	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF8	UART7_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE10	UART7_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART8	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	UART8_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD15	UART8_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART9	PD0	UART9_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	UART9_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG1	UART9_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG0	UART9_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PD4	USART2_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA0	USART2_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD11	USART3_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	USART3_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART6	PG15	USART6_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	USART6_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART10	PE3	USART10_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE2	USART10_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PI4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART8 Pwr
	PI5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UART8 Flt
	PJ15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USART2 Pwr
	PH15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CTD Flt
	PH14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CTD Pwr
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UART4 Flt

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PI6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART4 Pwr
	PJ14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USART2 Flt
	PI0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CTD Mode
	PH13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CTD DR
	PJ12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART5 Pwr
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USART10 Flt
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USART6 Pwr
	PI11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USART10 Pwr
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USART1 Pwr
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USART1 Flt
	PG3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USART6 Flt
	PI13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UART7 Flt
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART7 Pwr
	PH12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USART3 Pwr
	PD10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USART3 Flt
	PC4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	uSD Detec
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UART5 Flt
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USART3 Pwr
	PF15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UART9 Pwr
	PE14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UART9 Flt
	PH11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USART3 Flt

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Stream0	Peripheral To Memory	Low
USART1_TX	DMA1_Stream1	Memory To Peripheral	Low
USART2_RX	DMA1_Stream2	Peripheral To Memory	Low
USART2_TX	DMA1_Stream3	Memory To Peripheral	Low

USART1_RX: DMA1_Stream0 DMA request Settings:

Mode: **Circular ***
 Use fifo: **Enable ***
 FIFO Threshold: **Half Full ***
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte
 Peripheral Burst Size: Single
 Memory Burst Size: Single

USART1_TX: DMA1_Stream1 DMA request Settings:

Mode: Normal
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

USART2_RX: DMA1_Stream2 DMA request Settings:

Mode: Normal
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

USART2_TX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	Enable *
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. BDMA1 configuration

nothing configured in DMA service

8.4. BDMA2 configuration

nothing configured in DMA service

8.5. MDMA configuration

nothing configured in DMA service

8.6. NVIC configuration

8.6.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream1 global interrupt	true	0	0
DMA1 stream2 global interrupt	true	0	0
DMA1 stream3 global interrupt	true	0	0
Window watchdog interrupt	unused		
PVD and PVM interrupts through EXTI line	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
SDMMC1 global interrupt	unused		
UART4 global interrupt	unused		
UART5 global interrupt	unused		
USART6 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
UART7 global interrupt	unused		
UART8 global interrupt	unused		
SPI4 global interrupt	unused		
OCTOSPI1 global interrupt	unused		
LPTIM1 global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
HSEM1 global interrupt		unused	
LPTIM3 global interrupt		unused	
UART9 global interrupt		unused	
USART10 global interrupt		unused	
LPUART1 global interrupt		unused	
Window watchdog reset interrupt		unused	
ECC diagnostic Global Interrupt		unused	
OCTOSPI2 global interrupt		unused	

8.6.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
DMA1 stream2 global interrupt	false	true	true
DMA1 stream3 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware									
FATFS ✓									
System Core	Analog	Timers	Connectivity		Multimedia	Security	Computing	Trace and Debug	Power and Thermal
BDMA1		LPTIM1 ✓	I2C2 ✓	I2C3 ✓				DEBUG ✓	
BDMA2		LPTIM3 ✓	I2C4 ✓	LPUART1 ✓					
CORTEX_M7 ✓		RTC ✓	OCTOSPI1 ✓	OCTOSPI2 ✓					
DMA ✓			SDMMC1 ✓	SP1 ✓					
GPIO ✓			SPI2 ✓	SPI4 ✓					
IWDG1 ✓			UART4 ✓	UART5 ✓					
MDMA			UART7 ✓	UART8 ✓					
IVIC ✓			UART9 ✓	USART1 ✓					
RCC ✓			USART2 ✓	USART3 ✓					
SYS ✓			USART6 ✓	USART10 ✓					
WWDG1 ✓									

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00674683.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00463927.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00598144.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf

Application note http://www.st.com/resource/en/application_note/DM00393275.pdf

Application note http://www.st.com/resource/en/application_note/DM00354244.pdf

Application note http://www.st.com/resource/en/application_note/DM00315319.pdf

Application note http://www.st.com/resource/en/application_note/DM00407776.pdf

Application note http://www.st.com/resource/en/application_note/DM00356635.pdf

Application note http://www.st.com/resource/en/application_note/DM00380469.pdf

Application note http://www.st.com/resource/en/application_note/DM00354333.pdf

Application note http://www.st.com/resource/en/application_note/DM00395696.pdf

Application note http://www.st.com/resource/en/application_note/DM00431633.pdf

Application note http://www.st.com/resource/en/application_note/DM00493651.pdf

Application note http://www.st.com/resource/en/application_note/DM00535045.pdf

Application note http://www.st.com/resource/en/application_note/DM00525510.pdf

Application note http://www.st.com/resource/en/application_note/DM00536349.pdf

Application note http://www.st.com/resource/en/application_note/DM00623136.pdf

Application note http://www.st.com/resource/en/application_note/DM00625700.pdf

Application note http://www.st.com/resource/en/application_note/DM00660346.pdf

Application note http://www.st.com/resource/en/application_note/DM00600614.pdf

Application note http://www.st.com/resource/en/application_note/DM00606249.pdf

Application note http://www.st.com/resource/en/application_note/DM00725181.pdf