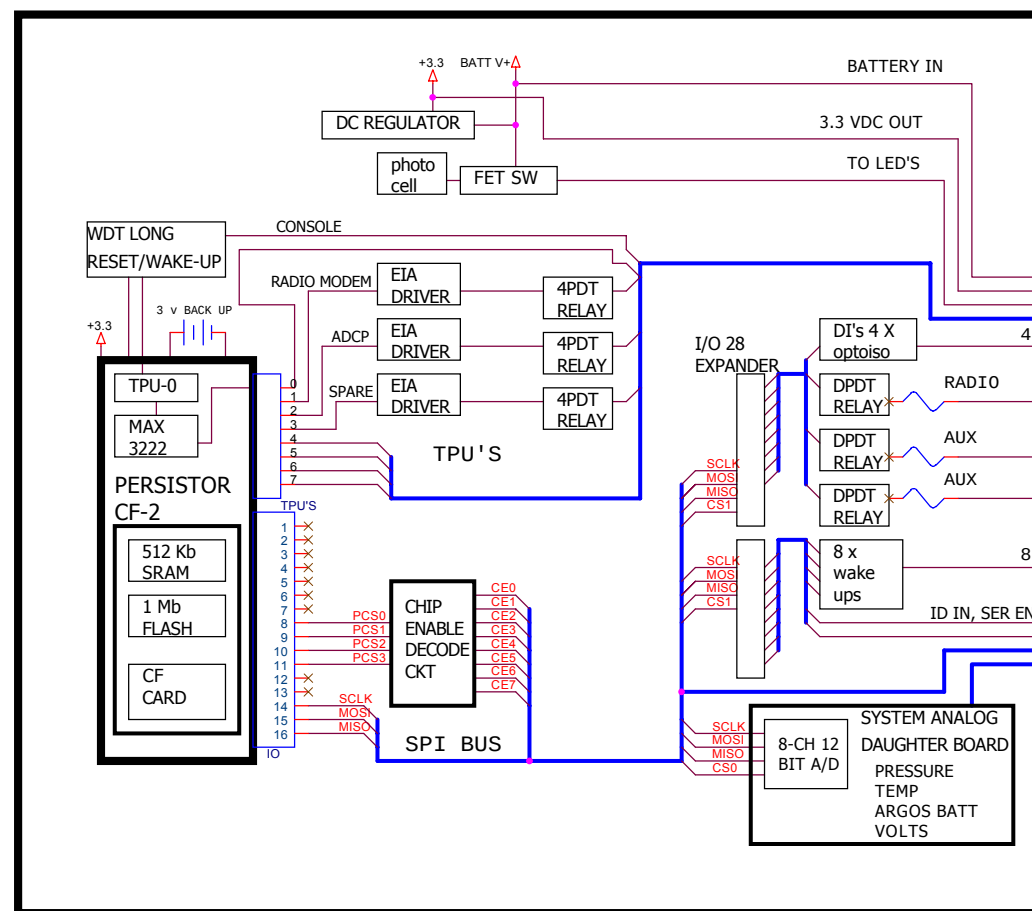
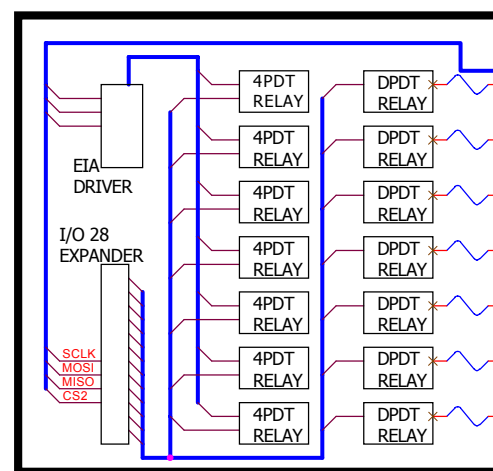


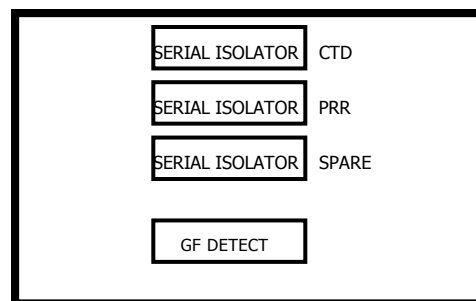


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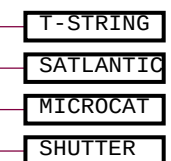
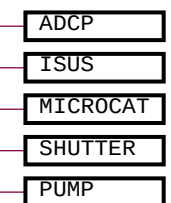
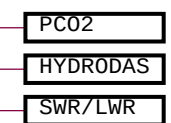
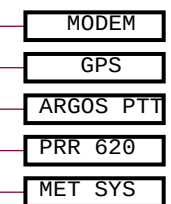
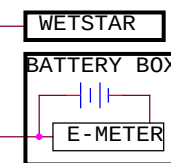
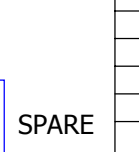
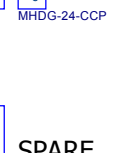
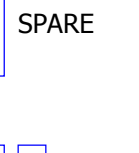
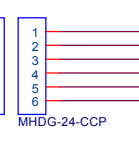
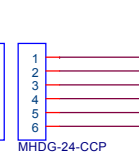
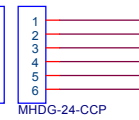
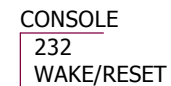
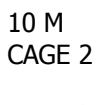
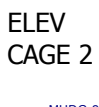
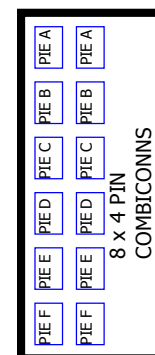
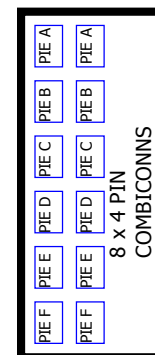
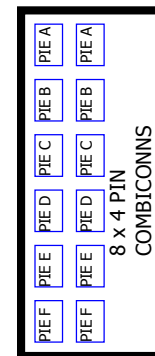
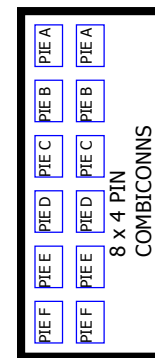
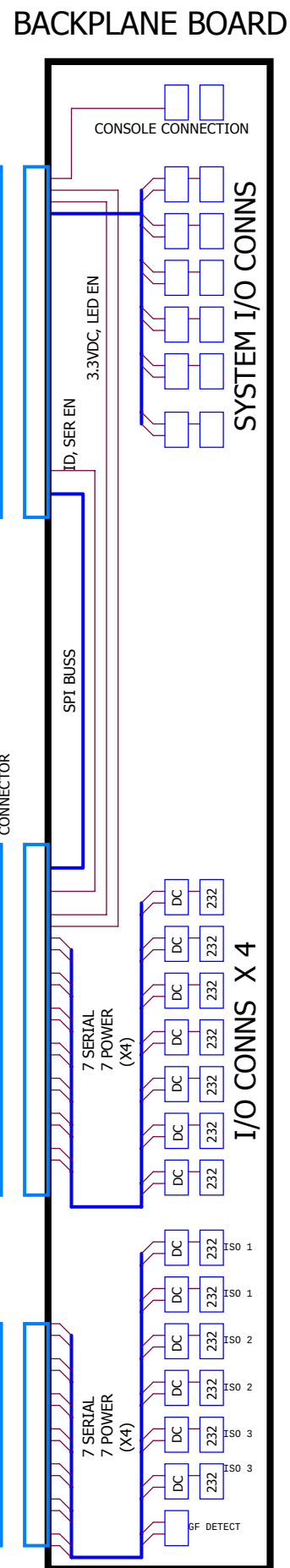
NOTE: NOT ALL CONNECTIONS SHOWN



IO BOARDS X 4

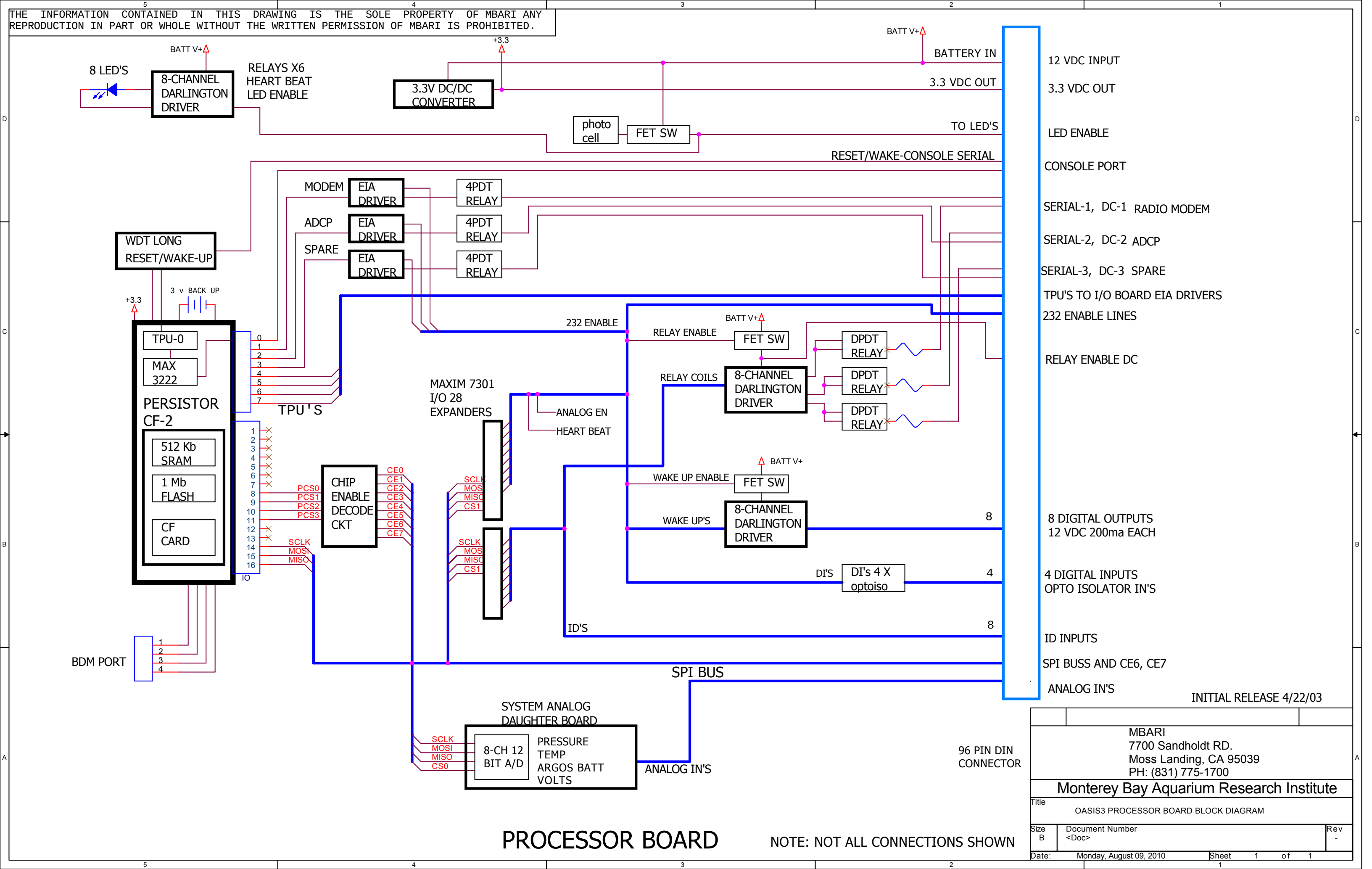


ACCESSORY BOARD



4/22/03

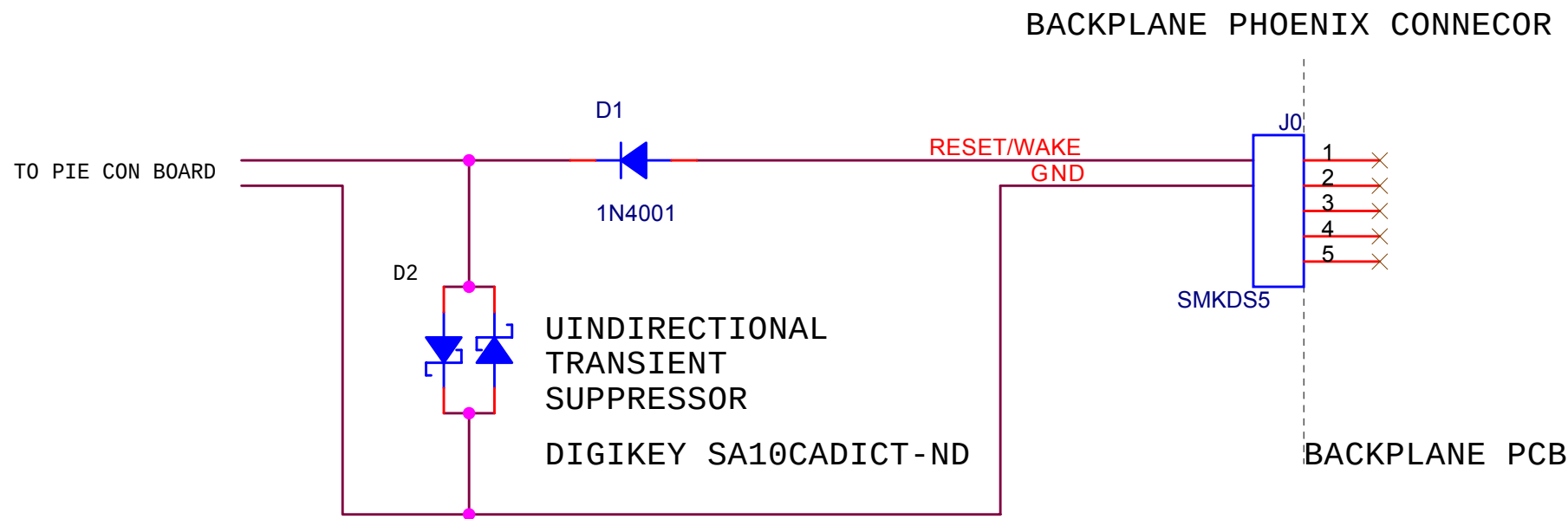
B	CORRECT ERRORS			4/22/03	
A	UPDATE TO AS BUILT			3/6/03	
MBARI 7700 Sandholdt RD. Moss Landing, CA 95039 PH: (831) 775-1700					
Monterey Bay Aquarium Research Institute					
Title OASIS3 SYSTEM BLOCK DIAGRAM					
Size C	Document Number OASIS3.SCH				Rev B
Date:	Monday, August 09, 2010		Sheet	1	of 1



PROCESSOR BOARD

NOTE: NOT ALL CONNECTIONS SHOWN

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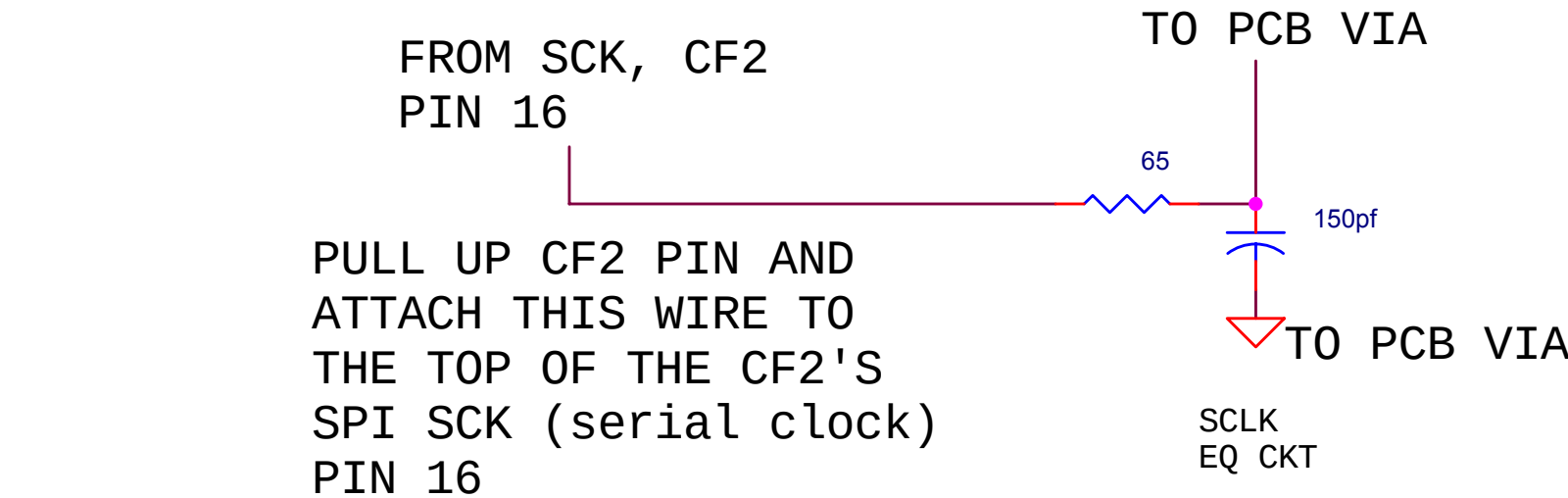
Monterey Bay Aquarium Research Institute

Title
OASIS3 PROCESOR BOARD RESET/WAKE PROTECTION CIRCUIT

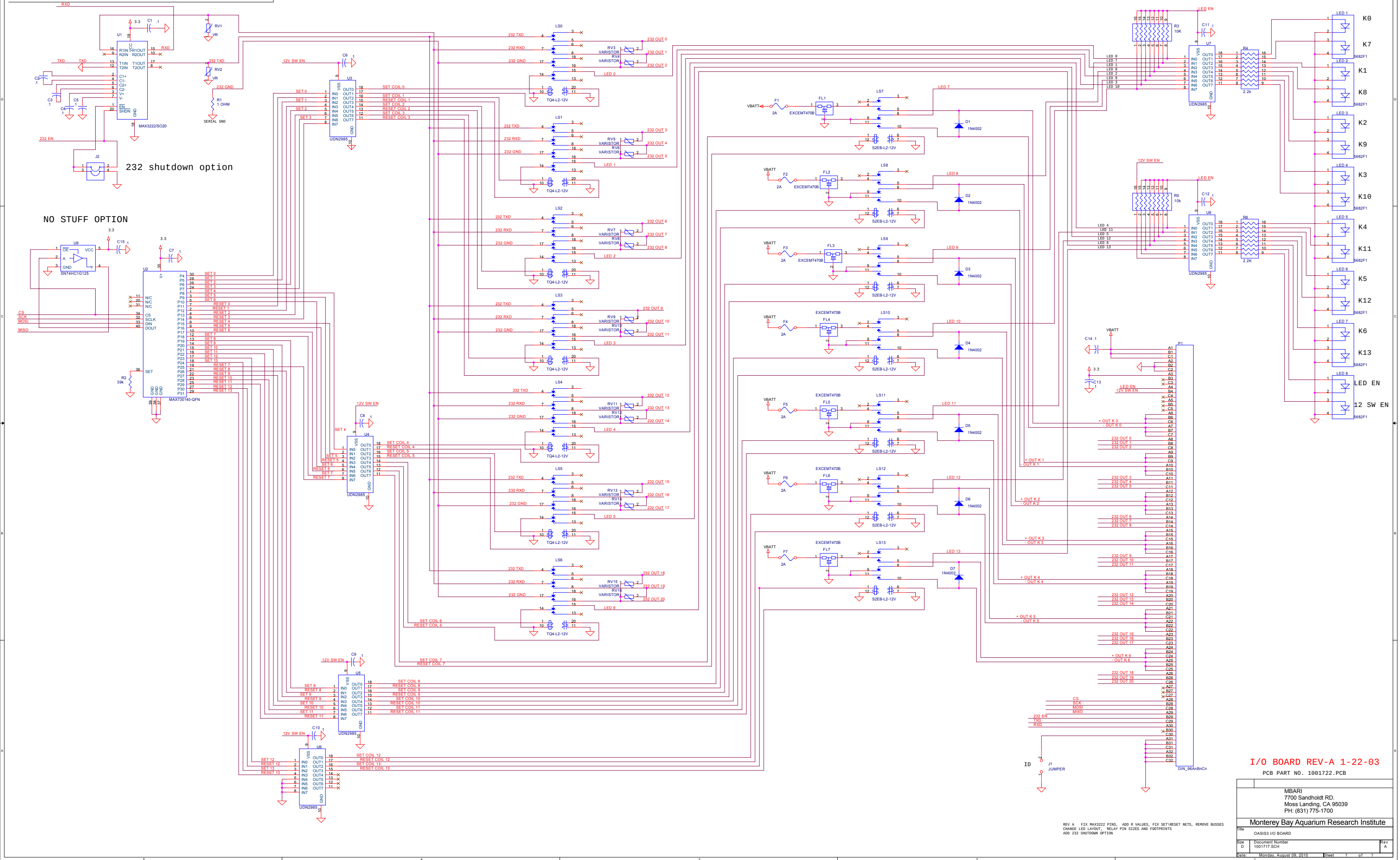
Size A	Document Number <Doc>	Rev -
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Date:	Monday, August 09, 2010	Sheet	1	of	1
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PROCESSOR BOARD

I/O BOARD

I/O BOARD

I/O BOARD

I/O BOARD

SLOT 5
(SPARE)

SLOT 6
(SPARE)

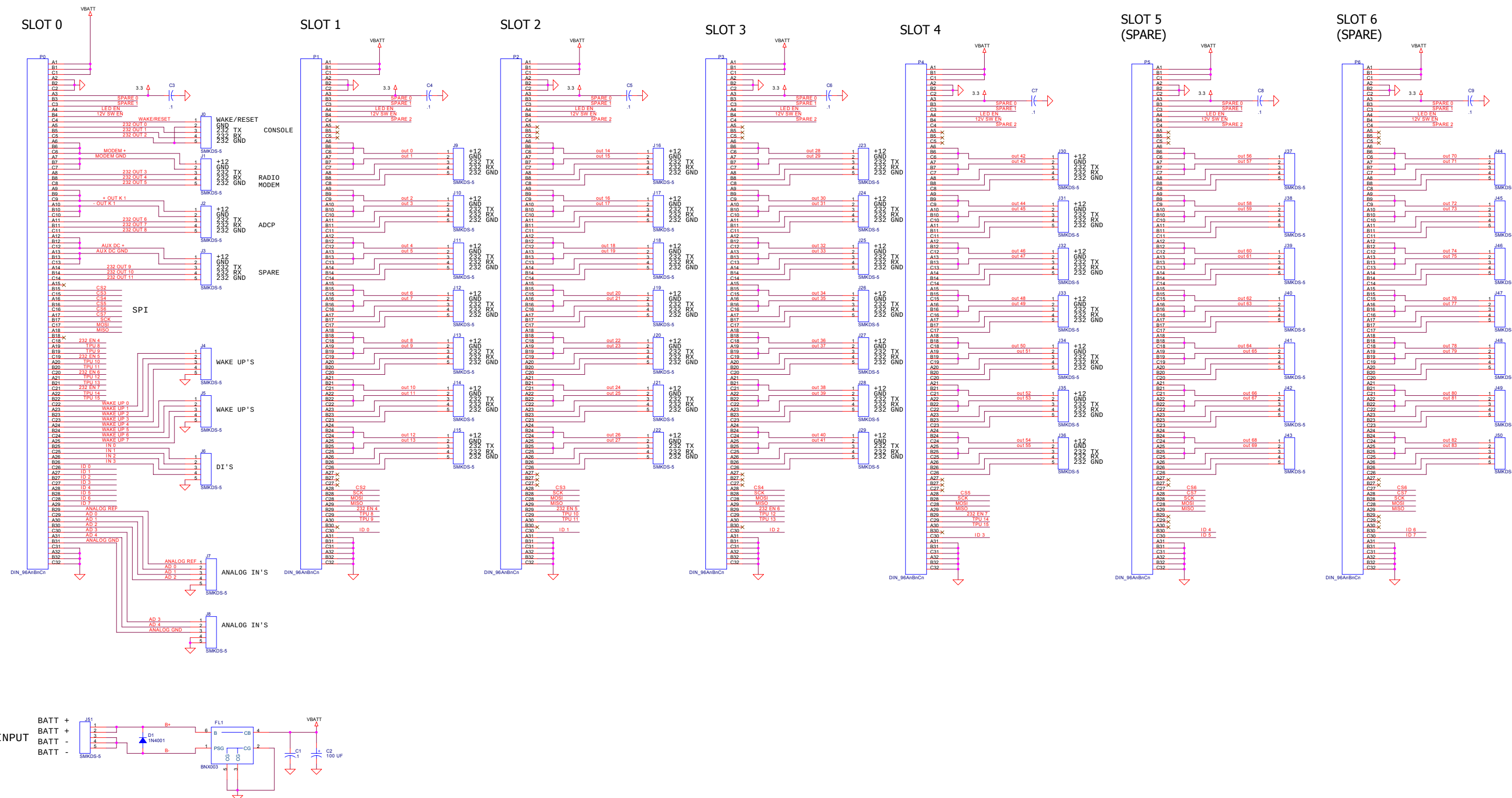
DC INPUT

REV A 1/21/03

PCB PART 1001723.PCB
NOTE: PCB LAYOUT IS REV-C

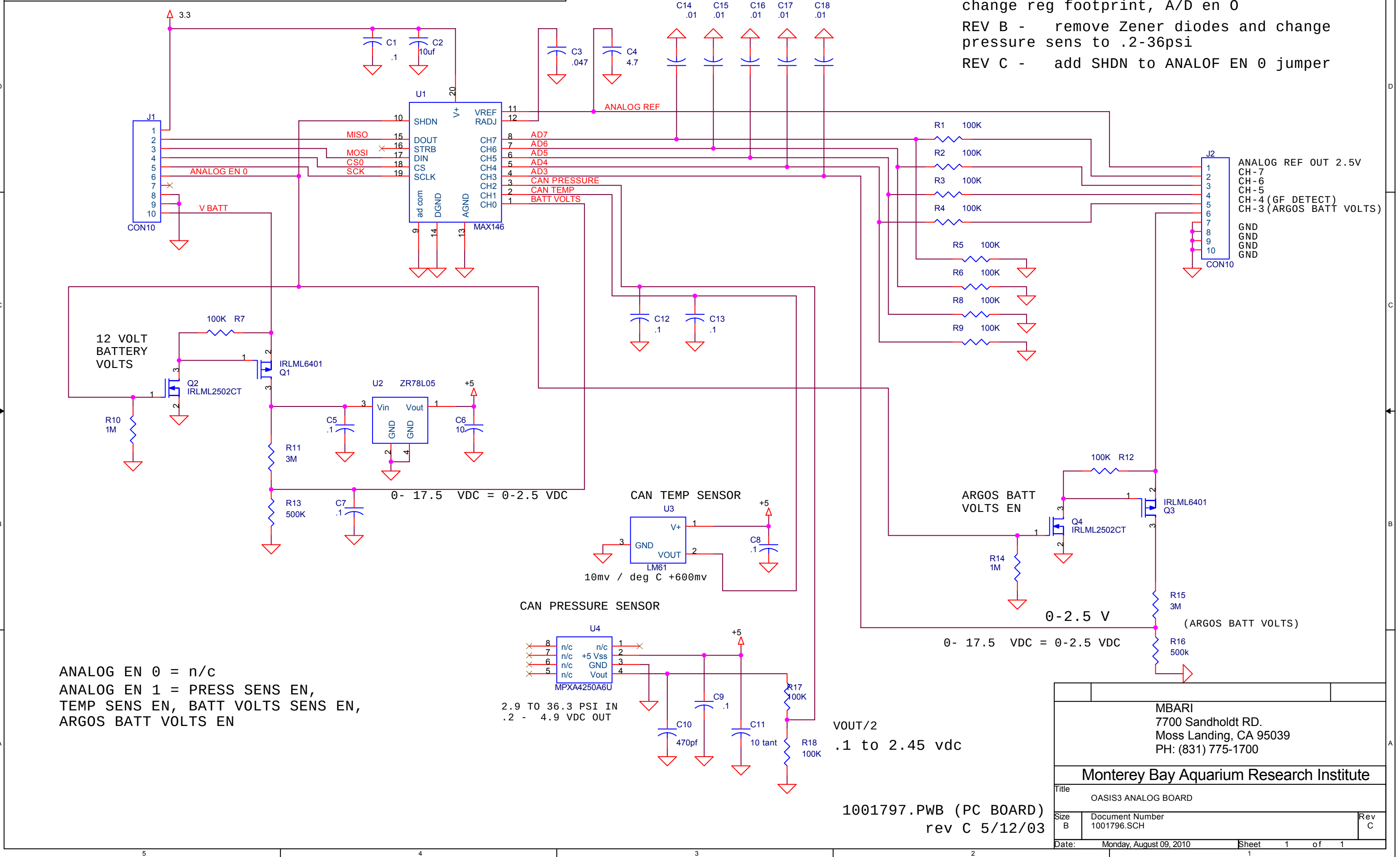
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Monterey Bay Aquarium Research Institute		
File	OASIS3 BACKPLANE BOARD	Rev
Size	D	Document Number
1001718.SCH		1
Date	Monday, August 09, 2010	Sheet
0	of	1

REV A ADD .1 BYPASS CAPS, CHANGE TO POL CAP C2
, CHANGE SMKDS5 FOOTPRINT HOLE SIZE TO .052
CORRECTED SLOT 6 SPI BUSS CONNECTION LOCATION

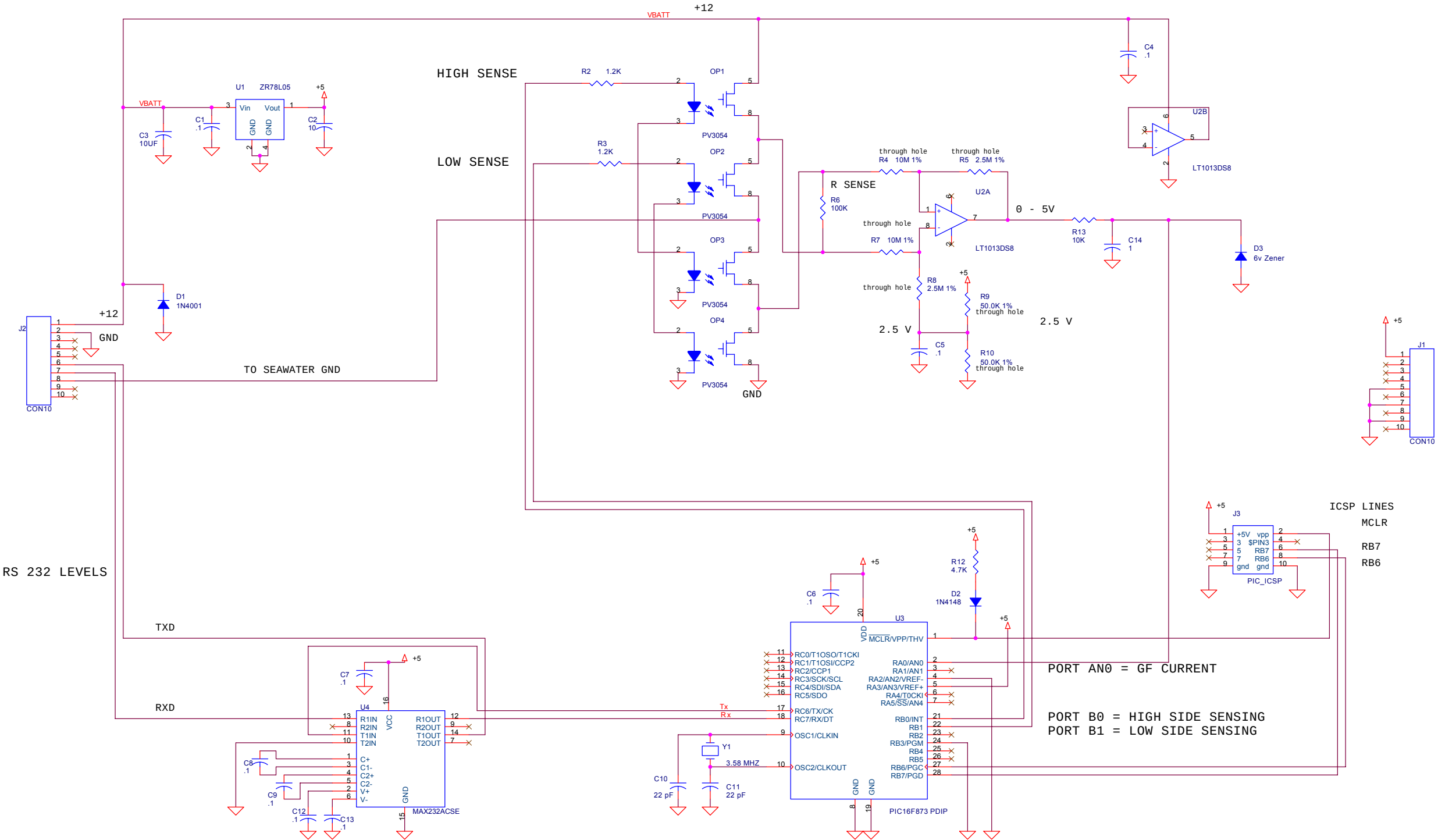


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REV A - ADD INPUT CAPS, CHANGE TEMP PART
change reg footprint, A/D en 0
REV B - remove Zener diodes and change
pressure sens to .2-36psi
REV C - add SHDN to ANALOF EN 0 jumper



GAIN = 4
R SENSE = 500 OHM
OFFSET V = 2.5 VDC
+/- .625 VDC = 0 - 5 VDC OUT
+/- 1.25 ma = 0 - 5 VDC OUT
RES AT 10 BITS, 1 COUNT = 2.4 ua



RS 232 LEVELS

PORT AN0 = GF CURRENT

PORT B0 = HIGH SIDE SENSING
PORT B1 = LOW SIDE SENSING

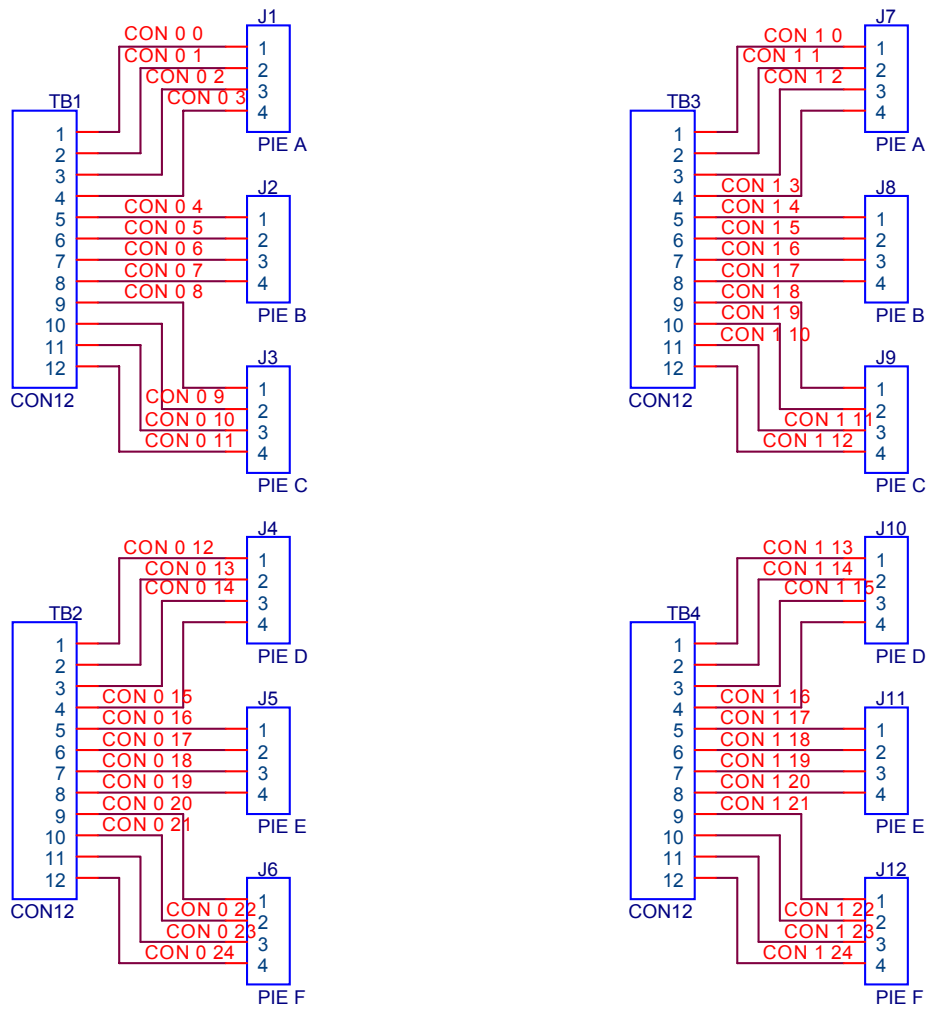
8/21/03 INITIAL RELEASE

12/2/03 CHANGE LT1013 PINOUT, ADD ICSP HEADER
ADD +5 TO ICSP ON J1

PCB PART _____ PCB REV-A

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Title OASIS3 AC GROUND FAULT BOARD		
Size C	Document Number <Doc>	Rev A
Date: Monday, August 09, 2010 Sheet 1 of 1		

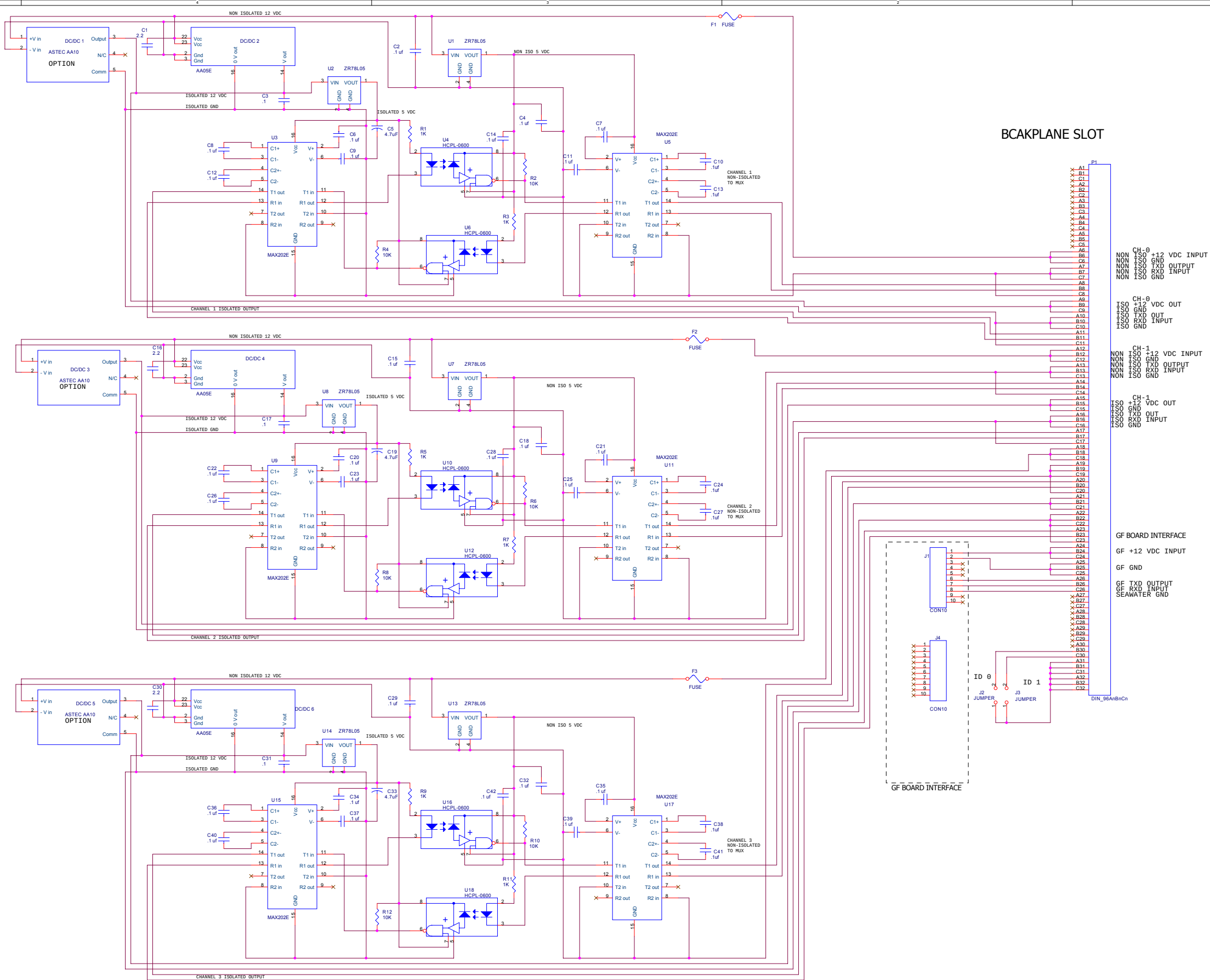
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1001720.PCB

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Size B	Document Number 1001719.SCH	Rev -
Date:	Monday, August 09, 2010	Sheet 0 of 1



PCB PART NO. 1001722.PCB

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OASIS3 I/O BOARD	
Size D	Document Number 1001717.SCH
Date Monday, August 09, 2010	Sheet 1 of 1
Rev C	

ACCESSORY BOARD BOARD REV C

4-17-03