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A Backside Contact ISFET with a Silicon–Insulator–Silicon Structure

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Abstract

A backside contact-type ISFET was developed applying a silicon–insulator–silicon (SIS) structure. A round etching procedure for edges of both silicon islands and backside contact wells enabled adequate photoresist mask layers on them, which were essential to the entire chip fabrication process. FETs formed on the chip have flat gate configurations, and they were insulated from each other and also from the side walls of the chip with a silicon dioxide layer. Making the most of this feature, the chips were encapsulated into flat contact type test probes, using a simple cast molding of three different resins. The gate leakage currents for the probes were under 10^{-11} A, which showed that the insulation of the SIS structure and the encapsulation were satisfactory. The leakage current changes for the probes were checked by elapsing in boiling water. The test results suggested that an ISFET probe, which can be sterilized in boiling water and has mechanical strength, would be available.

Introduction

It has been reported many times that encapsulation is one of the critical problems for ISFETs [1–3]. Planer type devices, which have been developed recently, have their sensing gates and electrodes on the same surface. Therefore, molding resin must be piled up on the electrodes, to encapsulate the chip while leaving the gates open so they can be exposed to solutions. However, these processes are not suitable for mass production and cause an obstructive bump near the gates. To avoid these problems, it is effective to move the electrodes onto the backside of the chip [1, 4, 5]. However, these proposed chips still have points to be improved, i.e. deep-set gate configuration [4] and uninsulated chip side wall [5]. From these points of view, the authors developed a new backside contact ISFET chip, applying the silicon–insulator–silicon structure [4].

Chip Fabrication

Figure 1 shows the chip structure. A pair of FETs and terminal buttons are integrated on a chip. The sensing gate area is arranged on the top of each FET island. The buttons are assumed to be used for a pseudo-reference electrode or some gate electrode terminals. Contact electrodes are on the back of the FETs and buttons. A bank, which surrounds these functional parts, is used as a resin flow stopper. This part is not essential for the chip, but is effective for cast molding, as shown later.

The chip fabrication process is shown in Fig. 2. First, an SIS structure wafer was prepared, using the silicon direct bonding method [6]. p-type silicon wafers, which have commercial level mirror surfaces, were thermally oxidized to form about 500 nm thick oxide layers on their surfaces. After washing with the usual acids and peroxide, a pair of wafers was placed in contact with their mirror

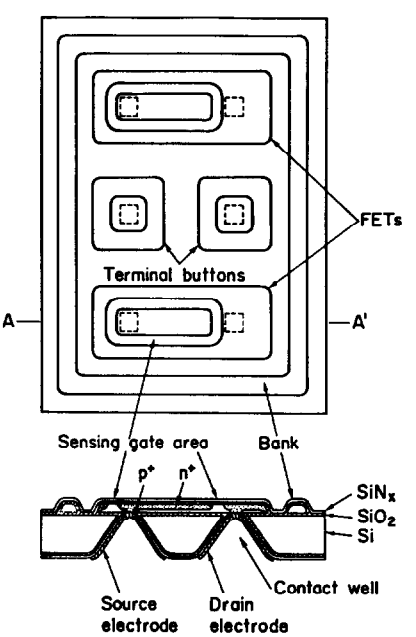

Fig. 1. ISFET chip structure (2.2 × 1.6 × 0.2 mm); (a) top view, (b) A–A′ cross-sectional view.

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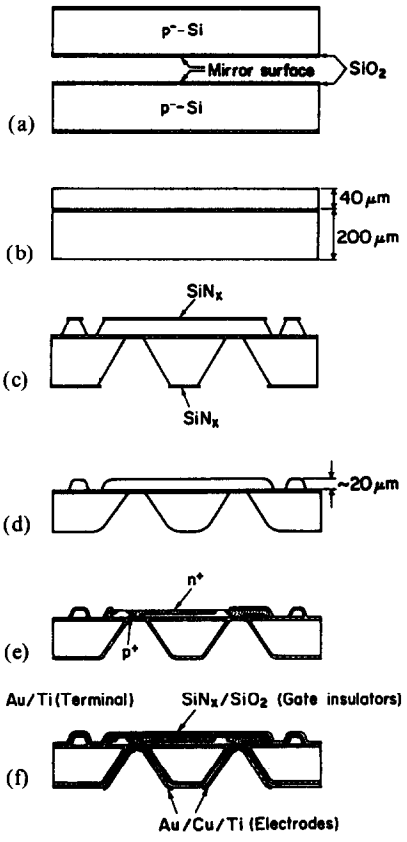

Fig. 2. Chip fabrication process: (a) direct wafer bonding, (b) adjust wafer thickness, (c) anisotropically etch FET islands and contact wells, (d) round etching, (e) phosphorus and boron diffusion, (f) gate oxidation, silicon nitride passivation and metallization.

surfaces touching each other, and heat-treated at 1100 °C in nitrogen gas atmosphere to form a direct chemical bond at the interface. The interface tensile strength was reported to be up to 100 kg/cm^2, which is almost the same as that of a bulk silicon crystal [6]. The bonded wafer surfaces were mechanically ground and polished to dimensions shown in Fig. 2(b).

Next, silicon islands and contact wells were shaped on both sides of the wafer by hydrazine anisotropic etching, using silicon nitride masks (Fig. 2(c)) [7]. Then, the masks were removed by chemical dry etching, preserving the intermediate silicon dioxide layer. After that, the edges of both the islands and wells were rounded by a HF–HNO_3 etchant (Fig. 2(d)) [8]. This etching could be sufficiently accomplished for rounding without worrying about damage to the well bottom silicon layers, because the intermediate silicon dioxide layer acted as an etching stopper. At the same time, island thicknesses were reduced to about 20 μm. The thicknesses could not be controlled

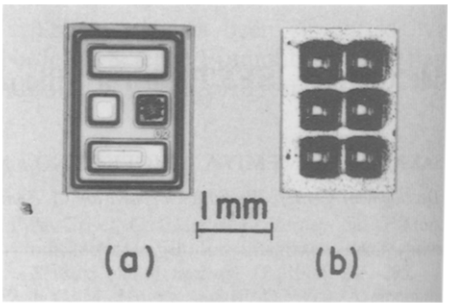

Fig. 3. ISFET chip microphotograph: (a) top view, (b) backside view.

precisely, because the etching rate for the etchant was fast, more than 1 μm/s. However, thicknesses within 10–30 μm were permissible to diffuse the n^+ layers from both sides of the island until they were connected together, retaining sufficient diaphragm strength. The edge rounding procedure and adoption of an extremely low viscosity photoresist at the PEP process made it possible to form adequate photoresist mask layers on both the silicon islands and contact wells with good step coverages. They were essential for making contact holes and other patterns on the chip. Most of our efforts to develop the entire chip fabrication process were made in these edge rounding and PEP steps. After that, impurity diffusions were implemented, as shown in Fig. 2(e). Phosphorus was deeply diffused from both sides of form the n^+ layers, as mentioned above. The boron diffused p^+ layer was formed around the source contact n^+ layer to act as a channel stopper and substrate contact.

Next, a 100 nm thick silicon dioxide layer was formed on the gate area and 150 μm thick silicon nitride layers were deposited on both sides of the chip by LPCVD. Finally, electrodes were deposited and heat treated to form ohmic contacts to the silicon layers. They were gold/titanium for the terminal on the button, and gold/copper/titanium for the contact pads. Completed chip microphotographs are shown in Fig. 3. The terminal electrode was formed only at the right side button, but it shrank by excessive heat treatment.

Probe Assembling

Figure 4 shows a test probe structure used for measuring the chip characteristics. First, 0.12 mm diameter fluorinated ethylene propylene (FEP) wires were directly connected to the contact electrodes, using gold–tin solder cream. Soldering was rather easy owing to the existence of a well dimple. After that, the chip was set at the bottom

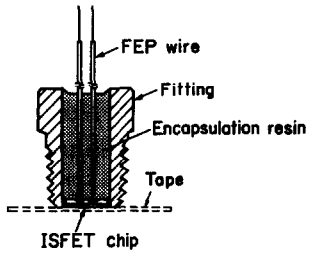

Fig. 4. Test probe cross-sectional view (tape was removed after molding).

of a metal fitting using polyimide adhesive tape, and encapsulation resin was poured from the topside to cast mold it. This molding process became possible because the chip does not need piled up protection on the gate side surface of the chip. Cast molding is one of the suitable processes for mass production. Its merit is that various molding materials can be adopted. Making the most of this feature, a thermosetting polybutadiene (Japan Hydrazine, Polybec W-2104), which has little thixotropic character before hardening, was tested for encapsulation. Conventional epoxide resin (Ciba-Geigy, Araldite AW106 + HV953U) and silicone resin (Toshiba Silicone, TSE-399) were also tested.

Characteristics

The FET characteristics for the polybutadiene probe are shown in Fig. 5. Measurements were carried out in a pH 6.86 phosphate buffer solution with the SCE as a reference electrode. Typical FET saturation curves were observed for the drain-source current (I_{DS}). Mutual conductance

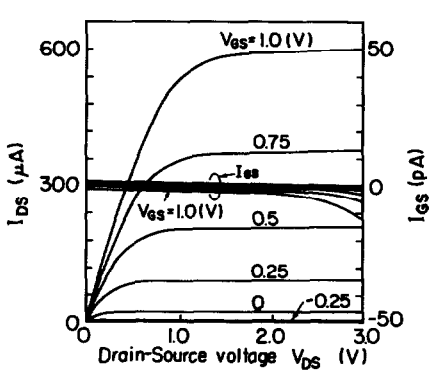

Fig. 5. Source-drain current (I_{DS}) and gate leakage current (I_{GS}) characteristics *vs.* source-drain voltage (V_{DS}) and gate-source voltage (V_{GS}) for polybutadiene molded probe.

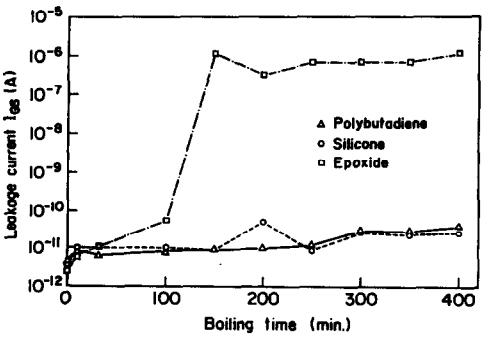

Fig. 6. Leakage current changes in sensor probes elapsed in boiling water.

was about 0.8 mS. The leakage currents from the SCE to the source (I_{GS}) were negligible at the usual driving condition in which the drain-source voltage (V_{DS}) was 2.0 V and the SCE-source voltage (V_{GS}) was about 0.5 V. Under this condition, the pH sensitivity for the probe was about 52 mV/pH within pH 2–10. These characteristics for the cases of silicone and epoxide were almost the same as that of polybutadiene.

Flat and non-obstructive swelling shapes for the probe are thought to be effective for various biological and medical applications [5, 9]. Sterilizing the probe by boiling is necessary when used for these purposes. Probe reliability was checked for this point. Figure 6 shows the I_{GS} change for probes which were elapsed in boiling water. The leakage current measurements were carried out in the phosphate solution at room temperature after each boiling period. The applied V_{GS} was swept from −2.5 to +1.0 V to the source and drain connected together, and the values at 1.0 V are plotted in the Figure. The epoxide probe I_{GS} increased abruptly up to 10^{-6} A after 100 min boiling, and swelling of the encapsulating resin was observed. On the other hand, the silicone and polybutadiene probe I_{GS} stayed at the 10^{-11} A level after 400 min treatment. Comparing the two probes, the silicone probe increase was rather small, but its weak mechanical strength is considered to become a problem in actual use. Though polybutadiene cannot yet be concluded as the best, it is thought that a practical probe will become applicable by trying out various molding materials.

Conclusions

A backside contact ISFET, applying the SIS structure, has been developed to solve the encapsulation related ISFET problems. Adding the sili-

con direct bonding method, the edge rounding procedure made the entire fabrication process possible. In the chip, FETs have flat gate configurations, and they are not only insulated from each other but also from the side walls of the chip with the silicon dioxide layer. Owing to these features, the chips were encapsulated into flat contact type probes by mass productive resin cast molding. It is obvious that other similar methods, for example injection molding and compression molding, are also applicable. A merit of these methods is that various encapsulating resins can be adopted. The negligible leakage currents of the tested probes, under 10^{-11} A, showed that the insulation of both the SIS structure and the encapsulation are satisfactory. The reliability test results indicated that a ISFET probe, which could be sterilized in boiling water still maintaining mechanical strength, would be available by applying the developed chip and encapsulation.

Acknowledgements

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