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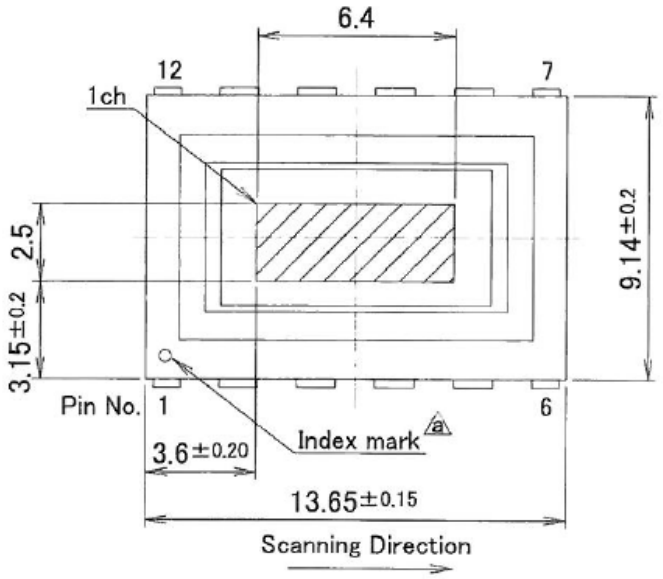
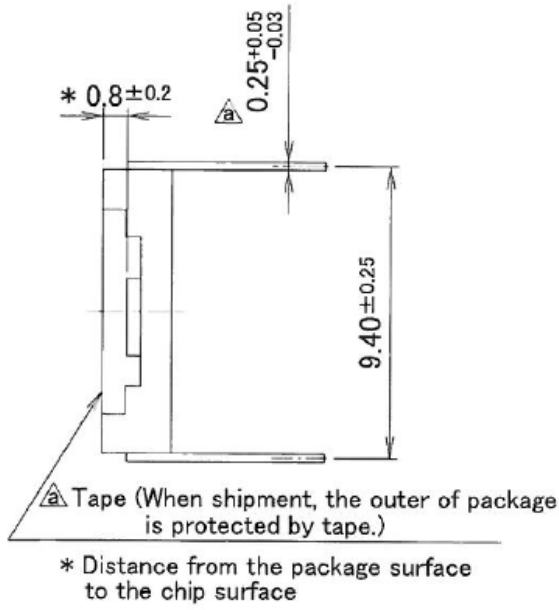
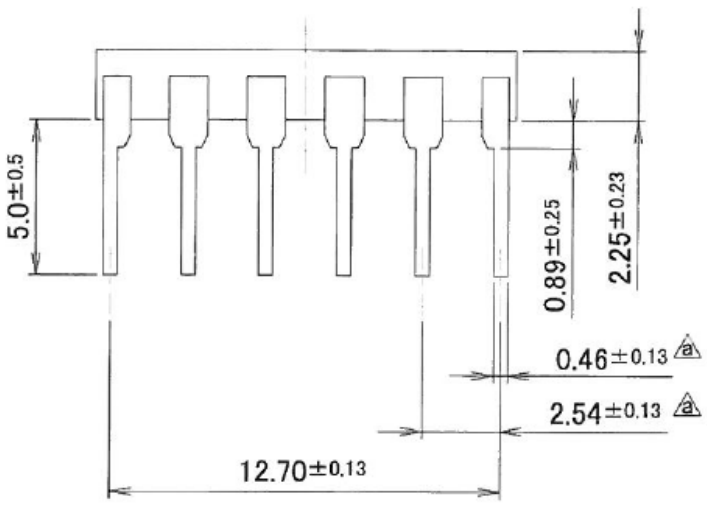
4. Dimensional outline (Unit : mm)







Pin Connection	
1	Vss
2	Vscg
3	Vsub
4	Vscd
5	NC
6	Vss
7	Active Video
8	Dummy Video
9	EOS
10	ϕ2
11	ϕ1
12	ϕst

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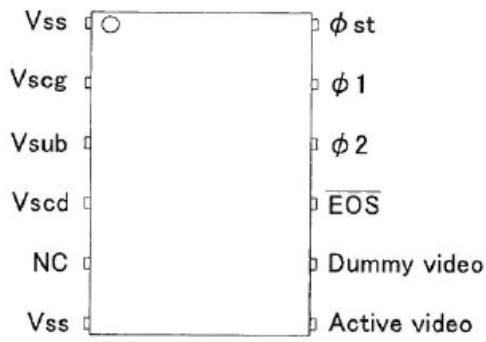
5. Pin-out and recommended operating conditions



Vss, Vsub, and NC should be grounded.

Terminals	Input or output	Description
ϕ1, ϕ 2	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. As the video output signal is obtained synchronized with the rise of ϕ2, the video data rate is equal to the clock pulse frequency.
ϕ st	Input (CMOS logic compatible)	Pulse to start operation of the MOS shift register. The time interval between start pulses is equal to the signal accumulation time.
Vss	Passive node	Connected to the anode of each photodiode. This should be grounded.
Vscg	Input	Used for restricting blooming. This should be set at the base line of each input pulse and is normally the ground level.
Vscd	Input	Used for restricting blooming. This should be biased at a voltage equal to the video bias at all times.
Active video	Output	Video output signal. A positive voltage should be applied to the video line which connects the photodiode cathodes so that each photodiode is reverse-biased. It is recommended that the video bias be 2V when the amplitude of ϕ1, ϕ2 and ϕst is at 5V.
Dummy video	Output	This has the same structure as the active video, but is not connected to the photodiodes, so only spike noise is output. It should be biased at a voltage equal to the active video line. When in use otherwise, it should be open circuited.
Vsub	Passive node	Connected to the silicon substrate. This should be grounded.
$\overline{\text{EOS}}$	Output (CMOS logic compatible)	This should be pulled up to 5V using a 10 kΩ resistor. Negative polarity. The end of scan signal is obtained synchronized with ϕ2 right after the last photodiode is addressed.
NC		No connection. These should be grounded.

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6. Timing chart