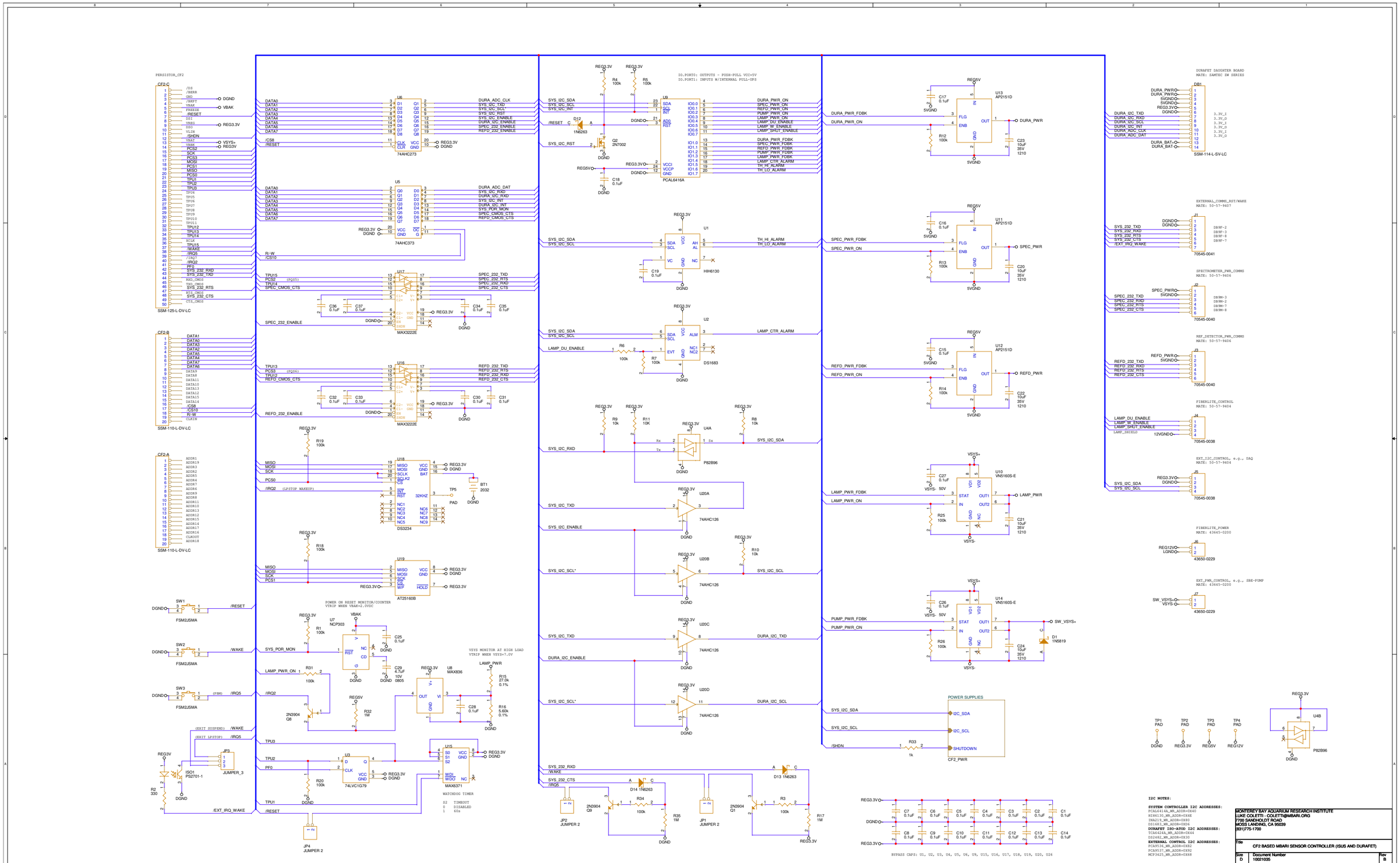

PERSISTOR_CF2
SSM-125-L-DV-LC
SSM-110-L-DV-LC
SSM-110-L-DV-LC
74AHC273
74AHC373
MAX3222E
MAX3222E
DS3234
AT25160B
PCAL6416A
HIH6130
DS1683
P82B96
74AHC126
74AHC126
74AHC126
74AHC126
74AHC126
AP2151D
AP2151D
AP2151D
VN5160S-E
VN5160S-E
POWER SUPPLIES
CF2_PWR
DURAFET DAUGHTER BOARD
MATE: SAMTEC IM SERIES
SSM-114-L-SV-LC
EXTERNAL_COMMS_RST/WAKE
MATE: 50-57-9407
70545-0041
SPECTROMETER_PWR_COMMS
MATE: 50-57-9406
70545-0040
REF_DETECTOR_PWR_COMMS
MATE: 50-57-9406
70545-0040
FIBERLITE_CONTROL
MATE: 50-57-9404
70545-0038
EXT_I2C_CONTROL, e.g., DAQ
MATE: 50-57-9404
70545-0038
FIBERLITE_POWER
MATE: 43645-0200
43650-0229
EXT_PWR_CONTROL, e.g., SBE-PUMP
MATE: 43645-0200
43650-0229
POWER ON RESET MONITOR/COUNTER
VTRIP WHEN VBAK=2.0VDC
VSYS MONITOR AT HIGH LOAD
VTRIP WHEN VSYS=7.0V
WATCHDOG TIMER
S2 TIMEOUT
0 DISABLED
1 60s
BYPASS CAPS: U1, U2, U3, U4, U5, U6, U9, U15, U16, U17, U18, U19, U20, U26
I2C NOTES:
SYSTEM CONTROLLER I2C ADDRESSES:
PCAL6416A_WR_ADDR=0X40
HIH6130_WR_ADDR=0X4E
INA219_WR_ADDR=0X80
DS1683_WR_ADDR=0X06
DURAFET ISO-ATOD I2C ADDRESSES:
TCA6424A_WR_ADDR=0X44
DS2482_WR_ADDR=0X30
EXTERNAL CONTROL I2C ADDRESSES:
PCA9536_WR_ADDR=0X82
PCA9537_WR_ADDR=0X92
MCP3425_WR_ADDR=0X68
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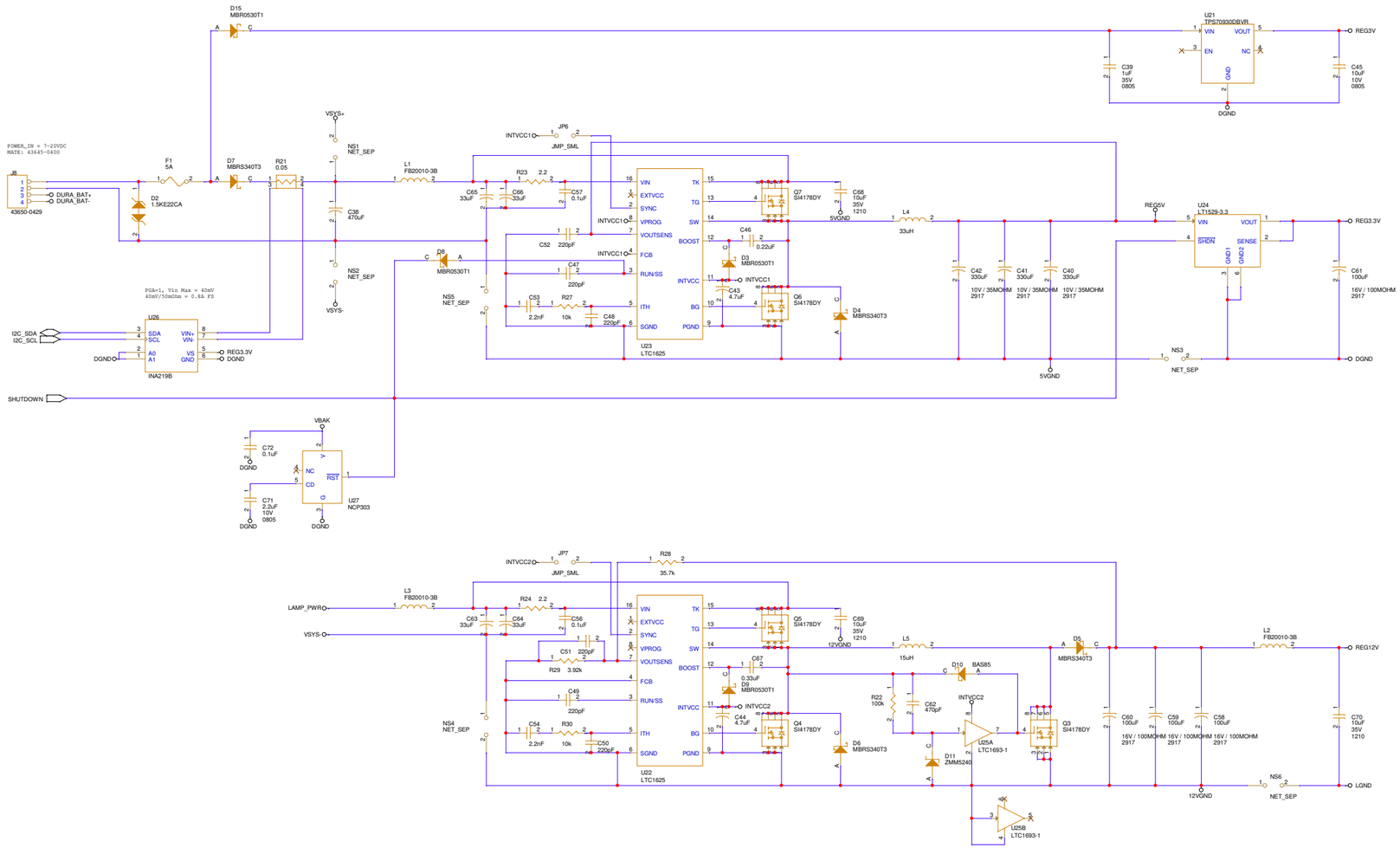
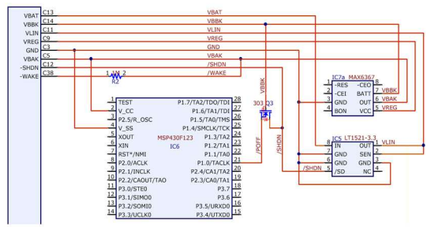
CF2 BASED MBARI SENSOR CONTROLLER (ISUS AND DURAFET)
Size D
Document Number 10021035
Rev B
Date: Thursday, March 12, 2015
Sheet 1 of 2




**CF2 POWER INPUTS:**
CF2-VBAT (PIN 13) SUPPLIED BY VSYS+
CF2-VBBK (PIN 14) SUPPLIED BY REG3V
CF2-VREG (PIN 9) SUPPLIED BY REG3.3V

**CF2 POWER OUTPUTS:**
CF2-VBAK (PIN 5) POWERS BOTH U7 AND U27 (NCP303)
CF2-VLIN (PIN 11) NOT USED

**POWER MONITOR RESET NOTES:**
If CF2-VREG (REG3.3V) is below 3.1V and CF2-VBBK (REG3V) is >= 2V, the MAX6367 will continue to hold the 68332 in reset.

If CF2-VREG (REG3.3V) is below 3.1V and CF2-VBBK (REG3V) is < 2V, the NCP303 (which actually monitors CF2-VBAK) will force the MSP430 into reset and stop the external crystal feed into the 68332. The NCP303 will continue to work and hold the MSP430 reset down to CF2-VBBK (REG3V) 0.7V and has 100ms of hysteresis.

**SHUTDOWN PIN NOTES:**
The FDV303N N-FET exists to prevent suspend in the case of missing or depleted CF2-VBBK. A fortunate side effect is that it also decreases the /SHDN level generated by the LT1521's internal 2-5uA 7V clamped pullup (the LTC1625 generates 2.5uA/4uA typ/max and the LT1529 generates 4.5uA/10uA typ/max) enough so that the MSP430's /PDFF input is well below the 3.6V maximum.

There is also a P-FET (not shown) controlled by the MSP430 that actively drives /SHDN high for 50us at the conclusion of a suspend to help kick start any capacitive loading from monitoring circuits.

**POWER SUPPLY SEQUENCING NOTES:**
POWER UP:
NCP303 MONITORS CF2-VBAK AND KEEPS /SHDN PULLED LOW UNTIL IT RISES ABOVE 2.0VDC. THE PROGRAMMABLE TIME DELAY SEQUENCES THE ACTIVATION OF CF2-VREG (REG3.3V) TO BE 2.2 SECS AFTER THE MSP430 HAS COME OUT OF RESET.

POWER DOWN:
NCP303 WILL PULL /SHDN LOW WHEN CF2-VBAK FALLS BELOW 2.0VDC. THE MSP430 WILL BE GOING INTO RESET AT THIS POINT AS WELL. THEREFORE, ANY POWER CYCLE THAT ALLOWS CF2-VBAK TO FALL BELOW 2.0VDC SHOULD RESULT IN A SUCCESSFUL REBOOT OF THE CF2.

**SYSTEM RECOVERY NOTES:**
TO FORCE THE CF2 INTO A KNOWN STATE FOLLOW THIS PROCEDURE:
1) UNPOWER THE CF2 FOR 5 SECS (TO ALLOW REG3V TO FALL BELOW 2.0VDC, WHICH WILL ENSURE A REBOOT).
2) ASSERT THE CTS LINE (RS232 HIGH AT J1.4)
3) POWER THE CF2 BACK UP.
4) THE CF2 SHOULD REBOOT INTO THE PERSISTENT BOOT MONITOR (PBM).
5) CONFIRM AND RELEASE CTS (/IRQ5).
6) FROM THE PBM PROMPT ENTER: "pico"
7) FROM THE PICODOS PROMPT ENTER: "ccc 1"
8) FROM THE PICODOS PROMPT ENTER: "app"

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Date: Saturday, March 28, 2015 Sheet 1 of 2