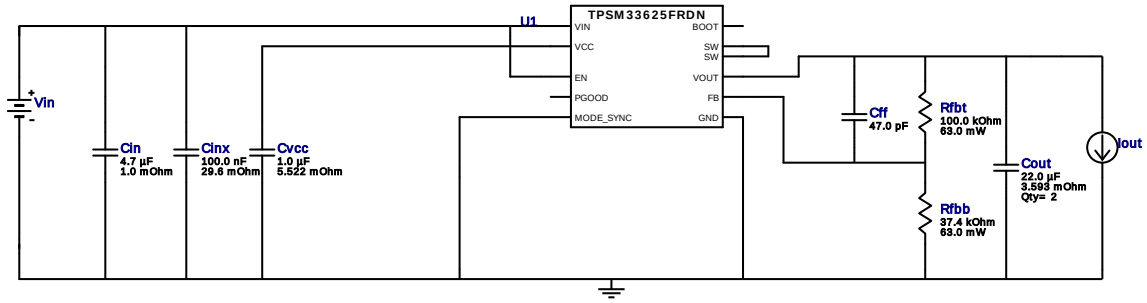
WEBENCH® Design Report

VinMin = 9.0V
VinMax = 36.0V
Vout = 3.6V
Iout = 1.0A

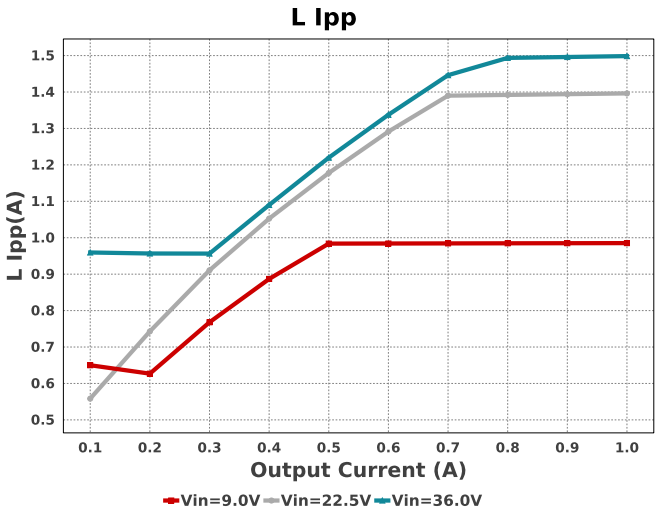
Device = TPSM33625FRDNR
Topology = Buck
Created = 2024-06-06 17:42:40.003
BOM Cost = $1.89
BOM Count = 9
Total Pd = 0.5W

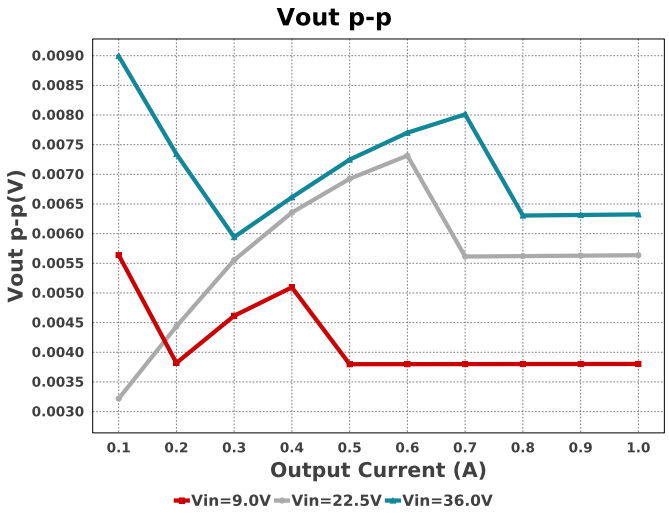
Design : 4 TPSM33625FRDNR
TPSM33625FRDNR 9V-36V to 3.60V @ 2A

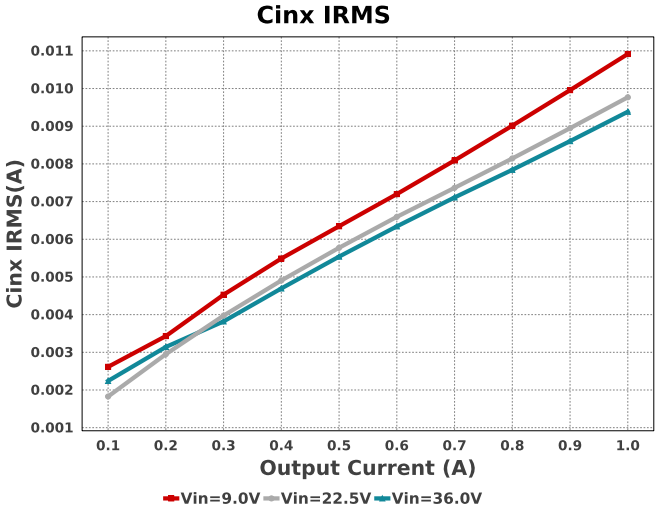


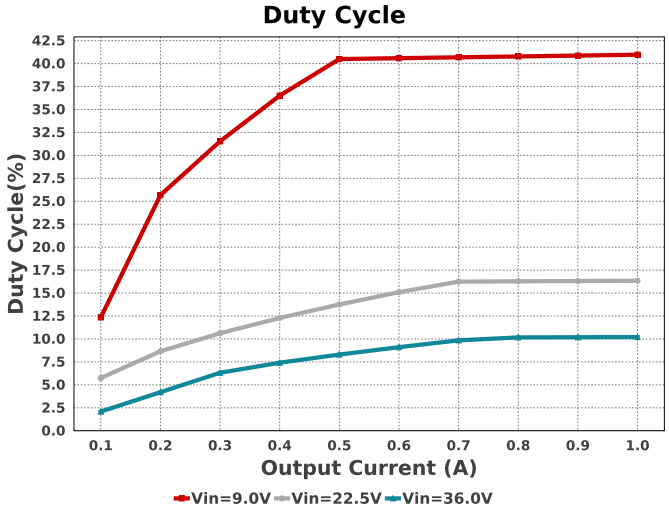
Electrical BOM

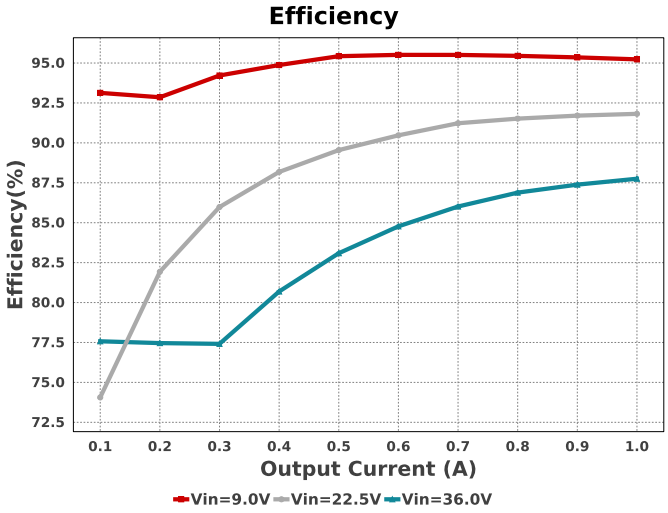
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cff	TDK	CGA1A2C0G1H470J030BA Series= C0G/NP0	Cap= 47.0 pF VDC= 50.0 V IRMS= 0.0 A	1	$0.01	0201 2 mm²
Cin	MuRata	GRM32ER71H475KA88L Series= X7R	Cap= 4.7 uF ESR= 1.0 mOhm VDC= 50.0 V IRMS= 6.0 A	1	$0.16	1210 15 mm²
Cinx	TDK	CGA3E2X7R1H104K080AA Series= X7R	Cap= 100.0 nF ESR= 29.6 mOhm VDC= 50.0 V IRMS= 971.99 mA	1	$0.01	0603 5 mm²
Cout	MuRata	GRM31CR71A226KE15L Series= X7R	Cap= 22.0 uF ESR= 3.593 mOhm VDC= 10.0 V IRMS= 3.5332 A	2	$0.12	1206_190 11 mm²
Cvcc	TDK	CGA3E1X7R1V105K080AC Series= X7R	Cap= 1.0 uF ESR= 5.522 mOhm VDC= 35.0 V IRMS= 2.2162 A	1	$0.05	0603 5 mm²
Rfbb	Vishay-Dale	CRCW040237K4FKED Series= CRCW..e3	Res= 37.4 kOhm Power= 63.0 mW Tolerance= 1.0%	1	$0.01	0402 3 mm²
Rfbt	Vishay-Dale	CRCW0402100KFKED Series= CRCW..e3	Res= 100.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	$0.01	0402 3 mm²
U1	Texas Instruments	TPSM33625FRDNR	Switcher	1	$1.40	RPE0009A 9 mm²

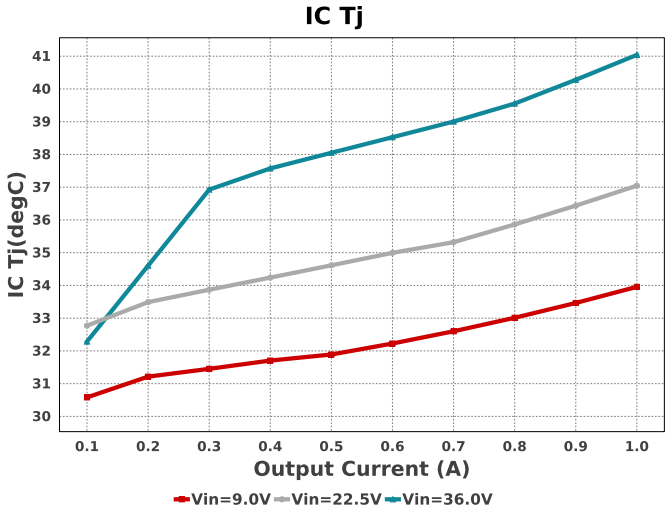


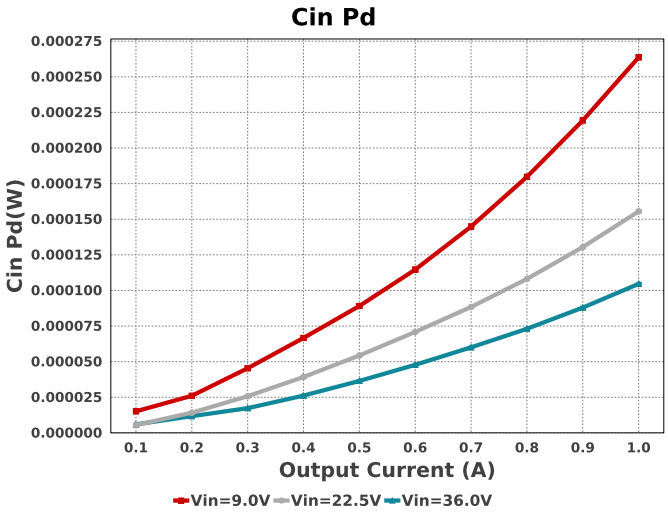


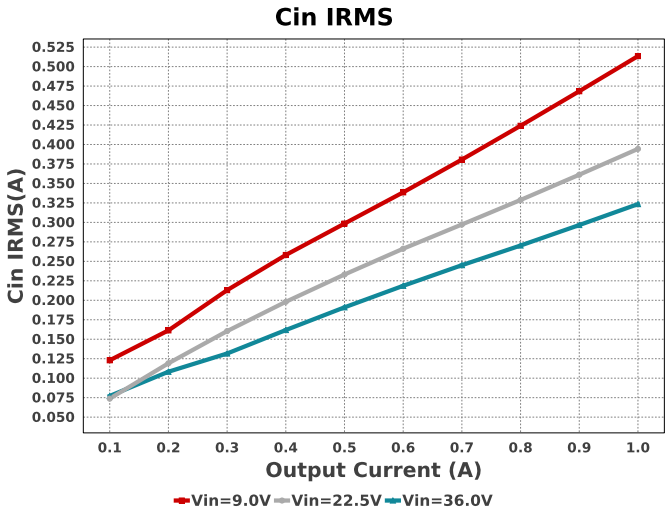


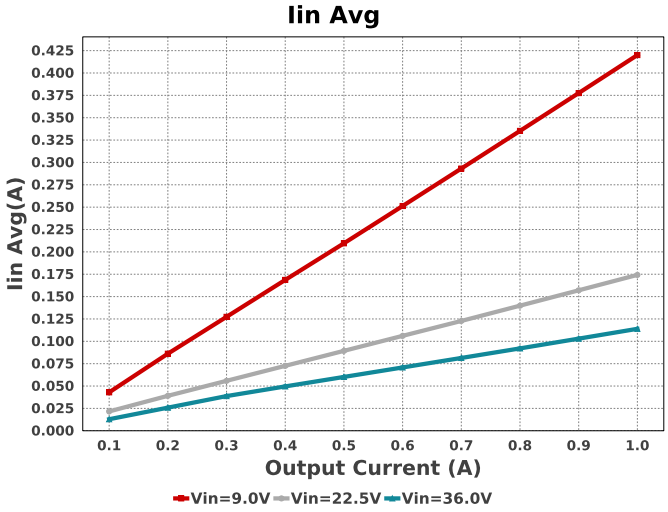


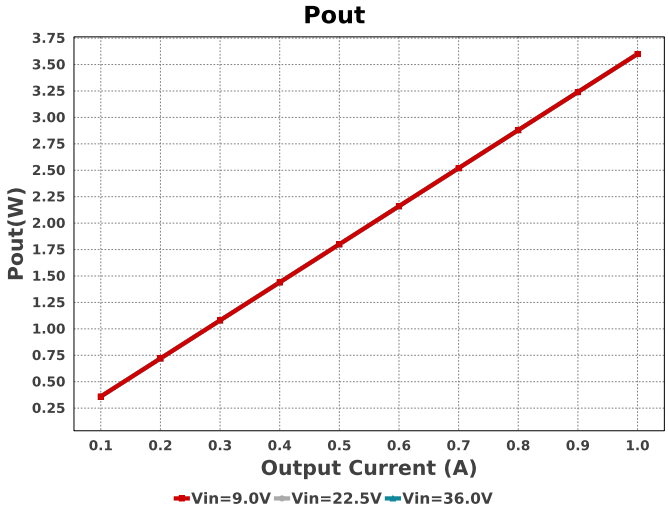


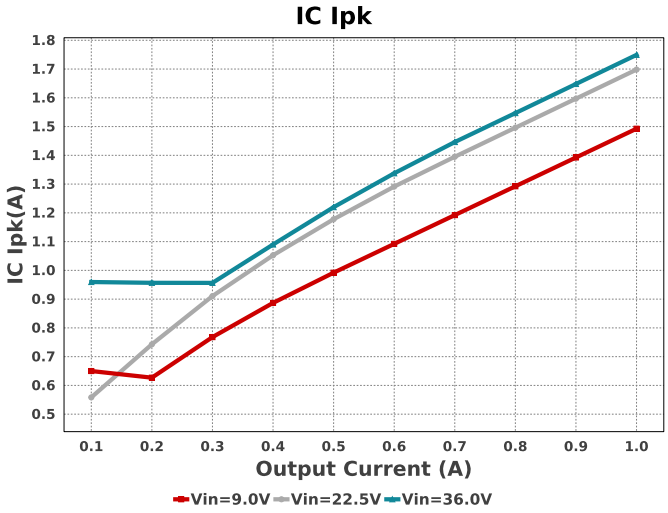


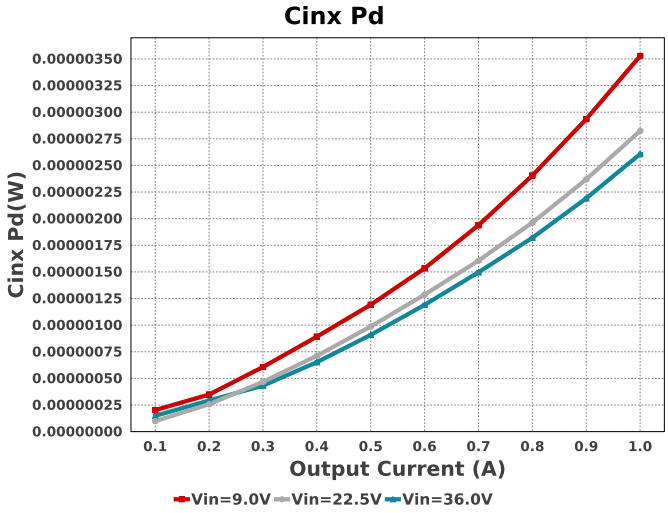


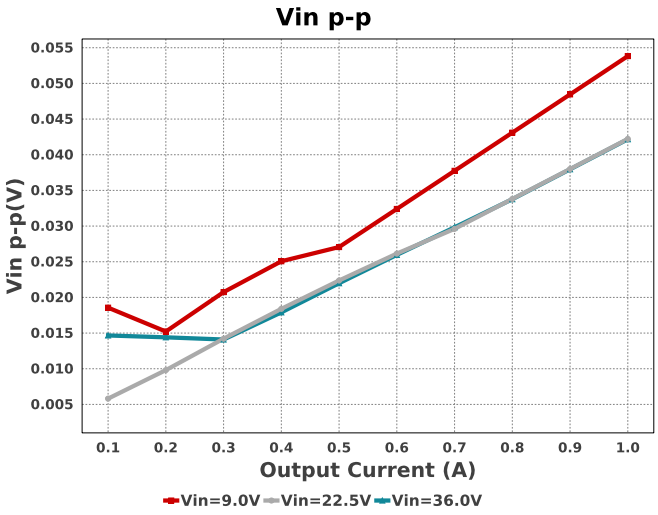


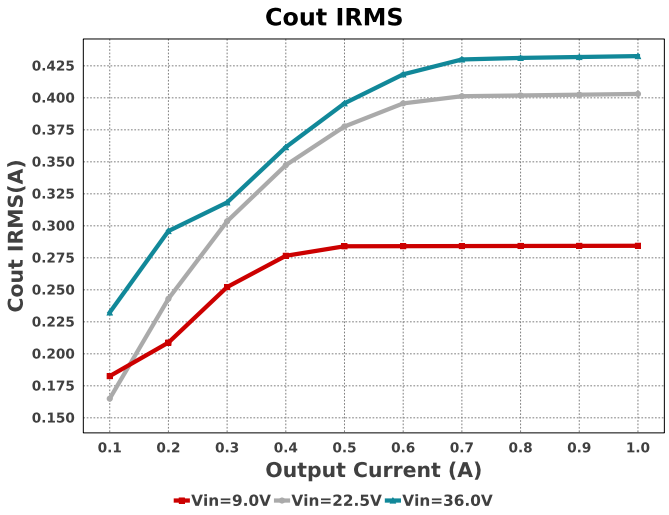


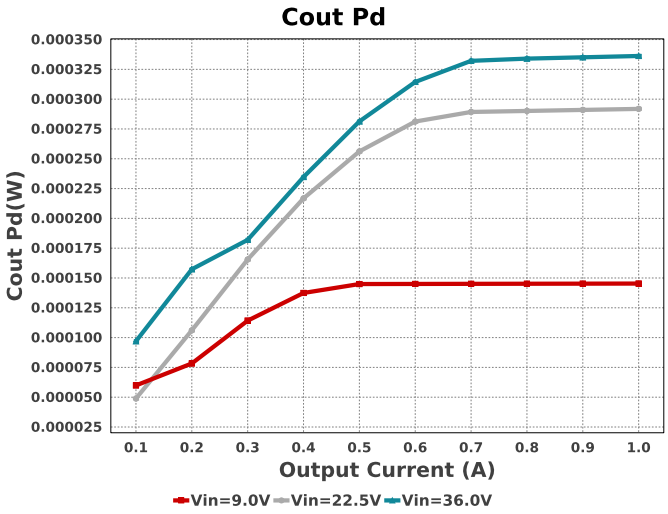


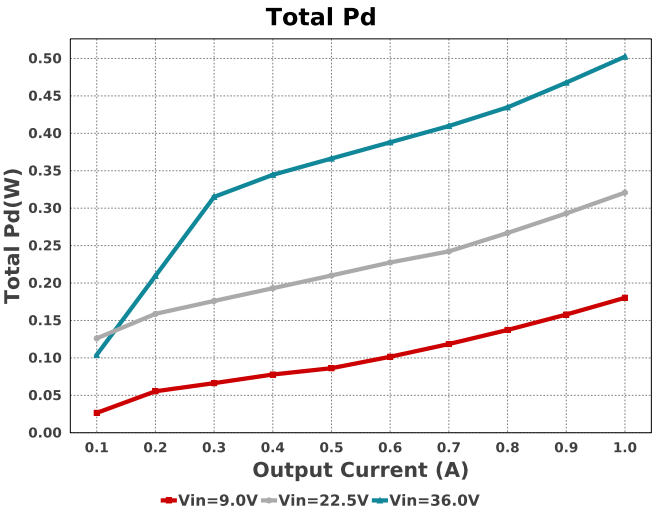


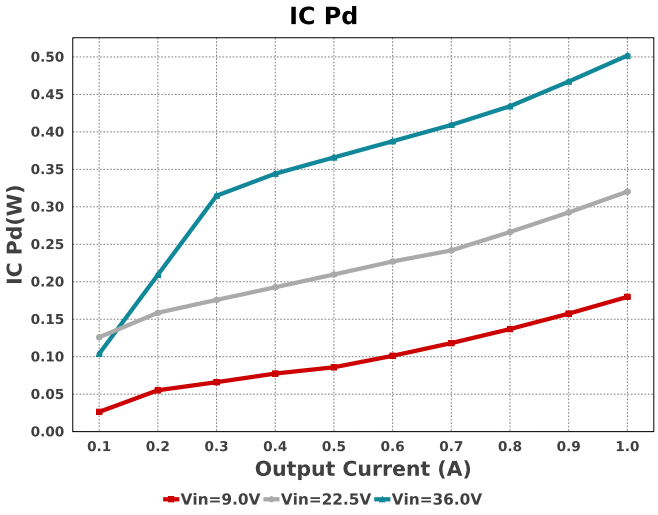


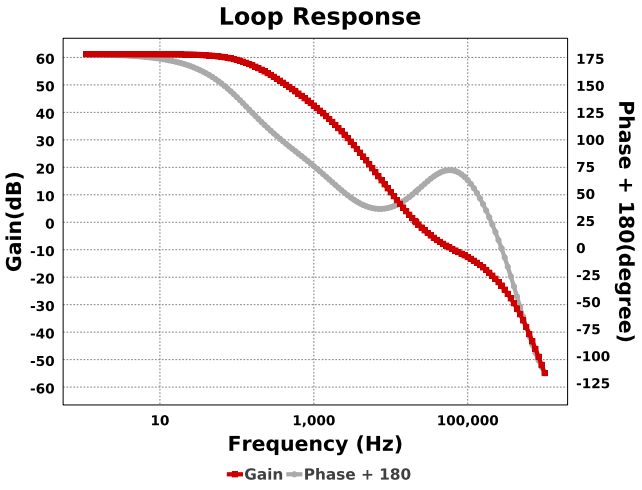


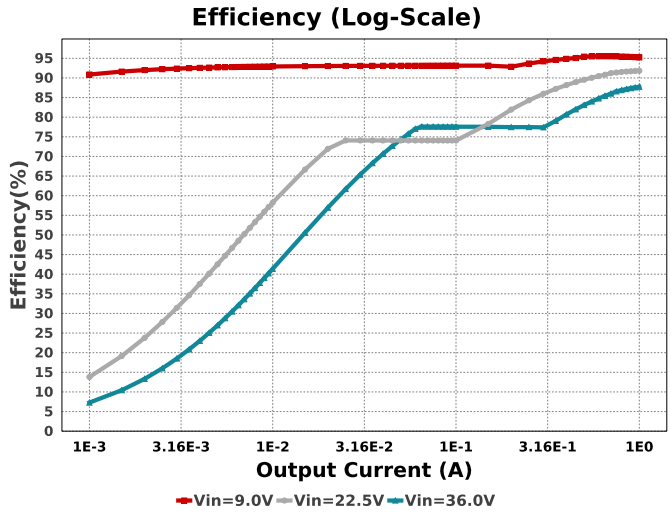












Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	323.457 mA	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	104.62 µW	Capacitor	Input capacitor power dissipation
3.	Cinx IRMS	9.384 mA	Capacitor	Bulk capacitor RMS ripple current
4.	Cinx Pd	2.607 µW	Capacitor	Bulk capacitor power dissipation
5.	Cout IRMS	432.605 mA	Capacitor	Output capacitor RMS ripple current
6.	Cout Pd	336.21 µW	Capacitor	Output capacitor power dissipation
7.	IC Ipk	1.749 A	IC	Peak switch current in IC
8.	IC Pd	501.85 mW	IC	IC power dissipation
9.	IC Tj	41.041 degC	IC	IC junction temperature
10.	IC Tolerance	12.5 mV	IC	IC Feedback Tolerance
11.	ICThetaJA Effective	22.0 degC/W	IC	Effective IC Junction-to-Ambient Thermal Resistance
12.	Iin Avg	113.96 mA	IC	Average input current
13.	Cin Pd	104.62 µW	Power	Input capacitor power dissipation
14.	Cinx Pd	2.607 µW	Power	Bulk capacitor power dissipation
15.	Cout Pd	336.21 µW	Power	Output capacitor power dissipation
16.	IC Pd	501.85 mW	Power	IC power dissipation
17.	Total Pd	502.399 mW	Power	Total Power Dissipation
18.	BOM Count	9	System Information	Total Design BOM count
19.	Cross Freq	21.431 kHz	System Information	Bode plot crossover frequency
20.	Duty Cycle	10.21 %	System Information	Duty cycle
21.	Efficiency	87.754 %	System Information	Steady state efficiency
22.	FootPrint	63.0 mm^2	System Information	Total Foot Print Area of BOM components
23.	Frequency	1000.0 kHz	System Information	Switching frequency
24.	Gain Marg	-23.082 dB	System Information	Bode Plot Gain Margin
25.	Iout	1.0 A	System Information	Iout operating point
26.	L Ipp	1.499 A	System Information	Peak-to-peak inductor ripple current
27.	Low Freq Gain	61.173 dB	System Information	Gain at 1Hz
28.	Mode	CCM	System Information	Conduction Mode
29.	Phase Marg	52.761 deg	System Information	Bode Plot Phase Margin
30.	Pout	3.6 W	System Information	Total output power
31.	Total BOM	$1.89	System Information	Total BOM Cost
32.	Vin	36.0 V	System Information	Vin operating point
33.	Vin p-p	42.169 mV	System Information	Peak-to-peak input voltage
34.	Vout	3.6 V	System Information	Operational Output Voltage

#	Name	Value	Category	Description
35.	Vout Actual	3.674 V	System Information	Vout Actual calculated based on selected voltage divider resistors
36.	Vout Tolerance	2.739 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
37.	Vout p-p	6.324 mV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	1.0	Maximum Output Current
VinMax	36.0	Maximum input voltage
VinMin	9.0	Minimum input voltage
Vout	3.6	Output Voltage
base_pn	TPSM33625F	Base Product Number
source	DC	Input Source Type
Ta	30.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

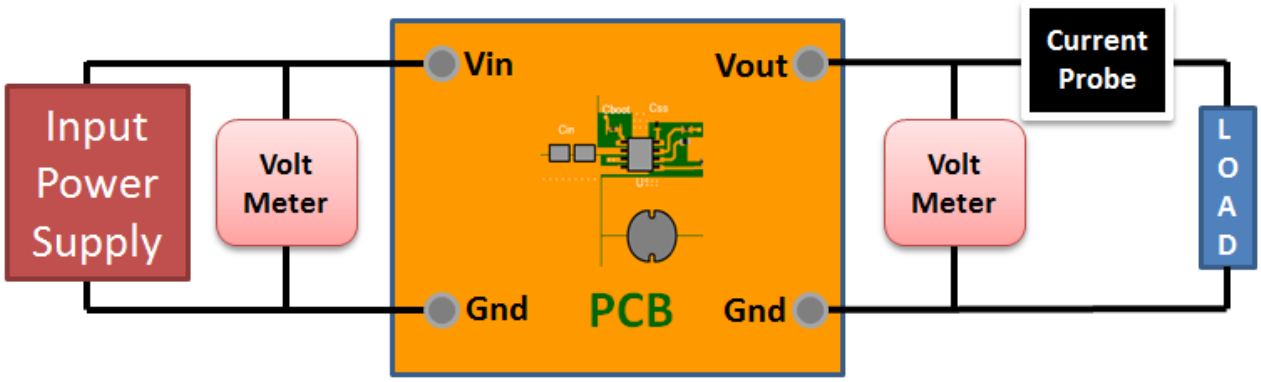
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 9.0V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum Iout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.



Design Assistance

1. Master key : E8A119AE42F0E3FD181D45ED1F5A0C7F[v1]
2. **TPSM33625F** Product Folder : http://www.ti.com/product/TPSM33625 : contains the data sheet and other resources.