Getting Started With Blackfin® Processors

Revision 4.0, November 2008

Part Number
82-000850-01

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ANALOG DEVICES

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SUPPORT OPTIONS

PREFACE

Thank you for your interest in the Blackfin® family of processors by Analog Devices, Inc

Purpose of This Manual

Getting Started With Blackfin Processors provides you with information about the design and evaluation process, Analog Devices tools, training, documentation, and other informational resources.

This manual provides an overview of a variety of documentation available in online form as well as a guide for evaluating Blackfin processors. This manual also describes the resources available to help you move your evaluation/design along quickly.

For engineers already using Blackfin processors in their designs, this guide provides resources and pointers to help transition your system to take advantage of the newest series of processors. For detailed descriptions of a processor's internal architectures, refer to the applicable processor's hardware reference manual. For detailed descriptions of processor software, refer to the *Blackfin Processor Programming Reference*. For a complete list of documents that support Blackfin processors, refer to "Support Options" on page 3-1.

Intended Audience

The primary audience for this guide is comprised of system designers, programmers, and hardware engineers who want to learn whether a specific Blackfin processor matches their design requirements for new applications.

Manual Contents

This manual consists of:

- Chapter 1, "Introduction"
  This chapter briefly describes the processor architecture, available models, and processor features.
- Chapter 2, "The Evaluation Process"
  This chapter focuses on available software and hardware tools.
- Chapter 3, "Support Options"
  This chapter describes support (documentation, training, and more) available during the evaluation and development processes.

What's New in This Manual

Revision 4.0 of *Getting Started With Blackfin Processors* provides information about new Blackfin processors, EZ-Extenders®, EZ-Boards, and EZ-KIT Lite® packages. It also updates URLs.

Technical or Customer Support

You can reach Analog Devices, Inc. Customer Support in the following ways:

- Visit the Embedded Processing and DSP products Web site at
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- E-mail tools questions to
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- E-mail processor questions to
  processor.support@analog.com (World wide support)
  processor.europe@analog.com (Europe support)
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  USA

Product Information

Product information can be obtained from the Analog Devices Web site, VisualDSP++® online Help system, and a technical library CD.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor series, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

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VisualDSP++ Online Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, Dinkum Abridged C++ library, and FLEXnet License Tools software documentation. You can search easily across the entire VisualDSP++ documentation set for any topic of interest.

For easy printing, supplementary Portable Documentation Format (`.pdf`) files for all manuals are provided on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

File	Description
`.chm`	Help system files and manuals in Microsoft help format
`.htm` or `.html`	Dinkum Abridged C++ library and FLEXnet License Tools software documentation. Viewing and printing the `.html` files requires a browser, such as Internet Explorer 6.0 (or higher).
`.pdf`	VisualDSP++ and processor manuals in PDF format. Viewing and printing the `.pdf` files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

Technical Library CD

The technical library CD contains seminar materials, product highlights, a selection guide, and documentation files of processor manuals, VisualDSP++ software manuals, and hardware tools manuals for the following processor families: Blackfin, SHARC®, TigerSHARC®, ADSP-218x, and ADSP-219x.

To order the technical library CD, go to `http://www.analog.com/processors/technical_library`, navigate to the manuals page for your processor, click the request CD check mark, and fill out the order form.

Data sheets, which can be downloaded from the Analog Devices Web site, change rapidly, and therefore are not included on the technical library CD. Technical manuals change periodically. Check the Web site for the latest manual revisions and associated documentation errata.

1 INTRODUCTION

This chapter briefly describes the Blackfin processor's architecture and key features and compares available models.

Topics include:

What are Blackfin Processors?

Blackfin processors from Analog Devices embody a new breed of 16/32-bit embedded processor with the industry's highest performance and power efficiency for applications where a convergence of capabilities—multi-format audio, video, voice and image processing; multi-mode baseband and packet processing; and real-time security and control processing—are critical.

Blackfin processors deliver breakthrough signal processing performance and power efficiency with a RISC programming model. Blackfin processors present high-performance, homogeneous software targets, which allow flexible resource allocation between hard real-time processor tasks and non real-time control tasks. System control tasks can often run in the shadow of processor and video tasks.

Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply/accumulate (MAC) digital signal processing functionality, and

8-bit video processing performance that had previously been the exclusive domain of very long instruction word (VLIW) media processors.

Blackfin processors include advanced memory management that supports memory-protected and non memory-protected embedded operating systems such as µClinux™, ThreadX® (Express Logic), INTEGRITY®, velOSity™, µ-velOSity™ (Green Hills Software), Nucleus® (Mentor Graphics), Fusion™ (Unicoi Systems), RTXC Quadros™ (Quadros Systems), and µC/OS-II (Micrium), to name a few.

Combining RISC MCU and Signal Processor Functionality

Blackfin processors provide microcontroller (MCU) and signal processing functionality in a unified architecture, allowing flexible partitioning between the needs of control and signal processing. If the application demands, the Blackfin processor can act as 100% MCU (with code density on par with industry standards), 100% signal processor (with clock rates at the leading edge of signal processor technology), or a combination of the two.

The Blackfin family of processors from Analog Devices integrates a 32-bit RISC instruction set with an 8-bit video instruction set with dual 16-bit MAC units. The processor's variable-length instruction set extends up to 64-bit opcodes used in processor inner loops (one single instruction, multiple data [SIMD] and two load/store/cycle), but is optimized so that 16-bit opcodes represent the most frequently used instructions. As a result, compiled code density figures are competitive with industry-leading MCUs, yet its interlocked pipeline and algebraic instruction syntax facilitate development in both C/C++ and assembly.

Figure 1-1 shows a block diagram of a single-core ADSP-BF549 Blackfin 16/32-bit processor.

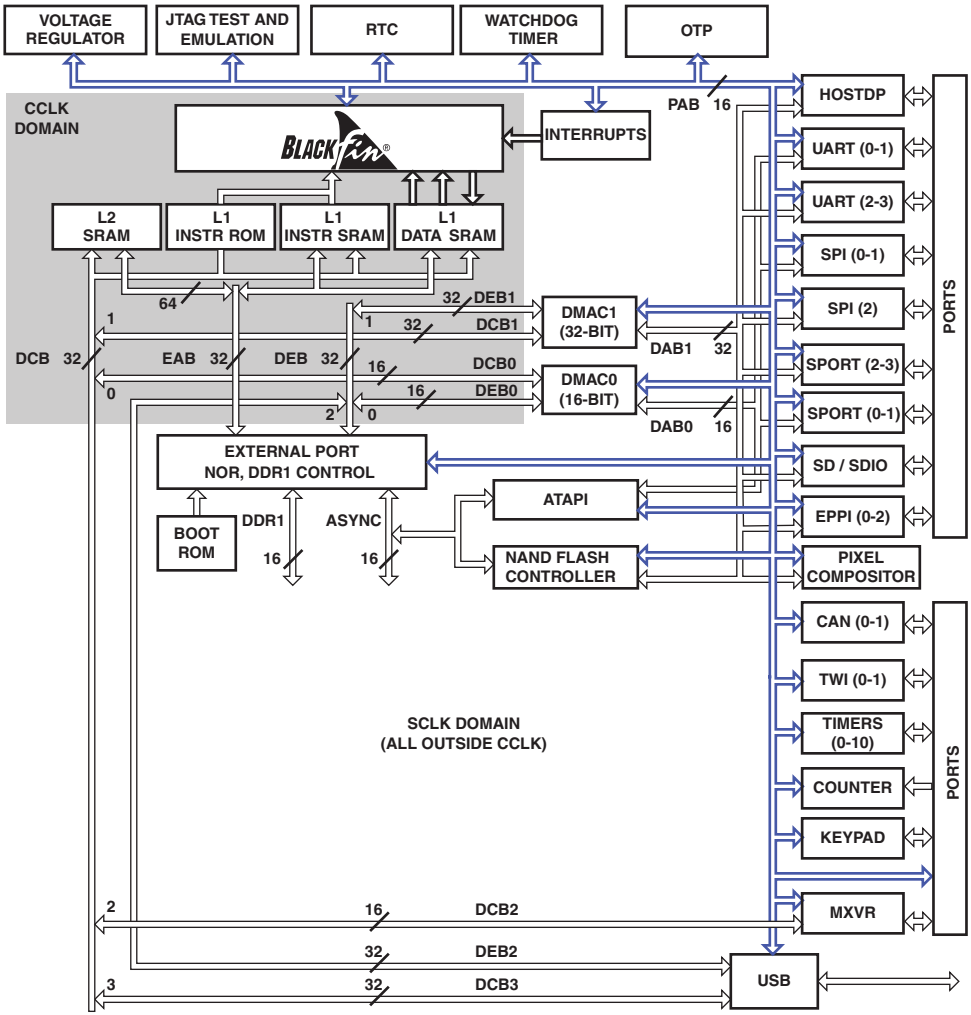


Figure 1-1. Single-Core ADSP-BF549 Blackfin 16/32-Bit Processor

Blackfin processors support both protected and unprotected operating modes that prevent users from accessing or affecting shared parts of the system. In addition, the processors provide memory management

capabilities that enable users to define separate application development spaces. This design feature prevents distinct code sections from being overwritten. At the same time, the Blackfin processor's architecture allows asynchronous interrupts and synchronous exceptions, as well as programmable interrupt priorities. Thus, Blackfin processors are well suited as targets for embedded operating systems.

Approaches to Application Development

Blackfin processors have a peripheral set that supports high-speed serial and parallel data movement. In addition, Blackfin processors include an advanced power management feature set that allows system architects to craft designs with low dynamic power profiles.

In today's design model, MCU (microcomputer unit) and traditional processor programmers often partition their code development into two separate groups, interacting only at the system boundary level where their two functional worlds meet. This makes some sense, as two separate groups of designers can develop their own sets of design practices based on application requirements. For instance, signal processing developers may want to implement techniques to improve performance. Another group may have opposing design goals; MCU programmers, for example, may prefer implementing a turnkey system and letting it perform all tasks without user intervention.

With this in mind, Blackfin processors were designed to support both DMA and cache memory controllers to move data through a system. Multiple high-speed DMA channels shuttle data between peripherals and memory systems, allowing the fine-tuning controls sought by processor programmers without using up valuable core processor cycles. Conversely, on-chip configurable instruction and data caches allow a hands-off approach to managing code and data in a manner very familiar to MCU programmers. Often, at the system integration level, a combination of both approaches is ideal.

Another reason for the historical separation of MCU and processor development groups is that the two processors have two separate sets of design imperatives. From a technical standpoint, engineers responsible for architecting a system often hesitate to mix a "control" application with a "signal processing" application on the same processor. Their most common fear is that non real-time tasks interfere with real-time tasks. For instance, programmers who handle tasks such as the graphical user interface (GUI) or the networking stack should not have to worry about hampering the system's "real-time" signal processing activities. Of course, the definition of real time varies based on the specific application. In an embedded application, the focus is on the time required to service an interrupt. For this purpose, assume there is a time frame of less than 1 microsecond between an interrupt and the time that the system context is saved at the start of the service routine.

With the introduction of the Blackfin processors, a C/C++-centric unified code base can be realized. This enables developers to leverage enormous amounts of existing application code developed from previous efforts. Because Blackfin processors are optimized for both control and signal processing operations, compilers can generate code that is both tight (from a code density standpoint) and efficient (for computationally-intensive signal processing applications). Of course for veteran programmers, targeted assembly coding is still an option for optimizing critical processing loops.

Operating system (OS) support is also key. Several layers of tasking can be realized by supporting an operating system or real-time kernel. An interrupt controller that supports multiple priority levels is needed to ensure that targeted performance is still achievable. Context switching must be attainable through hardware-based stack and frame pointer support. This enables developers to create systems that include both worlds—control and real-time signal processing—on the same device.

In addition, the Blackfin processor's memory protection facility permits OS support for memory protection. This allows one task, via a paging mechanism, to block memory or instruction accesses by another task.

An exception is generated whenever unauthorized access is made to a protected area of memory. The kernel services this exception and takes appropriate action.

The high processing speeds achieved by Blackfin processors translate into several tangible benefits. The first is time to market. There can be considerable savings in reducing or bypassing the code optimization effort when there is plenty of processing capacity to spare. A second benefit is reduced software maintenance, which can otherwise dominate a product's life cycle cost. Finally, for scalable Blackfin architectures, designers can base their work around the most capable member of the Blackfin processor family, and can use a cost-optimized processor.

Dual-Core Processors Add Flexibility

Blackfin processors are also available as dual-core devices. The traditional use of a dual-core processor employs discrete and often different tasks that run on each of the cores. For example, one core might perform all of the control-related tasks, such as graphics and overlay functionality, networking, interfacing to bulk storage, and overall flow control. This core is also where the operating system or kernel most likely resides. Meanwhile, the second core is dedicated to the application's high-intensity processing functions. For example, compressed data packets might be transferred over a network interface to the first core for preprocessing, and then passed to the second core for audio and video decoding. Figure 1-2 shows a block diagram of a typical dual-core processor.

The use of a dual-core processor is preferred for designs built by separate software development teams. The ability to segment these types of functions allows a parallel design process, eliminating critical path dependencies in the project. This programming model also aids the testing and validation phases of the project. For example, a code change on one core does not necessarily invalidate the testing efforts already completed on the other core.

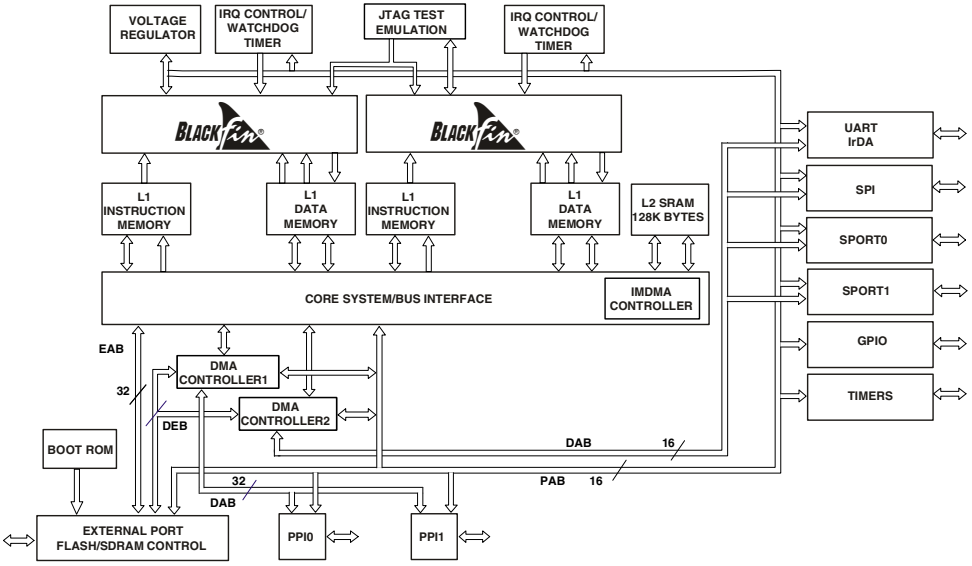


Figure 1-2. Functional Block Diagram

The Blackfin Family of Processors

New high-performance Blackfin processors are available now, while plans for additional Blackfin processors are designed to offer feature-packed, future-ready architectures for media-rich applications.

Blackfin Processors (Currently Available)

The ADSP-BF535 was the first released Blackfin processor, followed in March 2003 by three pin-compatible devices, the ADSP-BF531, ADSP-BF532, and ADSP-BF533 Blackfin processors. These three devices offer a range of memory and speed options, providing maximum scalability and design flexibility with standard serial interfaces such as SPI, UART, and a flexible programmable serial ports (SPORTs). The devices also offer 16-bit parallel peripheral interfaces (PPI) to connect gluelessly to high-speed converters and imaging components.

In January of 2005, Analog Devices introduced three Blackfin processors with embedded connectivity: the ADSP-BF536, ADSP-BF537, and ADSP-BF534. These three devices are also pin-compatible with each other and include a controller area network (CAN) and a two-wire interface (TWI), and on some models, a 10/100 ethernet MAC.

In May of 2006, Analog Devices introduced the ADSP-BF538 processors, which added the complement of on-board flash memory and also more instances of the communications peripherals for enhanced connectivity.

In November of 2006, Analog Devices introduced five new processors: ADSP-BF542, ADSP-BF544, ADSP-BF547, ADSP-BF548, and ADSP-BF549. These ADSP-BF54x processors focus on higher system performance for convergent applications through increased (2x) I/O bandwidth, increased on-chip memory, and a rich peripherals set including high-speed USB, ATAPI, NAND flash, DDR1, and LockBox™ secure technology. The PPI was also enhanced to support more high-speed parallel devices; up to three PPIs are available on some models.

In March of 2007, Analog Devices introduced ADSP-BF52x processors, which focus on the next generation of mobile devices. The ADSP-BF52x series is pin-compatible and is comprised of the ADSP-BF522, ADSP-BF523, ADSP-BF524, ADSP-BF525, ADSP-BF526, and ADSP-BF527 processors. This series concentrates on connectivity, including combinations of high-speed USB, 10/100 ethernet, NAND flash controller, an audio codec, and so on. The ADSP-BF52x processors offer lower dynamic and static power consumption over previous Blackfin processors.

In November of 2008, Analog Devices introduced the ADSP-BF51x processors. The ADSP-BF512/ADSP-BF514/ADSP-BF516/ADSP-BF518 processors extend the Blackfin family further into the industrial and instrumentation market with the availability of an on chip eMAC which supports 1588 version 2, a 3-phase PWM generation unit and a quadrature encoder.

All Blackfin processors mentioned above are single-core processors.

Analog Devices also developed a dual-core symmetric multiprocessor, the ADSP-BF561. This processor uses a dual-core processor and increases performance without switching processor architectures. In fact, by running both processor cores at lower frequencies and lower voltages, power consumption is lowered. The advantages of this technique are described in "Dual-Core Processors Add Flexibility" on page 1-6. In addition, the ADSP-BF561 offers a second PPI, making video in/out possible simultaneously.

Each Blackfin processor provides unique capabilities, while being pin-compatible with other Blackfin devices. Table 1-1 lists key Blackfin processor specifications.

All processors noted as "RoHS Compliant" are also lead free.

Also, unless they differ from processor to processor, the key peripherals are listed in the row designating the Blackfin series in bold typeface (such as **ADSP-BF522**).

The list of supported Blackfin processors is subject to change. For a complete and up-to-date listing of Blackfin processors, refer to:
http://www.analog.com/blackfin

Table 1-1. Summary of Blackfin Processor Specifications

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF51x					SPORT, SPI, PPI, GPIO, PWM, Rotary, LockBox
ADSP-BF512KBCZ-4	168-Ball CSP_BGA BC-168-1	400	0°C to +70°C	✓	
ADSP-BF512KSWZ-4	176-Lead LQFP_ED SQ-176-2	400	0°C to +70°C	✓	
ADSP-BF512BSWZ-4	176-Lead LQFP_ED SQ-176-2	400	–40°C to +85°	✓	
ADSP-BF514KBCZ-4	168-Ball CSP_BGA BC-168-1	400	0°C to +70°C	✓	RSI
ADSP-BF514KSWZ-4	176-Lead LQFP_ED SQ-176-2	400	0°C to +70°C	✓	RSI
ADSP-BF514BSWZ-4	176-Lead LQFP_ED SQ-176-2	400	–40°C to +8°C	✓	RSI

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF516KBCZ-4	168-Ball CSP_BGA BC-168-1	400	0°C to +70°C	✓	eMAC, RSI
ADSP-BF516KSWZ-4	176-Lead LQFP_ED SQ-176-2	400	0°C to +70°C	✓	eMAC, RSI
ADSP-BF516BSWZ-4	176-Lead LQFP_ED SQ-176-2	400	–40°C to +85°	✓	eMAC, RSI
ADSP-BF518KBCZ-4	168-Ball CSP_BGA BC-168-1	400	0°C to +70°C	✓	eMAC, IEEE1588, RSI
ADSP-BF518BSWZ-4	176-Lead LQFP_ED SQ-176-2	400	–40°C to +85°	✓	eMAC, IEEE1588, RSI
ADSP-BF512KBCZ-3	168-Ball CSP_BGA BC-168-1	300	0°C to +70°C	✓	
ADSP-BF512KSWZ-3	176-Lead LQFP_ED SQ-176-2	300	0°C to +70°C	✓	
ADSP-BF512BSWZ-3	176-Lead LQFP_ED SQ-176-2	300	–40°C to +85°	✓	
ADSP-BF514KBCZ-3	168-Ball CSP_BGA BC-168-1	300	0°C to +70°C	✓	RSI

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF514KSWZ-3	176-Lead LQFP_ED SQ-176-2	300	0°C to +70°C	✓	RSI
ADSP-BF514BSWZ-3	176-Lead LQFP_ED SQ-176-2	300	–40°C to +85°	✓	RSI
ADSP-BF516KBCZ-3	168-Ball CSP_BGA BC-168-1	300	0°C to +70°C	✓	eMAC, RSI
ADSP-BF516KSWZ-3	176-Lead LQFP_ED SQ-176-2	300	0°C to +70°C	✓	eMAC, RSI
ADSP-BF516BSWZ-3	176-Lead LQFP_ED SQ-176-2	300	–40°C to +8°C	✓	eMAC, RSI
ADSP-BF512KBCZ-4F	168-Ball CSP_BGA BC-168-1	400	0°C to +70°C	✓	Flash
ADSP-BF512KSWZ-4F4	176-Lead LQFP_ED SQ-176-2	400	0°C to +70°C	✓	Flash
ADSP-BF512BSWZ-4F4	176-Lead LQFP_ED SQ-176-2	400	–40°C to +8°C	✓	Flash
ADSP-BF514KBCZ-4F4	168-Ball CSP_BGA BC-168-1	400	0°C to +70°C	✓	RSI, Flash

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF514KSWZ-4F4	176-Lead LQFP_ED SQ-176-2	400	0°C to +70°C	✓	RSI, Flash
ADSP-BF514BSWZ-4F4	176-Lead LQFP_ED SQ-176-2	400	–40°C to +85°C	✓	RSI, Flash
ADSP-BF516KBCZ-4F4	168-Ball CSP_BGA BC-168-1	400	0°C to +70°C	✓	eMAC, RSI, Flash
ADSP-BF516KSWZ-4F4	176-Lead LQFP_ED SQ-176-2	400	0°C to +70°C	✓	eMAC, RSI, Flash
ADSP-BF516BSWZ-4F4	176-Lead LQFP_ED SQ-176-2	400	–40°C to +85°C	✓	eMAC, RSI, Flash
ADSP-BF518KBCZ-4F4	168-Ball CSP_BGA BC-168-1	400	0°C to +70°C	✓	IEEE1588, eMAC, RSI, Flash
ADSP-BF518BSWZ-4F4	176-Lead LQFP_ED SQ-176-2	400	–40°C to +8°C	✓	IEEE1588, eMAC, RSI, Flash

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF522					1 TWI, 1 SPI, 2 UARTs, 8 timers, PPI, host port, NAND flash controller
ADSP-BF522BBCZ-3A	208-CSP_BGA	300	-40°C to +85°C	✓	
ADSP-BF522BBCZ-4A	208-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF522KBCZ-3	289-CSP_BGA	300	0°C to +70°C	✓	
ADSP-BF522KBCZ-3C2	289-CSP_BGA	400	0°C to +70°C	✓	
ADSP-BF522KBCZ-4	289-CSP_BGA	400	0°C to +70°C	✓	
ADSP-BF522KBCZ-4C2	289-CSP_BGA	400	0°C to +70°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF523					HS USB OTG, 1 TWI, 1 SPI, 2 UARTs, 8 timers, PPI, host port, NAND flash controller
ADSP-BF523BBCZ-5A	208-CSP_BGA	533	-40°C to +85°C	✓	
ADSP-BF523KBCZ-5	289-CSP_BGA	533	0°C to +70°C	✓	
ADSP-BF523KBCZ-5C2	289-CSP_BGA	533	0°C to +70°C	✓	
ADSP-BF523KBCZ-6	289-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF523KBCZ-6A	208-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF523KBCZ-6C2	289-CSP_BGA	600	0°C to +70°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF524					HS USB OTG, 1 TWI, 2 SPIs, 2 UARTs, 8 timers, PPI, host port, NAND flash controller
ADSP-BF524BBCZ-3A	208-CSP_BGA	300	-40°C to +85°C	✓	
ADSP-BF524BBCZ-4A	208-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF524KBCZ-3	289-CSP_BGA	300	0°C to +70°C	✓	
ADSP-BF524KBCZ-3C2	289-CSP_BGA	300	0°C to +70°C	✓	
ADSP-BF524KBCZ-4	289-CSP_BGA	400	0°C to +70°C	✓	
ADSP-BF524KBCZ-4C2	289-CSP_BGA	400	0°C to +70°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF525					HS USB OTG, 1 TWI, 1 SPI, 2 UARTs, 8 timers, PPI, host port, NAND flash controller
ADSP-BF525BBCZ-5A	208-CSP_BGA	533	-40°C to +85°C	✓	
ADSP-BF525KBCZ-5	289-CSP_BGA	533	0°C to +70°C	✓	
ADSP-BF525KBCZ-5C2	289-CSP_BGA	533	0°C to +70°C	✓	
ADSP-BF525KBCZ-6	289-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF525KBCZ-6A	208-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF525KBCZ-6C2	289-CSP_BGA	600	0°C to +70°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF526					Ethernet MAC, HS USB OTG, 1 TWI, 1 SPI, 2 UARTs, 8 timers, PPI, host port, NAND flash controller
ADSP-BF526BBCZ-3A	208-CSP_BGA	300	-40°C to +85°C	✓	
ADSP-BF526BBCZ-4A	208-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF526KBCZ-3	289-CSP_BGA	400	0°C to +70°C	✓	
ADSP-BF526KBCZ-3C2	289-CSP_BGA	300	0°C to +70°C	✓	
ADSP-BF526KBCZ-4	289-CSP_BGA	300	0°C to +70°C	✓	
ADSP-BF526KBCZ-4C2	289-CSP_BGA	400	0°C to +70°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF527					Ethernet MAC, HS USB OTG, 1 TWI, 1 SPI, 3 UARTs, 8 timers, PPI, host port, NAND flash controller
ADSP-BF527BBCZ-5A	208-CSP_BGA	533	-40°C to +85°C	✓	
ADSP-BF527KBCZ-5	289-CSP_BGA	533	0°C to +70°C	✓	
ADSP-BF527KBCZ-5C2	289-CSP_BGA	533	0°C to +70°C	✓	
ADSP-BF527KBCZ-6	289-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF527KBCZ-6A	208-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF527KBCZ-6C2	289-CSP_BGA	600	0°C to +70°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF542					Pixel Compositor, HS USB OTG, 1 TWI, 2 SPIs, 3 UARTs, CAN, 8 timers, 2 PPIs, SD/SDIO controller, NAND flash controller, ATAPI
ADSP-BF542BBCZ-4A	400-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF542BBCZ-5A	400-CSP_BGA	533	-40°C to +85°C	✓	
ADSP-BF542KBCZ-6A	400-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF544					Pixel Compositor, 2 TWIs, 2 SPIs, 3 UARTs, 2 CANs, 11 timers, multiple PPIs, 18/24-bit LCD, NAND flash controller
ADSP-BF544BBCZ-4A	400-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF544BBCZ-5A	400-CSP_BGA	533	-40°C to +85°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF547					Pixel Compositor, HS USB OTG, 2 TWIs, 3 SPIs, 4 UARTs, 11 timers, 18/24-bit LCD, multiple PPIs, ATAPI, NAND flash controller
ADSP-BF547BBCZ-5A	400-CSP_BGA	533	-40°C to +85°C	✓	
ADSP-BF547KBCZ-6A	400-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF548					Pixel Compositor, HS USB OTG, 2 TWIs, 3 SPIs, 4 UARTs, 2 CANs, 11 timers, 18/24-bit LCD, multiple PPIs, ATAPI, NAND flash controller
ADSP-BF548BBCZ-5A	400-CSP_BGA	533	-40°C to +85°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF549					
ADBF549MWBBCZ	400 ball CSP_BGA	533	-40°C to +85°C	✓	External 1.8V mobile DDR controller
ADBF549WBBCZ-5xx	400-CSP_BGA	533	-40°C to +85°C	✓	Automotive use only. MXVR, 2 CANs, Pixel Compositor, HS USB OTG, 2 TWIs, 3 SPIs, 4 UARTs, 11 timers, 18/24-bit LCD, multiple PPIs, ATAPI, NAND flash controller
ADBF549MWBBCZ-5M	400 ball CSP_BGA	533	-40°C to +85°C	✓	External 1.8V mobile DDR controller
ADSP-BF538					CAN, 54 GPIOs, 4 SPORTs, 3 UARTs, 3 SPIs, 2 TWIs, PPI
ADSP-BF538BBCZ-4A	316-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF538BBCZ-4F4	316-CSP_BGA	400	-40°C to +85°C	✓	512K flash
ADSP-BF538BBCZ-4F8	316-CSP_BGA	400	-40°C to +85°C	✓	1M flash

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF538BBCZ-5A	316-CSP_BGA	533	-40°C to +85°C	✓	
ADSP-BF538BBCZ-5F4	316-CSP_BGA	533	-40°C to +85°C	✓	512K flash
ADSP-BF538BBCZ-5F8	316-CSP_BGA	533	-40°C to +85°C	✓	1M flash
ADSP-BF538BBCZ-4F8	316-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF531					PPI, UART, SPI, 2 SPORTs, 3 timers
ADSP-BF531SBBC400	160-CSP_BGA	400	-40°C to +85°C		
ADSP-BF531SBBCZ400	160-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF531SBSTZ400	176-LQFP	400	-40°C to +85°C	✓	
ADSP-BF531SBB400	169-PBGA	400	-40°C to +85°C		
ADSP-BF531SBBZ400	169-PBGA	400	-40°C to +85°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF532					PPI, UART, SPI, 2 SPORTs, 3 timers
ADSP-BF532SBBC400	160-CSP_BGA	400	-40°C to +85°C		
ADSP-BF532SBBCZ400	160-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF532SBSTZ400	176-LQFP	400	-40°C to +85°C	✓	
ADSP-BF532SBB400	169-PBGA	400	-40°C to +85°C		
ADSP-BF532SBBZ400	169-PBGA	400	-40°C to +85°C	✓	
ADSP-BF533					PPI, UART, SPI, 2 SPORTs, 3 timers
ADSP-BF533SBBZ400	169-PBGA	400	-40°C to +85°C		
ADSP-BF533SBSTZ400	176-PBGA	400	-40°C to +85°C		
ADSP-BF533SBBCZ400	160-CSP_BGA	400	-40°C to +85°C		
ADSP-BF533SBBC500	160-CSP_BGA	500	-40°C to +85°C		
ADSP-BF533SBBCZ500	160-CSP_BGA	500	-40°C to +85°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF533SBB500	169-PBGA	500	-40°C to +85°C		
ADSP-BF533SBBZ500	169-PBGA	500	-40°C to +85°C	✓	
ADSP-BF533SBBC-5V	160-CSP_BGA	533	-40°C to +85°C		
ADSP-BF533SBBCZ-5V	160-CSP_BGA	533	-40°C to +85°C	✓	
ADSP-BF533SKBC-6V	160-CSP_BGA	600	0°C to +70°C		
ADSP-BF533SKBCZ-6V	160-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF534					CAN, PPI, TWI, 2 UARTs, timers, 1 SBI
ADSP-BF534BBC-4A	182-CSP_BGA	400	-40°C to +85°C		
ADSP-BF534BBCZ-4A	182-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF534BBCZ-4B	208 Sparse MiniBGA	400	-40°C to +85°C	✓	
ADSP-BF534BBC-5A	182-CSP_BGA	500	-40°C to +85°C		

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF534BBCZ-5A	182-CSP_BGA	500	-40°C to +85°C	✓	
ADSP-BF534BBCZ-5B	208 Sparse MiniBGA	500	-40°C to +85°C	✓	
ADSP-BF537					10/100 ethernet, CAN, PPI, TWI, 8 timers, 2 UARTs, SPI
ADSP-BF537BBC-5A	182-CSP_BGA	500	-40°C to +85°C		
ADSP-BF537BBCZ-5A	182-CSP_BGA	500	-40°C to +85°C	✓	
ADSP-BF537BBCZ-5B	208-CSP_BGA	500	-40°C to +85°C	✓	
ADSP-BF537BBCZ-5AV	182-CSP_BGA	500	-40°C to +85°C	✓	
ADSP-BF537BBCZ-5BV	208-CSP_BGA	500	-40°C to +85°C	✓	
ADSP-BF537KBCZ-6AV	182-CSP_BGA	600	-0°C to +70°C	✓	
ADSP-BF537KBCZ-6BV	208-CSP_BGA	600	-0°C to +70°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF536					10/100 ethernet, CAN, PPI, TWI, 2 UARTs, SPI, 8 timers
ADSP-BF536BBC-3A	182-CSP_BGA	300	-40°C to +85°C		
ADSP-BF536BBCZ-3A	182-CSP_BGA	300	-40°C to +85°C	✓	
ADSP-BF536BBCZ-3B	208 Sparse MiniBGA	300	-40°C to +85°C	✓	
ADSP-BF536BBC-4A	182-CSP_BGA	400	-40°C to +85°C		
ADSP-BF536BBCZ-4A	182-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF536BBCZ-4B	208-CSP_BGA	400	-40°C to +85°C	✓	
ADSP-BF561					Dual cores, 2 PPIs, UART, 12 timers, 2 SPORTs
ADSP-BF561SBB500	297-PBGA	500	-40°C to +85°C		
ADSP-BF561SBBZ500	297-PBGA	500	-40°C to +85°C	✓	
ADSP-BF561SBBCZ-5A	256-CSP_BGA	500	-40°C to +85°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Compliant	Key Peripherals[1]
ADSP-BF561SKBZ500	297-PBGA	500	0°C to +70°C	✓	
ADSP-BF561SKBCZ-5A	256-CSP_BGA	500	0°C to +70°C	✓	
ADSP-BF561SKBCZ-5V	256-CSP_BGA	533	0°C to +70°C	✓	
ADSP-BF561SBB600	297-PBGA	600	-40°C to +85°C		
ADSP-BF561SBBZ600	297-PBGA	600	-40°C to +85°C	✓	
ADSP-BF561SBBCZ-6A	256-CSP_BGA	600	-40°C to +85°C	✓	
ADSP-BF561SKBZ600	297-PBGA	600	0°C to +70°C	✓	
ADSP-BF561SKBCZ-6A	256-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF561SKBCZ-6V	256-CSP_BGA	600	0°C to +70°C	✓	
ADSP-BF535					PCI, USB device, 2 SPORTs, 2 SPI
ADSP-BF535PKB-350	260-PBGA	350	0°C to +70°C		
ADSP-BF535PKBZ-350	260-PBGA	350	0°C to +70°C	✓	

Table 1-1. Summary of Blackfin Processor Specifications (Cont'd)

Blackfin Family Matrix	Package	Clock Speed MHZ Max	Temp Range Ambient	RoHS Comp-liant	Key Peripherals[1]
ADSP-BF535PBB-300	260-PBGA	300	-40°C to +85°C		
ADSP-BF535PKB-300	260-PBGA	300	0°C to +70°C		
ADSP-BF535PKBZ-300	260-PBGA	300	0°C to +70°C	✓	
ADSP-BF535PBB-200	260-PBGA	200	-40°C to +85°C		
ADSP-BF535PBBZ-200	260-PBGA	200	-40°C to +85°C	✓	

1 Lists peripherals common to all models in the Blackfin series. Additional peripherals are listed in the row for each individual model.

Future Blackfin Processor Releases

Increased performance and a feature-rich variety of new peripherals are the focus in future Blackfin releases.

Blackfin Processor Features

Blackfin processors represent a class of devices that combine an extremely capable single-instruction, multiple-data SIMD processor engine with powerful features such as a memory protection unit, watchdog timer, real-time clock, variable-length RISC instructions, UARTs, and SPI ports. These features are typically found only in microcontrollers and microprocessors.

Because Blackfin processors possess all the power of a signal processor and are full featured, they can replace other classes of signal processors and 32-bit RISC MCUs or an ASIC in designs.

At the core, Blackfin processors have a 16-bit, dual MAC (multiply/accumulate) architecture with 32-bit registers and 64-bit internal data paths. This core is surrounded by high-speed memory and high-speed peripherals including 100 Mbps serial ports (SPORTs), a high-speed parallel peripheral interface (PPI) capable of moving digital video on and off chip (ITU-R/CCIR-656 compliant), UART with IrDA® support, SPI port, and an external memory interface for connection to SDRAM or DDR SDRAM, flash, SRAM, and so on.

In addition to its advanced peripherals, Blackfin processors include a software-programmable on-chip phase lock loop (PLL) that allows software to control the core and system clock speeds. Many Blackfin processors also feature an on-chip switching regulator to provide software control of core voltage as well. Either of these features used individually, or both used in tandem, can result in significant power savings because the clock and/or the voltage can be constantly varied, depending on the task at hand.

Because Blackfin processors can be used for both control/data processing and signal processing, the efficiency of data movement and storage has a high impact on performance. Efficient numerical precision is important, although efficiency of data movement is equally important. The measured width of a signal processing device is often based on the type of data it processes most efficiently. The width of a processor is typically measured by its data paths and register widths. Blackfin processors support 8-, 16-, and 32-bit arithmetic operations in hardware, but are optimized for (and have the most support for) 16-bit operations. Thus, Blackfin processors are considered to be 16/32-bit processors.

Performance

Processors can no longer be judged solely on core clock speed, MHz, MIPS, MACS, FLOPS, and so on. Newer Blackfin processors run at core clock frequencies starting at 300 MHz. Their internal memory is L1, which means that memory also runs at the core clock rate, providing large amounts of bandwidth between a processor's core and its internal memory. The core supports two 16-bit multiply/accumulates per cycle sustained, providing 1.2 GMACs at 600 MHz.

Although these numbers provide a rough idea of a device's performance, they do not measure how an application runs on a device because they do not take into account memory efficiency or instruction set efficiency. Often, these peak specifications occur only momentarily (that is, they are not sustained), and the sustained values are much lower. This is where benchmark data can be useful. "Benchmarks Against Other Processors" on page 1-33 describes performance measurements reported by third parties.

Figure 1-3 shows a chart that demonstrates power consumption versus speed for a 750 MHz Blackfin processor and various devices. What follows is the Berkeley Design Technology, Inc. (BDTI) text description of the figure:

> BDTImark2000™ scores for fixed-point DSPs based on their fastest family member. The BDTImark2000 is a summary measure of processors' DSP speed. The score is derived from a processor's performance on BDTI's DSP Kernel Benchmark™ suite. A higher BDTImark2000 score indicates a faster processor.

System developers can leverage the wide range of performance options available with Blackfin processors. Lower frequency, signal-core devices scale up to high-frequency, high-bandwidth, dual-core devices.

ADSP-BF561 Blackfin processors provide additional options for power management. Because this symmetric processor contains two identical cores, traditional processing-intensive applications can be split equally to run on each of the two cores. In this model, code running on each core is identical; only the data being processed is different. In a channel

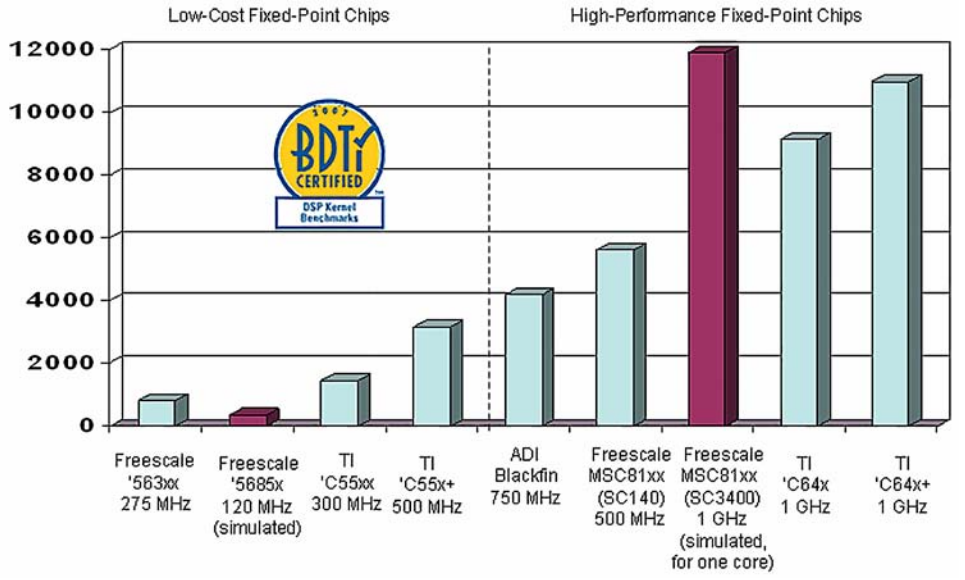


Figure 1-3. Power Consumption Versus Speed for Various Devices

streaming application, the first core processes half of the channels and the other core processes the other channels. In video and imaging applications, this technique can be used to process alternate frames on each of the cores.

Dual-core processing melds with the Blackfin processor's additional power savings features. The energy consumed by a processor is based on static and dynamic components. Even when the application fits on a single-core processor, you can employ a dual-core processor to reduce overall energy consumption. Specifically, by running an application at half the frequency of a single-core system, the processor core voltages can also be dropped to values as low as 0.9 V. This is possible because of the Blackfin processor's

wide voltage operating range. Dual-core Blackfin processors contain large amounts of on-chip memory along with data paths and DMA controllers that have been sized specifically to handle a shared processing load. This combination allows an algorithm to be split easily without the loss of efficiency that can be felt on multicore solutions with different processors.

Benchmarks Against Other Processors

When evaluating processors, it can be confusing to look at data sheets and compare the specifications. We recommend that you refer to accepted industry-standard benchmarks like BDTI, Dhrystone, Whetstone, and nbench.

The Dhrystone, Whetstone, and nbench benchmarks run under the Linux platform.

The benchmarks are presented in the following sections.

Dhrystone

The Dhrystone benchmark was designed to test performance factors important to non-numeric systems programming (operating systems, compilers, word processors, and so forth). It is notable in that:

- It contains no floating-point operations.
- A considerable percentage of time is spent in string functions making the test very dependent upon the way such operations are performed (for example, by in-line code, routines written in assembly language, and so on), making it susceptible to manufacturers "tweaking" of critical routines.

- It contains hardly any tight loops so in the case of very small caches, the majority of instruction accesses are misses; however, the situation changes radically as soon as the cache reaches a critical size and can hold the main measurement loop.
- Only a small amount of global data is manipulated (as opposed to Whetstone).

There are two versions of the Dhrystone benchmark. A deprecated version (Version 1.1) contained some "dead code" that could be removed by optimizing compilers. Version 2.1 corrected this and should be the version used in practice (and is the one that is in the µClinux distribution). Some manufacturers, however, still quote the (better) results of Version 1.1, so care must be taken when comparing Dhrystone performance figures to check which version was used.

Recent Dhrystone test results can be found at:
https://docs.blackfin.uclinux.org/doku.php?id=uclinux-dist:dhrystone

Whetstone

The Whetstone benchmark was first written to measure computer performance and was later designed to simulate floating-point numerical applications. The Whetstone benchmark is notable in that:

- It contains a large percentage of floating-point data and instructions.
- A high percentage of execution time (approximately 50%) is spent in mathematical library functions.
- The majority of its variables are global and the test does not show up the advantages of architectures such as RISC where the large number of processor registers enhance the handling of local variables.

- It contains a number of very tight loops; the use of even fairly small instruction caches will enhance performance considerably.
- The original program was written in Fortran using single- or double-precision calculations.

Recent Whetstone test results can be found at:
https://docs.blackfin.uclinux.org/doku.php?id=uclinux-dist:whetstone

nbench

nbench is a Linux/Unix port of release 2 of *BYTE Magazine's* BYTEmark benchmark program (previously known as BYTE's Native Mode Benchmarks). These are native mode (also known as algorithm level) tests. They are benchmarks designed to expose the capabilities of a system's CPU, FPU, and memory system. Read more about it at *BYTE Magazine's* benchmark page.

This benchmark program takes less than ten minutes to run (on most machines) and compares the system it is run against to two benchmark systems (a Dell Pentium 90 with 256 KB cache running MSDOS, and an AMD K6/233 with 512 KB cache running Linux). The following listing shows the nbench Blackfin compilation results.

Listing 1-1. nbench Blackfin Compilation Results

```
root:~> nbench

BYTEmark* Native Mode Benchmark ver. 2 (10/95)
Index-split by Andrew D. Balsa (11/97)
Linux/Unix* port by Uwe F. Mayer (12/96,11/97)

TEST                : Iterations/sec.  : Old Index   : New Index
                    :                  : Pentium 90* : AMD K6/233*
```

```
--------------------:------------------:-----------:------------
NUMERIC SORT        :          116.12  :       2.98  :       0.98
STRING SORT         :          3.8685  :       1.73  :       0.27
BITFIELD            :      4.7085e+07  :       8.08  :       1.69
FP EMULATION        :          22.923  :      11.00  :       2.54
FOURIER             :          94.582  :       0.11  :       0.06
ASSIGNMENT          :          1.6106  :       6.13  :       1.59
IDEA                :          355.45  :       5.44  :       1.61
HUFFMAN             :          146.31  :       4.06  :       1.30
NEURAL NET          :         0.10077  :       0.16  :       0.07
LU DECOMPOSITION    :          3.5476  :       0.18  :       0.13
================ORIGINAL BYTEMARK RESULTS==================
INTEGER INDEX       : 4.836
FLOATING-POINT INDEX: 0.147
Baseline (MSDOS*)   : Pentium* 90, 256 KB L2-cache, Watcom* com-
piler 10.0
=========================LINUX DATA BELOW=============
CPU                 :
L2 Cache            :
OS                  : Linux 2.6.19.3-ADI-2007R1-pre-svn2773
C compiler          : bfin-linux-uclibc-gcc
libc                : static
MEMORY INDEX        : 0.895
INTEGER INDEX       : 1.509
FLOATING-POINT INDEX: 0.082
Baseline (LINUX)    : AMD K6/233*, 512 KB L2-cache, gcc 2.7.2.3,
libc-5.4.38
* Trademarks are property of their respective holder.
```

BDTI

If your application requires a great deal of signal processing, examine the BDTI Benchmark™ results.

These test results were obtained using a VisualDSP++ compiler.

The following paragraphs, taken from the BDTI Web site, describe the company's evaluation process and conclusions.

Company Background

BDTI was formed in 1991 as an extension of the founders' work in developing DSP design tools, methodologies, and architectures at the University of California at Berkeley. In the years since its inception, BDTI has continued to expand both its engineering and management staff by hiring a diverse and talented group of DSP specialists. BDTI's customers include major semiconductor, consumer electronics, telecommunications, and design tool companies who are leaders in the application of DSP technology.

Processor Benchmarking and Analysis

Benchmarks from BDTI are a trusted, independent means to measure and compare performance in signal processing applications. BDTI provides the BDTI Benchmarks™, a suite of algorithm kernel benchmarks, and also the BDTI DSP Application Benchmarks™, which represent key signal processing applications. BDTI licenses its benchmark suites for vendor use, and can implement the benchmarks if needed.

BDTI's benchmark suites have been implemented on a wide range of DSPs, general-purpose processors, and FPGAs. Nearly all mainstream processors used in signal processing applications today have been benchmarked with the BDTI Benchmarks.

Beyond the benchmark results, BDTI analyzes processors and FPGAs to provide invaluable perspective and insight. BDTI's rigorous, in-depth evaluations identify competitive strengths and weaknesses, and serve the needs of both engineering and marketing.

The BDTI Benchmark Suites™

Good benchmarks are essential for evaluating and comparing technologies, for making informed decisions, and for developing credible marketing programs. But not all benchmarks are created equal, and using the wrong benchmarks can result in poor decisions, ineffective marketing, and failed products.

BDTI has over a decade of experience in developing and implementing signal processing benchmarks for chips, systems, and tools. We are the only vendor-independent source for signal processing benchmarks. We've benchmarked the signal-processing performance of DSP processors, general-purpose processors, multi-core processors, and reconfigurable cores, among other targets. If you use BDTI's benchmarks, you'll be confident that you're working with technically sound and unbiased performance data.

About the Scores

The BDTImark2000™ is a summary measure of processors' signal processing speed. The score is distilled from a processor's results on the BDTI DSP Kernel Benchmarks, a suite of 12 key DSP algorithms. A higher score indicates a faster processor.

Because it is based on realistic benchmarks, the BDTImark2000 characterizes a processor's signal processing speed far more accurately than simplified measures such as millions of multiply-accumulates per second (MMACS).

BDTI's policy is to verify benchmark results on silicon before issuing a BDTImark2000 score. This policy helps to ensure that the score accurately reflects the performance that can be expected from actual silicon available today.

However, it is not always practical to verify benchmarks on hardware. For example, a chip designer may need to evaluate a licensable core before the core has been fabricated. To meet such needs, BDTI publishes the **BDTIsimMark2000™**. This metric is calculated in the same manner as the BDTImark2000, but is based on simulated results instead of hardware measurements.

Although BDTIsimMark2000 and BDTImark2000 scores are calculated in the same manner, they should be compared with caution. In addition, caution should be used when comparing scores for chips to scores for cores.

The BDTImemMark2000™ is a summary measure of processors' memory efficiency on signal processing applications. The BDTImemMark2000 is based on the same suite of signal processing benchmarks as the BDTImark2000 and BDTIsimMark2000. A higher BDTImemMark2000 score indicates a more efficient processor. That is, a higher BDTImemMark2000 score indicates *lower* memory use. Memory efficiency is important for two reasons: First, a processor's memory efficiency has a significant impact on overall system cost and energy consumption. Second, a processor may experience significant performance degradation if frequently-accessed application code and data do not fit in level-one memory.

The BDTImark2000, BDTIsimMark2000, and BDTImemMark2000 summarize performance on the 12 BDTI DSP Kernel Benchmarks. These summary metrics are useful for making first-order assessments of processors. System designers can obtain a more accurate assessment—one that takes into account the nature of their applications—by inspecting the results for each of the BDTI DSP Kernel Benchmarks. System designers can obtain these individual results by purchasing a BDTI report or by licensing the BDTI Benchmark Analysis Tool™.

Using their May and July 2006 benchmark scores, BDTI compares devices with regard to power consumption, speed, and price. Figure 1-4 and Figure 1-5 look at processor speed and Figure 1-6 examines memory use. Figure 1-7 and Figure 1-8 examine speed versus cost, while Figure 1-9 and Figure 1-10 examine speed versus power. Clearly Blackfin processors are highly competitive based on processors that have been certified by BDTI.

To learn more about the BDTI benchmarks and find out how Blackfin processors perform against the competition, go to the following BDTI Web page:
`http://www.BDTI.com/benchmarks.html`

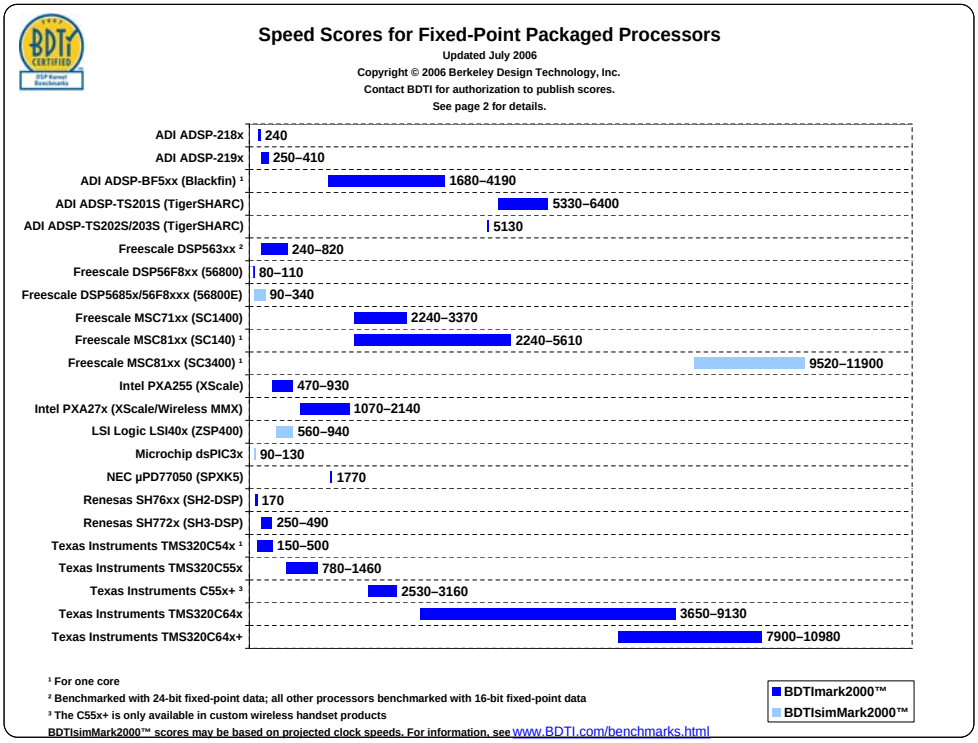


Figure 1-4. BDTI Comparisons as of July 2006: Processor Speed Graph

Speed Scores for Fixed-Point Packaged Processors

Updated July 2006

Processor Family	Clock Rate (min-max)	**BDTImark2000™**, *BDTIsimMark2000™* (min-max)
ADI ADSP-218x	80 MHz	**240**
ADI ADSP-219x	100–160 MHz	**250–410**
ADI ADSP-BF5xx (Blackfin) [1]	300–750 MHz	**1680–4190**
ADI ADSP-TS201S (TigerSHARC)	500–600 MHz	**5330–6400**
ADI ADSP-TS202S/203S (TigerSHARC)	500 MHz	**5130**
Freescale DSP563xx [2]	80–275 MHz	**240–820**
Freescale DSP56F8xx (56800)	60–80 MHz	**80–110**
Freescale DSP5685x/56F8xxx (56800E)	32–120 MHz	*90–340*
Freescale MSC71xx (SC1400)	200–300 MHz	**2240–3370**
Freescale MSC81xx (SC140) [1]	200–500 MHz	**2240–5610**
Freescale MSC81xx (SC3400) [1]	800–1000 MHz	*9520–11900*
Intel PXA255 (XScale)	200–400 MHz	**470–930**
Intel PXA27x (XScale/Wireless MMX)	312–624 MHz	**1070–2140**
LSI Logic LSI40x (ZSP400)	120–200 MHz	**560–940**
Microchip dsPIC3x	30–40 MHz	*90–130*
NEC µPD77050 (SPXK5)	250 MHz	*1770*
Renesas SH76xx (SH2-DSP)	62.5 MHz	**170**
Renesas SH772x (SH3-DSP)	100–200 MHz	**250–490**
Texas Instruments TMS320C54x [1]	50–160 MHz	**150–500**
Texas Instruments TMS320C55x	160–300 MHz	**780–1460**
Texas Instruments C55x+ [3]	400–500 MHz	**2530–3160**
Texas Instruments TMS320C64x	400–1000 MHz	**3650–9130**
Texas Instruments TMS320C64x+	720–1000 MHz	**7900–10980**

[1] For one core
[2] Benchmarked with 24-bit fixed-point data; all other processors benchmarked with 16-bit fixed-point data
[3] The C55x+ is only available in custom wireless handset products

BDTImark2000™, BDTIsimMark2000™: The BDTImark2000™ and BDTIsimMark2000™ provide a summary measure of signal processing speed. BDTIsimMark2000™ scores may be based on projected clock speeds. For more info and scores see:
www.BDTI.com/benchmarks.html

Figure 1-5. BDTI Scores as of July 2006: Processor Speed Chart

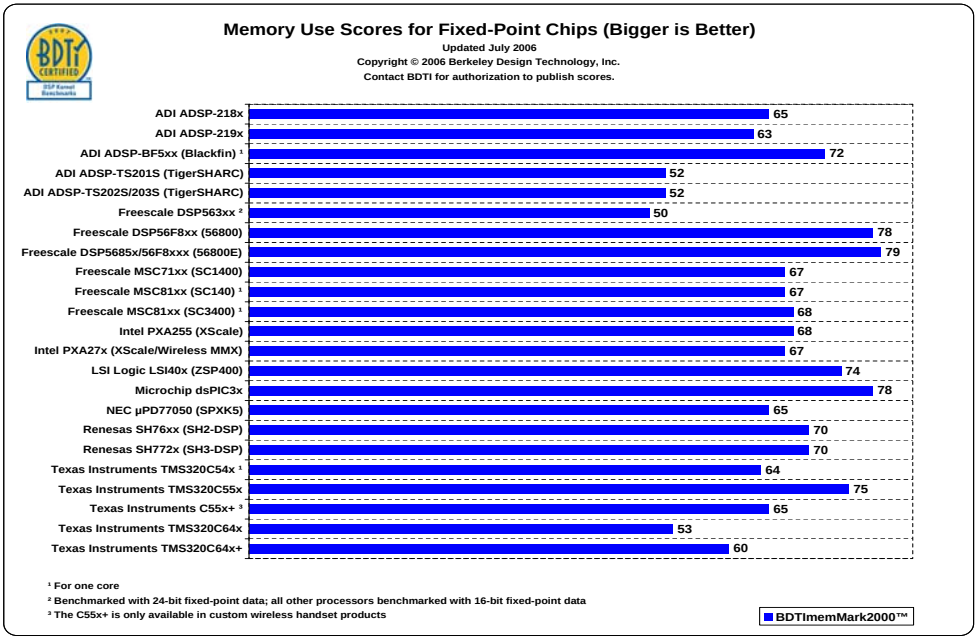


Figure 1-6. BDTI Scores as of July 2006: Memory Use Graph

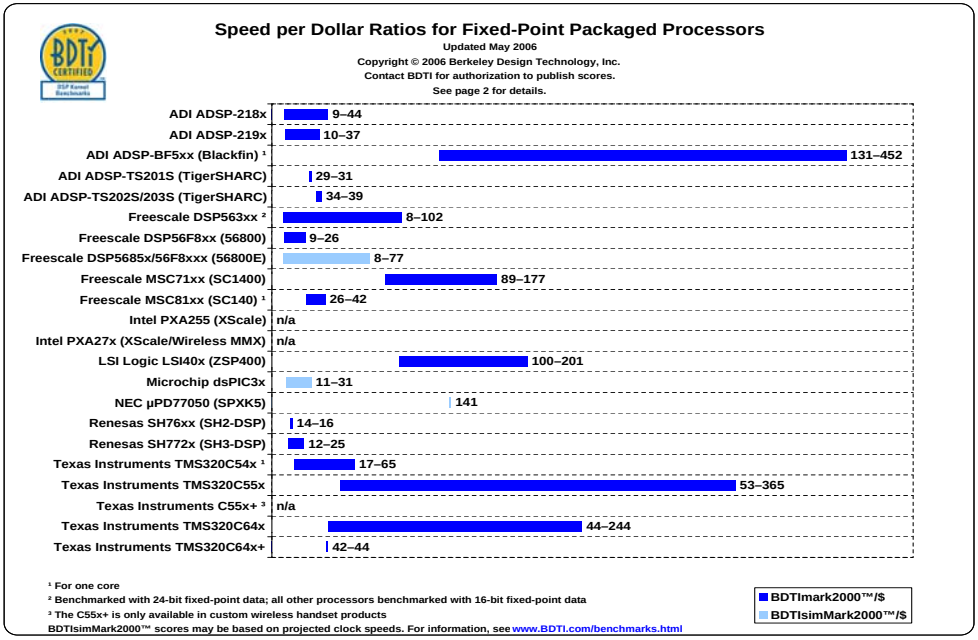


Figure 1-7. BDTI Scores as of May 2006: Speed versus Cost Graph

Speed per Dollar Ratios for Fixed-Point Packaged Processors

Updated May 2006

Contact BDTI for authorization to publish scores.

Processor Family	Clock Rate (min-max)	**BDTImark2000™**, *BDTIsimMark2000™* (min-max)	Cost (min-max)	**BDTImark2000™/$**, *BDTIsimMark2000™/$* (min-max)
ADI ADSP-218x	80 MHz	**240**	$6–26	**9–44**
ADI ADSP-219x	100–160 MHz	**250–410**	$11–26	**10–37**
ADI ADSP-BF5xx (Blackfin) [1]	300–750 MHz	**1680–4190**	$5–32	**131–452**
ADI ADSP-TS201S (TigerSHARC)	500–600 MHz	**5330–6400**	$186–205	**29–31**
ADI ADSP-TS202S/203S (TigerSHARC)	500 MHz	**5130**	$131–149	**34–39**
Freescale DSP563xx [2]	80–275 MHz	**240–820**	$4–47	**8–102**
Freescale DSP56F8xx (56800)	60–80 MHz	**80–110**	$3–12	**9–26**
Freescale DSP5685x/56F8xxx (56800E)	32–120 MHz	*90–340*	$3–20	*8–77*
Freescale MSC71xx (SC1400)	200–300 MHz	**2240–3370**	$13–35	**89–177**
Freescale MSC81xx (SC140) [1]	200–500 MHz	**2240–5610**	$76–184	**26–42**
Intel PXA255 (XScale)	200–400 MHz	**470–930**	n/a	n/a
Intel PXA27x (XScale/Wireless MMX)	312–624 MHz	**1070–2140**	n/a	n/a
LSI Logic LSI40x (ZSP400)	120–200 MHz	**560–940**	$4–9	**100–201**
Microchip dsPIC3x	30–40 MHz	*90–130*	$3–8	*11–31*
NEC µPD77050 (SPXK5)	250 MHz	*1770*	$13	*141*
Renesas SH76xx (SH2-DSP)	62.5 MHz	**170**	$11–13	**14–16**
Renesas SH772x (SH3-DSP)	100–200 MHz	**250–490**	$17–23	**12–25**
Texas Instruments TMS320C54x [1]	50–160 MHz	**150–500**	$3–24	**17–65**
Texas Instruments TMS320C55x	160–300 MHz	**780–1460**	$4–17	**53–365**
Texas Instruments C55x+ [3]	400–500 MHz	**2530–3160**	n/a	n/a
Texas Instruments TMS320C64x	400–1000 MHz	**3650–9130**	$15–208	**44–244**
Texas Instruments TMS320C64x+	720–1000 MHz	**7900–10980**	$179–259	**42–44**

[1] For one core

[2] Benchmarked with 24-bit fixed-point data; all other processors benchmarked with 16-bit fixed-point data

[3] The C55x+ is only available in custom wireless handset products

BDTImark2000™, BDTIsimMark2000™: The BDTImark2000™ and BDTIsimMark2000™ provide a summary measure of signal processing speed. BDTIsimMark2000™ scores may be based on projected clock speeds. For information see: www.BDTI.com/benchmarks.html

Note: In general, BDTImark2000™/$ and BDTIsimMark2000™/$ scores cannot be computed from the speed and pricing data presented here. For example, the fastest processors are not always the most expensive processors. Therefore, it is not always possible to calculate a speed per dollar ratio by dividing the maximum speed for a family by the maximum price for the family.

Figure 1-8. BDTI Scores as of May 2006: Speed versus Cost Chart

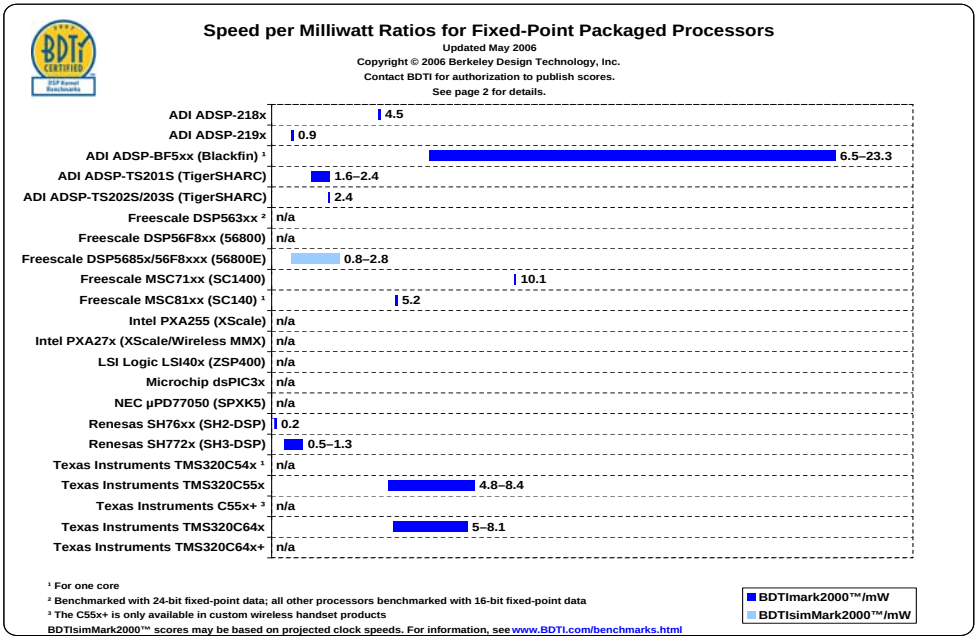


Figure 1-9. BDTI Scores as of May 2006: Speed versus Power Graph

Speed per Milliwatt Ratios for Fixed-Point Packaged Processors

Updated May 2006

Contact BDTI for authorization to publish scores.

Processor Family	Clock Rate (min-max)	**BDTImark2000™**, *BDTIsimMark2000™* (min-max)	Power (min-max)	**BDTImark2000™/mW**, *BDTIsimMark2000™/mW* (min-max)
ADI ADSP-218x	80 MHz	**240**	54 mW	**4.5**
ADI ADSP-219x	100–160 MHz	**250–410**	460 mW	**0.9**
ADI ADSP-BF5xx (Blackfin) [1]	300–750 MHz	**1680–4190**	24–644 mW	**6.5–23.3**
ADI ADSP-TS201S (TigerSHARC)	500–600 MHz	**5330–6400**	2583–3907 mW	**1.6–2.4**
ADI ADSP-TS202S/203S (TigerSHARC)	500 MHz	**5130**	2583 mW	**2.4**
Freescale DSP563xx [2]	80–275 MHz	**240–820**	n/a	n/a
Freescale DSP56F8xx (56800)	60–80 MHz	**80–110**	n/a	n/a
Freescale DSP5685x/56F8xxx (56800E)	32–120 MHz	*90–340*	120–213 mW	*0.8–2.8*
Freescale MSC71xx (SC1400)	200–300 MHz	**2240–3370**	222–333 mW	**10.1**
Freescale MSC81xx (SC140) [1]	200–500 MHz	**2240–5610**	433–650 mW	**5.2**
Intel PXA255 (XScale)	200–400 MHz	**470–930**	n/a	n/a
Intel PXA27x (XScale/Wireless MMX)	312–624 MHz	**1070–2140**	n/a	n/a
LSI Logic LSI40x (ZSP400)	120–200 MHz	**560–940**	n/a	n/a
Microchip dsPIC3x	30–40 MHz	*90–130*	n/a	n/a
NEC µPD77050 (SPXK5)	250 MHz	*1770*	n/a	n/a
Renesas SH76xx (SH2-DSP)	62.5 MHz	**170**	1080 mW	0.2
Renesas SH772x (SH3-DSP)	100–200 MHz	**250–490**	375–1020 mW	**0.5–1.3**
Texas Instruments TMS320C54x [1]	50–160 MHz	**150–500**	n/a	n/a
Texas Instruments TMS320C55x	160–300 MHz	**780–1460**	62–204 mW	**4.8–8.4**
Texas Instruments C55x+ [3]	400–500 MHz	**2530–3160**	n/a	n/a
Texas Instruments TMS320C64x	400–1000 MHz	**3650–9130**	654–1303 mW	**5–8.1**
Texas Instruments TMS320C64x+	720–1000 MHz	**7900–10980**	n/a	n/a

[1] For one core
[2] Benchmarked with 24-bit fixed-point data; all other processors benchmarked with 16-bit fixed-point data
[3] The C55x+ is only available in custom wireless handset products

BDTImark2000™, BDTIsimMark2000™: The BDTImark2000™ and BDTIsimMark2000™ provide a summary measure of signal processing speed. BDTIsimMark2000™ scores may be based on projected clock speeds. For information see: www.BDTI.com/benchmarks.html

Note: In general, BDTImark2000™/mW and BDTIsimMark2000™/mW scores cannot be computed from the speed and power data presented here. For example, the fastest processors are not always the highest-power processors. Therefore, it is not always possible to calculate a speed per milliwatt ratio by dividing the maximum speed for a family by the maximum power for the family.

Figure 1-10. BDTI Scores as of May 2006: Speed versus Power Chart

EEMBC

If the application demands the performance of a signal processing engine and a microcontroller, examine what the Embedded Microprocessor Benchmark Consortium (EEMBC) says about Blackfin processors.

These test results were obtained using a VisualDSP++ compiler.

The following paragraphs are taken from the EEMBC Web site.

> EEMBC, the Embedded Microprocessor Benchmark Consortium, was formed in 1997 to develop meaningful performance benchmarks for the hardware and software used in embedded systems. Through the combined efforts of its members, EEMBC® benchmarks have become an industry standard for evaluating the capabilities of processors, compilers, and Java implementations according to objective, clearly defined, application-based criteria.
>
> Since releasing its first certified benchmark scores in April 2000, EEMBC scores have effectively replaced the obsolete Dhrystone mips, especially in situations where real engineering value is important. EEMBC benchmarks reflect real-world applications and the demands that embedded systems encounter in these environments. The result is a collection of "algorithms" and "applications" organized into benchmark suites targeting telecommunications, networking, digital media, Java, automotive/industrial, consumer, and office equipment products. An additional suite of algorithms specifically targets the capabilities of 8- and 16-bit microcontrollers.
>
> EEMBC's certification rules represent another break with the past. For a processor's scores to be published, the EEMBC Certification Laboratories (ECL) must execute benchmarks run by the manufacturer. ECL certification ensures that scores are repeatable, obtained fairly, and according to EEMBC's rules. Scores for devices that have been tested and certified by ECL can be searched from our Benchmark Search page.

To find out more about how Blackfin processors perform compared to the competition, go to the following EEMBC Web page:
`http://www.eembc.org`

Based on recent EEMBC data, Figure 1-11 shows results of various EEMBC benchmarks.

EEMBC Benchmarks

Processor	Blackfin	ARM1136JF-S™	ARM926EJ-S™
Product	BF533	i.MX31	i.MX21
Clock Frequency (MHz)	594	532	266
Certified on Hardware?	yes	yes	yes
EEMBC Networking 2.0*			
IPmark**	45	**50.4**	24.4
TCPmark**	**117**	68.5	29.2[a]
EEMBC AutoBench 1.1*			
Automark**	**183.1**	126.6	29.6
EEMBC ConsumerBench 1.1*			
Consumermark**	**54.9**	26.6	13.7
EEMBC OABench 1.1*			
OAmark**	**352**	341	152
EEMBC TeleBench 1.1*			
Telemark**	**11.7**	6.1	2.5
EEMBC DENBench 1.0*			
MPEG Decodemark**	**337**	231	112
MPEG Encodemark**	**392**	243	100
Cryptomark**	**257**	219	104
Imagemark**	**352**	315	154
DENmark**	**57.5**	45.5	21.6
Geometric Mean	**138.7**	**99.3**	**42.6**

* Out-of-the-box category
** bigger is better

[a] i.MX21 TCPmark contains an estimate for one subtest whose result is filed n/a at EEMBC. (Estimate was ½ i.MX31 performance.)

Figure 1-11. EEMBC: Assorted Benchmark Results

Analog Devices Benchmarks

Analog Devices has assembled benchmarks to test Blackfin processors. The synergy of the Blackfin processor architecture and the VisualDSP++ complier yields high-density code.

Links to Comparative Benchmarks

Access comparative data to see how Blackfin processors compare to other manufacturers' parts.

Open your browser and access the following Web page, which contains links to the BDTI and EEMBC Web sites:
http://www.analog.com/processors/blackfin/overview/benchmarks/index.html

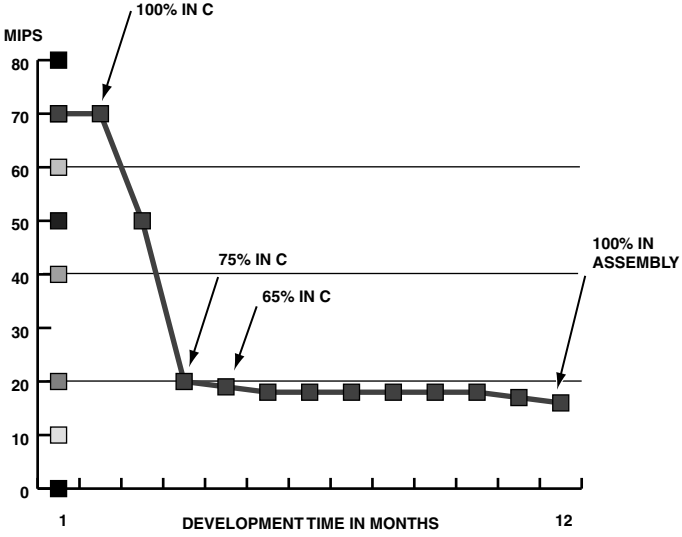
Blackfin Processor Compiler and Code Density

Blackfin processors coupled with the powerful VisualDSP++ software development tools now make it possible to develop code in C/C++ more easily and efficiently than before. The high MIPS availability from the core processor allows for initial versions of software to be compiled and run on the processor much earlier in the design cycle, thus allowing for quicker overall system debug to shorten time to market. The goal is to alleviate software as a potential critical path element in system development.

Figure 1-12 shows an example of the code development efficiency on Blackfin processors using an adaptive multi-rate (AMR) encoder.

COMPILER RESULTS IN FULLY FUNCTIONAL CODE
FROM FIRST WEEK OF IMPLEMENTATION.

PERSON MONTHS	PERCENTAGE IN C	PERCENTAGE OVERHEAD
0.25	100	366
3.00	75	36
5.00	65	20
12.00	0	0



AMR ENCODER CODE DEVELOPMENT EFFICIENCY

Figure 1-12. The VisualDSP++ Compiler Yields High-Density Code

2 THE EVALUATION PROCESS

This chapter introduces software and hardware tools that are currently available. Topics include:

Selecting Software Development Tools

This section examines the process through which Blackfin processor applications are developed. Various tools are used at each stage, where typical application development occurs over multiple stages. The section provides a summary of the available software development tools for Blackfin processors.

Most users acquire a set of *software development tools* first. The software development tools run on a PC and provide code generation and debug utilities such as a compiler, assembler, linker, simulator, debugger, and libraries.

Currently, three sets of software development tools are available for the Blackfin processor architecture:

- VisualDSP++ 5.0 from Analog Devices
- MULTI® from Green Hills Software
- Open source GCC tool chain and µClinux

Each offers advantages for different types of applications. Other software development tools are available in languages such as Japanese and Chinese. Contact your local Analog Devices sales office or distributor for more information. Figure 2-1 on page 2-3 shows the tool selection workflow.

VisualDSP++ From Analog Devices

VisualDSP++ is an easy-to-install and easy-to-use integrated software development and debugging environment (IDDE) that enables efficient management of projects from start to finish from within a single interface.

Because project development and debugging is integrated, you can move quickly and easily between editing, building, and debugging activities. Key features include the native C/C++ compiler, advanced graphical plotting tools, statistical profiling, and the VisualDSP++ kernel (VDK), which allows a user's code to be implemented in a more structured and easier-to-scale manner. Other features include assembler, linker, libraries, splitter, cycle-accurate and functional-accurate compiled simulators, emulator support, and more. VisualDSP++ offers programmers a powerful yet easy-to-use programming tool with flexibility that significantly reduces the time to market.

Platform and Processor Support

VisualDSP++ supports Blackfin processors from Analog Devices. Windows® Vista, Windows XP, and Windows 2000 hosts are supported.

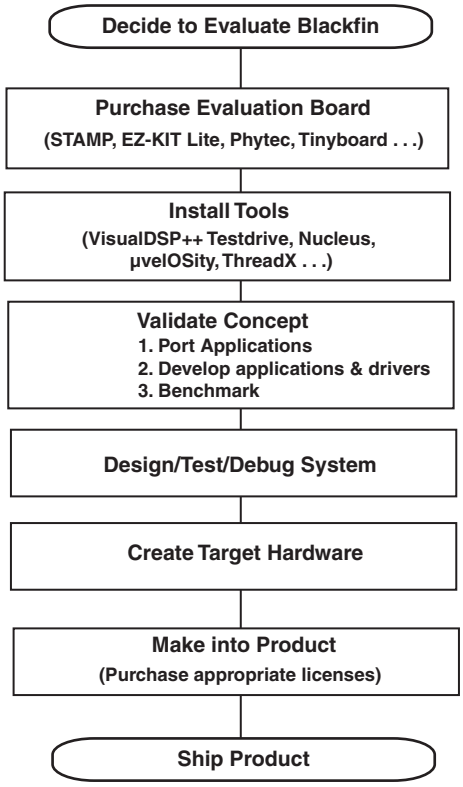


Figure 2-1. Tool Selection Workflow

Develop High-Performance Applications Quickly

At the heart of VisualDSP++ is a robust and powerful C/C++ compiler. The compiler consistently delivers industry-leading performance on standard benchmarks, ensuring that all but the most performance-demanding applications can be written entirely in the C language, accelerating

development time while maintaining a portable code base. The compiler is backed by a rich library of signal processing routines, allowing easy access to hand-coded, optimized implementations of FFTs, FIRs, and so forth.

The ANSI-C compiler is also augmented with popular language extensions and enhancements to make it more amiable to existing code bases. Examples include GNU GCC extensions, ETSI fractional libraries, and multiple heap support.

A compiler's overriding mission is to produce correct code, so there are occasions when the compiler must take a conservative approach to a code sequence when a more aggressive approach could have been taken if certain constraints could be guaranteed by the programmer. The VisualDSP++ compiler supports a broad range of pragmas that allow the programmer to better exploit the compiler while maintaining C language neutrality. Just as important, the compiler has the ability to feed back advisory information to the programmer, offering further improvements to a code sequence, should the programmer be able to make certain guarantees about it. This information is displayed seamlessly in the VisualDSP++ main editor window. This removes the black box label that compilers sometimes have.

Backing the compiler is a powerful assembler and linker technology. Processors from Analog Devices are noted for their intuitive algebraic assembly language syntax, and the VisualDSP++ assembler extends that ease of use with the ability to import C header files, allowing for symbolic references into arbitrarily complex C data structures. Binary data can be included directly into assembly source files, creating an easy way to add blocks of static data (such as audio samples and bitmaps) to an application. The VisualDSP++ linker is fully multicore and multiprocessor (MP) aware, allowing for the creation of cross-linked, multi-executable applications in a single pass. Other powerful capabilities of the linker include dead code and data elimination, code and data overlays, section spilling (that is, automatic overflow from internal to external memory), and automatic short-to-long call expansion.

Leverage-Proven Application Infrastructure

VisualDSP++ goes beyond robust code generation tools, providing considerable application infrastructure and middleware out of the box to speed application development. The VisualDSP++ kernel (VDK) is a robust, royalty-free, real-time operating system (RTOS) kernel. It provides essential kernel features in a minimal footprint. Features include a fully pre-emptive scheduler (time slicing and cooperative scheduling are also supported), thread creation, semaphores, interrupt management, inter-thread messaging, events, and memory management (memory pools and multiple heaps). In MP environments, messaging is also provided. Configuration of these elements is done graphically, with code wizards to speed the creation of new threads and interrupt handlers. VDK has been available for multiple releases of VisualDSP++ and is now a key component of products shipping from several high-volume vendors.

Blackfin processors can take advantage of the system service library, which provides consistent, easy C language access to Blackfin features such as the interrupt manager, direct memory access (DMA), and power management units. Clock frequency and voltage can be changed easily at run time through a set of simple APIs. Interrupt handling can be live, fired at the time of the event, or deferred to a later time of the application's choosing. A device manager integrates device drivers for on- and off-chip peripherals. VisualDSP++ includes device driver support for all on-chip peripherals and off-chip devices found on Analog Devices EZ-KIT Lite and EZ-Extender products. The system service library is OS-neutral and can be run standalone or in conjunction with an RTOS.

As embedded applications become increasingly part of the connected world, the ability to rapidly add reliable ethernet or USB connectivity to an application can often make or break a development schedule. For Blackfin processors, VisualDSP++ includes a tuned port of the open source LwIP TCP/IP stack. An example application showcasing an embedded Web server is among the highlights of this support. USB 2.0

device connectivity is provided. Bulk and asynchronous transfer modes are supported out of the box. Host applications are provided with full source code.

The VisualDSP++ state-of-the-art integrated development and debugging environment (IDDE) includes full-featured editing and project management tools. It uses incremental builds, multiple build configurations ("Debug" and "Release," for example), a syntax-coloring editor, and many other code editing features. Makefiles can be imported and exported freely. Many application attributes can be configured graphically, enabling point-and-click access to SDRAM setup, stack and heap placement, power management, clock speed, cache setup, and more.

Debug and Tune Your Application With Ease

The ability to develop a high-performance application is often gated by the visibility into your running system that your debugger provides. VisualDSP++ excels in this regard, with best-in-class debugging and inspection support. Robust fundamental C language source debugging (source-level stepping and breakpoints, stack unwinds, local variable and C expression support, memory and register windows) serves as a foundation upon which multiple innovative and unique tools rest.

VisualDSP++ supports a variety of debug targets. Most common is a JTAG (Joint Test Action Group) connection to an EZ-KIT Lite board or to a custom target board by means of Analog Devices emulator products. However, there will be occasions where closer inspection in a simulated environment may be required. VisualDSP++ provides cycle-accurate simulators, allowing inspection of every nuance of activity within the processor core, including visualization of the processor's pipeline and cache. These simulators are robust and highly accurate, so much so that silicon designers at Analog Devices use them for validation. A second simulator is available to Blackfin processor users—a high-speed, functional simulator. Using proprietary just-in-time (JIT) technology, the simulators have the ability to model millions of cycles per second on the most modest of host

PCs. Effectively, this means that what used to be an overnight run is now a 10-minute coffee break, and what was once a coffee break is now a near-instantaneous simulation.

As many of the most performance-demanding applications process a signal of some sort, comprehensive memory plotting is a cornerstone of VisualDSP++ debugger support. VisualDSP++ provides multiple views, from basic (line plots) to sophisticated (eye diagrams and waterfalls) to pinpoint anomalous data sequences in your application. Image viewing in a number of data formats is also available.

Users of the VDK get unparalleled visibility into the internals of the kernel. Status on a per-thread basis is available, as is a comprehensive pictorial history of kernel events and CPU loading. Thread changes, posted and pended semaphores, and other kernel events are captured in this display.

Inspection, or even application stimulation, from the debugger at run time is possible through the use of the processor's background telemetry channels (BTCs). BTCs allow for an arbitrary number of communication channels to be established between the host debugger and the application. Channels may go in either direction, so BTCs can be used to read and write data as the processor runs. Scalar values or entire arrays may be serviced by a channel. Arrays read from the target can even be plotted in real time.

Multiprocessor (MP) users get the same set of debugging features across all processors, unified into a single debugging interface. Individual windows can be made to float their focus to whichever processor currently is the debugger's focus, or they can be pinned to a specific processor so their contents do not follow the debugger's focus. To further aid MP debug, synchronous run, step, halt, and reset are also provided.

The patented statistical profiler from Analog Devices offers unprecedented and unique visibility into a running application. Operating completely non-intrusively to the application, the application is polled thousands of

times per second and a statistical view of where an application is spending the majority of its time is quickly assembled. This tool can be used to easily inspect an application for unexpected hotspots (for example, suggesting the need to move a key routine from external to internal memory). Simulator targets provide a completely linear profiling view. For Blackfin processors, traditional instrumented profiling is also available.

Going even further, the VisualDSP++ compiler is able to act upon profiling information. Profile-guided optimization (PGO) is a technique that allows the compiler to instrument an application, run the application, and then make a second pass compilation, exploiting the information that was gathered during the previous run of the application. This gives the compiler unique insight on a block-by-block basis, allowing it to optimize with a level of granularity that is not possible with a tool that operates only on a file-by-file basis.

Integrate Into Your Existing Environment

A development tool suite is always a part of an organization's larger software engineering environment. VisualDSP++ has been designed to operate in a larger environment.

An embedded engineer is often developing on a new platform while maintaining existing products that were likely developed with an earlier version of the tools. VisualDSP++ can be installed discretely an arbitrary number of times at a variety of release levels, allowing engineering to easily switch between current and legacy versions of VisualDSP++.

To better integrate to source code control (SCC) systems, VisualDSP++ is able to connect to any SCC provider that supports the Microsoft® common source code control (MCSCC) interface. This interface is supported by all leading SCC vendors. VisualDSP++ goes one step further by supporting the control of VisualDSP++ itself within a source code control system.

The ability to robustly test an embedded application is enabled through a comprehensive automation application programmers interface (API). Using Microsoft's language-neutral automation technology, nearly every feature of the graphical environment is available to script authors. Applications can be rebuilt, downloaded, and run from a simple script executed from the command line or from within a custom test harness framework. The automation API is supported by C++ and VBScript examples for all API calls, though any automation-aware language can be used.

For prototype runs and/or small volume deployment, an Analog Devices emulator can be used to flash a program onto your custom system. Accessible through the automation API, the flash programmer can be scripted, making it possible to develop a turnkey user interface for use by a production floor technician or other individual not familiar with VisualDSP++. Device drivers are provided for all flash devices found on EZ-KIT Lite products, and these drivers can be easily adjusted to support an arbitrary flash device.

Get Help and Stay Up to Date

Analog Devices is aware that best-in-class customer support is ultimately in the interest of both customers and Analog Devices in the long run. Analog Devices is committed to this customer support for VisualDSP++.

VisualDSP++ includes a comprehensive, indexed, searchable online Help system. In addition to information concerning VisualDSP++, manuals for Analog Devices processors, application notes, and more are included in the Help system. The `.pdf` file versions of these documents are also available on the installation CD or online at:
`http://www.analog.com/processors`

Licensed users of VisualDSP++ are entitled to free technical support. The support staff is dedicated to VisualDSP++ and has specific expertise regarding it. There is never a per-incident or maintenance fee; support remains free regardless of how long you have owned your software.

Major and minor upgrades and updates to VisualDSP++ are also free and are released through the Analog Devices Web site.

Use The Collaborative

The Collaborative™ is an independent network of third-party developers. For more information, see “The Collaborative” on page 3-21.

Take a VisualDSP++ Test Drive!

Take a free 90-day test drive of VisualDSP++. To take a test drive, you can download a test drive or request a CD from the Analog Devices DSP Tools Web site at `http://www.analog.com/processors/tools/testdrive` or contact your local Analog Devices sales representative/distributor.

Analog Devices Tools

CROSSCORE® (development tools from Analog Devices) provides easier and more robust methods for engineers to develop and optimize systems by shortening product development cycles for faster time to market. The CROSSCORE components include the VisualDSP++ software development environment, EZ-KIT Lite evaluation systems, EZ-Extender daughterboards, and emulators for rapid on-chip debugging. For more information on development tools, visit the Analog Devices Web site at: `http://www.analog.com/processors/tools`

Embedded Processors and DSPs

Blackfin processors and integrated mixed-signal DSPs are ideal for an ever-increasing spectrum of applications. Advances in design from Analog Devices provide faster processing, more memory, lower power consumption, and simplified system integration. Analog Devices products and technology provide a competitive edge complete with expert technical support, comprehensive development tools, and third-party developers.

Code Examples

Specific code examples for many DSP algorithms optimized for Blackfin processors are currently available. The code examples are contained in `.zip` files available from the following Web page:
`http://www.analog.com/en/embedded-processing-dsp/blackfin/content/blackfin_code_examples/fca.html`

The examples are grouped into the following categories: multi-rate filters, Fourier and discrete cosine function sets, convolution encoder sets, speech- and audio-related algorithms, image processing function sets, image analysis, audio/video, and so on.

To receive automatic notification by e-mail when any of these code examples are updated, register for `myAnalog.com` and select **Blackfin** as the "product category" and **Code Examples** as the "publication type".

Device Drivers and System Services

Powerful system services are available to applications through the system services library, which can be used to control the Blackfin processor's dynamic power management capabilities as well as control external asynchronous and synchronous memories, and manage interrupt processing. Applications can utilize the services of the DMA and callback services to easily schedule peripheral and memory DMA transfers, and defer non-critical, event-driven processing to a lower priority.

MULTI Integrated Development Environment

MULTI, from Green Hills Software, Inc., is a complete integrated development environment for embedded applications that use C, C++, and embedded C++. It runs on Windows, Linux, and UNIX hosts and supports remote debugging to a variety of target environments. MULTI

provides a direct graphical interface with all Green Hills Software compilers, and it supports multi-language development and debugging. MULTI contains all of the tools needed to complete a major programming project.

The MULTI tool chain is designed to support application development that has more microcontroller code than DSP code. The Green Hills compiler is optimized for control code.

Information on this development tool chain can be found on the Web at: http://www.ghs.com/products/blackfin_development.html

Open Source Software for Blackfin Processor

This section contains the following subsections:

- GNU Toolchain
- Linux and GNU Toolchain Help
- Eclipse IDE
- µClinux Distribution
- Blackfin µClinux
- Board Support Packages
- Daughter Cards
- GNU Toolchain

GNU Toolchain

The components of the GNU toolchain consist of:

- The GNU Binutils, which is a collection of binary tools, the main ones being as (the GNU assembler) and ld (the GNU linker). The mainline binutils project can be found on the GNU pages, where a comprehensive manual can be found.
- The GNU Compiler Collection (gcc), which includes front ends for C, C++, Fortran. The mainline gcc project can be found on the GNU pages, which also contain a comprehensive manual.
- The GNU Debugger (gdb), allows you to see what is occurring inside another program while it executes or what another program was doing when it crashed. The mainline project can be found on the GNU pages.
- The generation of µClinux's flat format — elf2flt
- Tools to support embedded file system generation for a variety of types. These include:
    - ext2 with genext2fs
    - cram with cramfs
- Tools to support bare metal application development and booting, called ldr-utils. These tools take standard gcc elf files, and convert them into a format that the Blackfin bootloader can interpret.
- Libraries, including libdsp, newlib, libgloss, and µClibc.
- Toolchain components that support the Canadian Cross Compiler. This means you no longer need to have a Linux host. You can develop bare metal applications, and Linux applications (not kernel) on a Microsoft Windows PC.

- JTAG tools: (both urjtag and gdbproxy) to program flash over JTAG, or debug a standalone application.
- Integrated Development Environments (IDE). The Blackfin GNU Toolchain plugs into many IDEs and graphical debuggers.

Linux and µClinux

µClinux stands for microcontroller Linux. (µ is the Greek letter mu denoting micro and C for controller.) The name µClinux normally refers to the complete distribution, and is not the name of the kernel. Similar to RedHat, Debian, Gentoo, or Damn Small Linux, µClinux is the name of the collection of userspace applications, userspace libraries, the system libraries, and the Linux kernel.

For more information about the difference between Linux and µClinux, visit this URL:
http://docs.blackfin.uclinux.org/doku.php?id=uclinux-dist:difference_from_linux

Linux and GNU Toolchain Help

The Blackfin Koop is supported by both an active open source community as well as a dedicated team from Analog Devices Inc. The URL is:
http://blackfin.uclinux.org/gf/

The Blackfin Koop provides support (including user assistance and defect correction) for the GNU Toolchain, Das U-Boot, the Linux Kernel, the µClinux Distribution and the schematics. These items can be found on this Web site:
http://blackfin.uclinux.org/

If you have a question, or think you have found a defect, please use the Help or Bugs links found on the home page.

Eclipse IDE

Eclipse is an integrated development environment (IDE) that provides support for managing projects, editing and debugging source code, and using external build tools. Eclipse can be downloaded from The Eclipse Foundation at:
http://eclipse.org/downloads

It is available for a variety of platforms including Windows, Linux, and Mac OS X.

Blackfin-specific plug ins can be found at
http://blackfin.uclinux.org/eclipse/

µClinux Distribution

Blackfin processors target embedded applications such as networking and internet appliances, automotive telematics, and portable devices. Many developers want more than just the processor and a software tool chain. To speed time to market, processor selection often hinges on operating system (OS) availability and existing software support.

µClinux is an open source OS that has been gaining significant attention and popularity over the past few years. There are several drivers for µClinux's expanding user base—source code availability, royalty-free licenses, reliability, open source community support, tools availability, networking support, portability, and an extensive application base.

To foster the sharing of this knowledge, the http://blackfin.uclinux.org/ Web site was launched in February, 2004. The site serves as a central repository for all µClinux Blackfin processor projects worldwide and hosts code examples, question and answer forums, and bug tracking. By creating an open source solution, embedded applications developers are able to leverage a wealth of knowledge and support from the open source community.

Blackfin µClinux

This section provides information about Blackfin support for µClinux. It also provides tables containing information about hardware and software support for µClinux projects.

Analog Devices Processors Supported for µClinux

µClinux has been ported and supports the following Analog Devices Processors:

- ADSP-BF522/3/4/5/6/7 (revision 0.1 or higher)
- ADSP-BF531/2/3 (revision 0.3 or higher)
- ADSP-BF534/6/7 (revision 0.2 or higher)
- ADSP-BF542/4/7/8/9 (revision 0.1 or higher)
- ADSP-BF561 (revision 0.3 or higher)

Latest Versions of Linux and Corresponding URLs

These are the approximate versions of Linux to date. Check out their corresponding URLs for the precise version numbers.

- Linux kernel: 2.6.x
  http://blackfin.uclinux.org/gf/project/uclinux-dist/frs
- Tool chain: gcc 4.x
  http://blackfin.uclinux.org/gf/project/toolchain/frs
- Das U-Boot: 1.x
  http://blackfin.uclinux.org/gf/project/u-boot/frs

µClinux Footprint

The default kernel is 500 Kbytes – 1 Mbytes

Recommended Flash Size

A workable image will fit in 4 Mbytes of flash memory (serial, NAND or parallel NOR).

Supported Debugging Tools

The following debugging tools are supported:

- GDB with simulation and JTAG support
- KGDB (for kernel and driver development)
- GDBSERVER (over ethernet or serial port)
- ICEBear USB ICE (for use with GBD). Visit this URL: http://www.section5.ch/icebear
- gnICE USB JTAG In-Circuit-Emulator. Visit this URL: http://www.bluetechnix.com/

Real-Time and General-Purpose Kernels

ADEOS has been ported to the Blackfin processor. ADEOS is a hardware abstraction layer allowing a real-time kernel and a general-purpose kernel to coexist. ADEOS supports the kinds of dual-OS Linux environments that are achieved using RTLinux or RTAI, without making use of the technology that is the subject of the RTLinux patent.

Linux Software Projects

Table 2-1 describes Linux software projects that work with Blackfin processors. For an enhanced version of this table that includes URLs for each project, visit:
http://docs.blackfin.uclinux.org/doku.php?id=projects

Table 2-1. Linux Software Projects

Name	Description
Arbitrary Waveform Generator	A simple arbitrary waveform generator – define a plot via a Web interface, generate data, and send it to a DAC.
Asterisk PBX	A complete PBX in software. uCasterisk is one part of a project to build a completely open telephony hardware platform.
QT GUI Library	A multi-platform C++ GUI toolkit created and maintained by Trolltech. It is enabled on Blackfin/µClinux.
Nano-X window system	An open source project aimed at bringing the features of modern graphical windowing environments to smaller devices and platforms. Nano-X allows applications to be built and tested on the Linux desktop, as well as cross-compiled for the target device.
Browsers	Two open source http text browsers are known to work on Blackfin/µClinux: links, and lynx. One is a graphic Web browser (Konqueror3) embedded. Included is documentation to download these applications, configure them for Blackfin/µClinux, and run them on the Blackfin processor.
LinPhone Voice over IP Phone	Use the console version of Linphone to make voice calls over the Internet.
Net Audio Player	Mount a Windows Share over the network, and play compressed audio files, controlled via a Web browser.
Networked Scope	A simple networked oscilloscope –capture data with a ADC, plot it with gnuplot, and pass it as a Web page with boa or thttpd.

Table 2-1. Linux Software Projects (Cont'd)

Name	Description
PocketSphinx	A version of the open source Sphinx-II speech recognition system which runs on handheld and embedded devices. This snapshot is now running under real time on the Blackfin/µClinux.
Adeos and Xenomai	Adeos provides a flexible environment for sharing hardware resources among multiple operating systems, or among multiple instances of a single OS. Xenomai is a real-time development framework cooperating with the Linux kernel. It provides real-time support to user-space applications, seamlessly integrated into the GNU/Linux environment. Xenomai is based on Adeos.
kaffe	A clean room implementation of the Java virtual machine, plus the associated class libraries needed to provide a Java run-time environment.
xmame/xmess	Ports of MAME, the multiple arcade machine emulator and MESS, the multi-emulator super system.
BlueZ	An implementation of the Bluetooth™ wireless standards specifications for Linux. The code is licensed under the GNU general public license (GPL) and is now included in the Linux 2.4 and Linux 2.6 kernel series.
FFmpeg & vlc	FFmpeg is a very fast video and audio converter. It can also grab from a live audio/video source. On the Blackfin processor, we couple it with vlc (video LAN client) to make a free IP camera.

Board Support Packages

Existing ports for Blackfin processors can be downloaded at no cost from: http://blackfin.uclinux.org

The open source GNU tool chain has been ported to Blackfin processors and can also be downloaded from the same site.

The latest release can be downloaded from the SVN tree or from the files section of the "GNU tool chain" project.

The community of open source developers for the Blackfin processor has been growing quickly. To find active development communities go to http://blackfin.uclinux.org.

For more information, see "µClinux Distribution" on page 2-15.

Daughter Cards

Several daughter cards developed for the ADI development boards are currently available. These cards provide features such as audio and video codecs, interfaces to standard connectors, and data acquisition capabilities. As the project expands, new daughter cards will continue to become available so check here often:
http://docs.blackfin.uclinux.org/doku.php?id=buy_stuff

Linux Hardware Projects

Table 2-2 describes Linux hardware projects that work with the Blackfin processor. For an enhanced version of this table that includes URLs for each project, visit the URL below. Note that this enhanced table is on the same page as the Linux software projects table.
http://docs.blackfin.uclinux.org/doku.php?id=projects

Table 2-2. Linux Hardware Projects

Name	Description
CF / IDE / NAND card	Multifunction interface cards, which includes CompactFlash (attribute memory, common memory, TRUE IDE MODE, PC Card I/O); IDE for hard drive and CD-ROM; and NAND flash
AD7476A card	This implements an A/D converter with (AC or DC input) a 2-MHz anti-aliasing filter, connecting to the serial peripheral interface (SPI) connector on the STAMP board.
AD1836A card	The first audio card is an AD1836A - 6 analog channels of output, 4 analog channels of input, and SPDIF in/out.

Table 2-2. Linux Hardware Projects (Cont'd)

Name	Description
AD73311L card	This audio card has an AD73311 that provides one 16-bit input and one 16-bit output.
AD5443 card	This implements a D/A converter connecting to the serial peripheral interface (SPI) connector on the STAMP board.
USB card	This card features two different USB host/device/OTG controllers – ISP1362 and SL811HS for Blackfin STAMP and EZ-KIT Lites.
TWI cards	These TWI (aka I2C) cards provide ease of connectivity to all kinds of low-speed peripherals such as LCD character displays (HD44780), keypad matrices, LEDs, and so on for Blackfin STAMP cards and ADSP-BF537 EZ-KIT Lites.
TFT LCD card	An introduction on how to use SHARP TFT LCD in µClinux for Blackfin ADSP-BF537 STAMP boards.

Summary: Software Development Tools

Table 2-3 compares available Blackfin processor development tools suites.

Table 2-3. Summary of Software Development Tools

Function	VisualDSP++	MULTI	GNU Compiler Collection
C/C++ compiler	YES	YES	YES
C run-time libraries	YES	YES	YES
C DSP run-time libraries	YES	YES	YES
Assembler, linker, loader	YES	YES	YES
IDDE	YES	YES	YES (w/Eclipse)
Project management	YES	YES	YES (w/Eclipse)

Table 2-3. Summary of Software Development Tools (Cont'd)

Function	VisualDSP++	MULTI	GNU Compiler Collection
Simulation support	YES	YES	YES
JTAG emulation support	YES	YES	YES

Examples Included With VisualDSP++

VisualDSP++ includes scores of examples built for Blackfin processors. Folders contain programs for signal processing, overlays, scripting, VDK, BTC, and more. Other folders provide example programs that run on EZ-KIT Lite evaluation systems.

The programs help you learn about processor core and peripherals, audio effects, signal processing, video and graphics, kernel and operating systems, and automation and scripting.

Software Modules

Analog Devices has a wide range of tested and optimized software modules, including decoders, encoders, codecs and other algorithms that provide multimedia functions for the Blackfin family. The software modules allow engineers to quickly and easily incorporate these functions, providing a faster development path to the end product. In addition, the highly-optimized software modules feature a consistent API and framework to ensure rapid development of multiple functions.

Selecting Hardware Development Tools

Users acquire a *hardware tool* to begin testing the application on a Blackfin processor. Development boards typically provide expansion headers, allowing you to prototype basic hardware without customized user hardware.

Hardware development tools include development and evaluation boards (such as EZ-KIT Lite or STAMP), expansion boards, and JTAG emulators.

EZ-KIT Lite Evaluation Systems

Typically, development and evaluation boards are standalone printed circuit boards (PCBs) that contain a Blackfin processor with other devices.

Analog Devices offers an evaluation system, called an EZ-KIT Lite, for each series of Blackfin processors. Each EZ-KIT Lite includes a board, cable, power supply, documentation, software, and a license key.

The EZ-KIT Lite board is a low-cost hardware platform that includes a Blackfin processor surrounded by several other devices such as audio codecs, video encoders, video decoders, flash, SDRAM, and so on.

Each EZ-KIT Lite board also includes an on-board JTAG emulator with a USB 2.0 connector and a standard 13-pin, 100-mil, JTAG header for use with high-performance JTAG emulators available from Analog Devices. Via the processor's JTAG port and the VisualDSP++ software, you can set breakpoints, single-step through code, view memory, fill/dump memory, perform real-time data manipulation, profile execution and memory access, plot data, and use standard I/O.

EZ-KIT Lite evaluation systems include a serial number, that when registered, yields full VisualDSP++ license status for 90 days from the date of installation. After 90 days, the license changes to restricted status, which limits the size of the application that can be built and supports debug

agent connectivity only. Refer to "Selecting Software Development Tools" to see where the EZ-KIT Lite fits into the phases of program development.

Most EZ-KIT Lite boards include three expansion connectors configured in the shape of a "U". Several third-party expansion boards connect to the EZ-KIT Lite board via these connectors. See "EZ-KIT Lite Expansion Boards" on page 2-42 for details.

The following sections briefly describe EZ-Board and EZ-KIT Lite development systems that are currently available for Blackfin processors.

ADSP-BF526 EZ-Board From Analog Devices

Part Number: ADZS-BF526-EZBRD

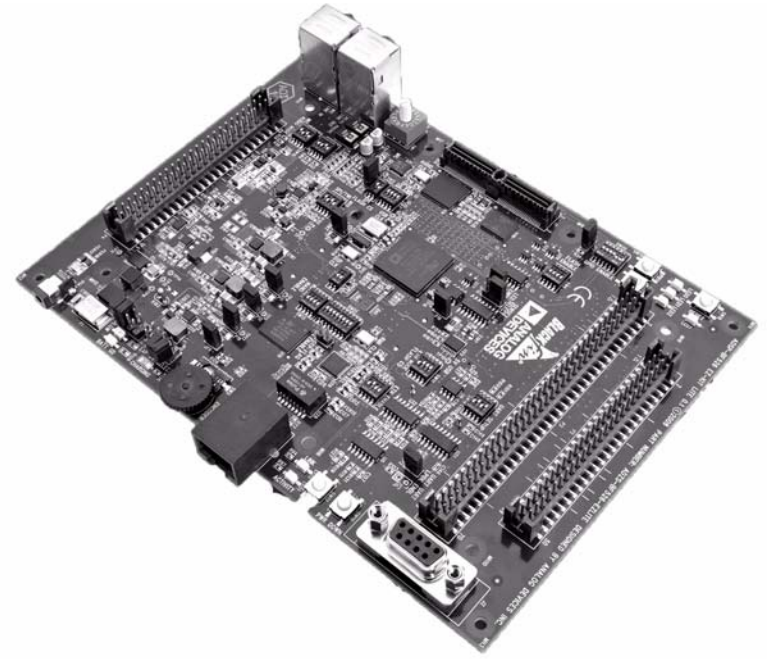


Figure 2-2. ADSP-BF526 EZ-Board Evaluation System

The Blackfin ADSP-BF526 EZ-Board evaluation system, as shown in Figure 2-2, provides developers with a low-cost platform for initial evaluation of the BF522/BF524/BF526 Blackfin processors via an external emulator, standalone debug agent board, or uClinux®.

This board is not equipped with a JTAG debug interface. To debug, you must have a Debug Agent board or emulator. The ADSP-BF526 EZ-Board has an expansion interface that allows for modularity with different EZ-Extender boards.

This evaluation system includes an ADSP-BF526 Blackfin processor desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a USB-based PC-hosted tool set. With this board, you can learn more about Analog Devices ADSP-BF526 Blackfin processor hardware and software development and prototype applications. The EZ-Board provides an evaluation suite of the VisualDSP++ integrated development and debug environment (IDDE) with the C/C++ compiler, advanced plotting tools, statistical profiling, and the VisualDSP++ kernel (VDK). Other features include: assembler, linker, libraries, loader, and splitter. VisualDSP++ offers programmers a powerful programming tool with flexibility that shortens time to market.

Features

- ADSP-BF526: 208-ball BGA, 400 MHz, 17mmX17mm/0.8 pitch
- SDRAM: Mobole SDRAM 1.8 V, 64 MB, 32M x 16, VFBGA 54-ball, Micron MT48H32M16LFCJ-75
- Flash: 4 MB (2M x 16), Numonyx M58WR032KB 1.8 V, VFBGA56
- NAND Flash: 2 Gb 1.8 V, 256Mb x 8, TFBGA63, Numonyx NAND02G-B2C 1.8 V
- SPI Flash: 4 Mb SST 1.8 V, SST25WF040
- Audio Codec: ADI SSM2602 1.8 V low-power audio codec
- Power Analysis Interface: Sense resistors to measure VDDINT, VDDEXT, VDDMEM, SDRAM
- Ethernet PHY: SMSC (RMII) 3.3 V with internal 1.8 V regulator, LAN8700
- Battery Charger: ADP2291, 1.5A linear charger, single cell LI
- Battery: Lithium ION, 740mAh, Ultralife UBBP005

- Thumbwheel: Panasonic, Rotary Encoder, 2-Bit Binary, EVQ-WKA001
- Connectors: USB OTG, Ethernet, HOST, EBIU Expansion, Group 1 Expansion, Group 2 Expansion, Group 3 Expansion
- Fuel Gauge: Benchmarq (TI), I2C interface BQ2750
- UART: ADM1385 RS-232 line driver/receiver 3.3 V, DB9 female connector
- LEDs - 9 LEDs: 1 board reset (red), 3 general-purpose (amber), 3 Battery status, 2 Ethernet (amber)
- Push Buttons: 5 push buttons w/ debounce logic: 1 reset, 2 programmable flag, 1 wake and 1 power down
- Connectors: USB OTG, Ethernet, Host, EBIU Expansion, Group 1 Expansion, Group 2 Expansion, Group 3 Expansion, land grid array
- JTAG ICE 14-pin header, USB cable, Ethernet cable
- Power supply, CE compliant external power supply (US or European)
- µClinux distribution CD

ADSP-BF527 EZ-KIT Lite From Analog Devices

Part Number: ADZS-BF527 EZ-KIT

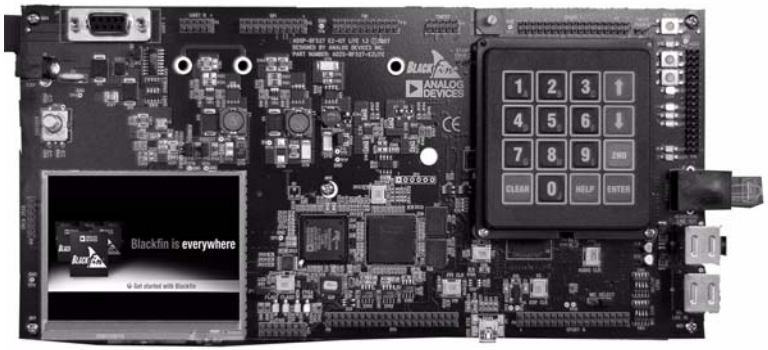


Figure 2-3. ADSP-BF527 EZ-KIT Lite Evaluation System

The ADSP-BF527 EZ-KIT Lite, as shown in Figure 2-3, is a low-cost evaluation platform for the Analog Devices ADSP-BF527 embedded processor, the VisualDSP++ development tools and associated application software.

This evaluation platform satisfies the needs of portable handheld vertical requirements. All of the STAMP interfaces are fully supported on this EZ-KIT Lite platform.

The evaluation board ships with a landscape, low-power QVGA touch-screen LCD panel. Also included are a set of stereo headphones and the necessary supplemental cables (USB, ethernet, and so on) required to run the VisualDSP++ examples programs.

All versions of ADSP-BF523, ADSP-BF525, and ADSP-BF527 Blackfin processors, which are pin-compatible, have similar memory maps. Software development for any of these devices can be performed on the ADSP-BF527 EZ-KIT Lite evaluation system.

Features

- ADSP-BF527 Blackfin processor
- 64 Mbytes SDRAM (32 M x 16 bits)
- Flash memory (4 Mbytes [2 M x 16 bits]; 2 Gbytes NAND; 16 Mbytes SPI)
- USB-based debugger interface
- JTAG ICE 14-pin header
- SPORT0 connector
- Evaluation suite of VisualDSP++
- 13 LEDs: 1 power (green), 1 board reset (red), 8 general-purpose (amber), 1 USB monitor (amber), 2 ethernet (amber)
- CE certified
- 3 push buttons with one reset
- 2 programmable flags
- µClinux distribution CD

ADSP-BF548 EZ-KIT Lite From Analog Devices

Part Number: ADZS-BF548 EZ-KIT

Figure 2-4. ADSP-BF548 EZ-KIT Lite Evaluation System

The ADSP-BF548 EZ-KIT Lite evaluation system, as shown in Figure 2-4, is a low-cost platform for the ADSP-BF548 Blackfin processor. This processor includes an 8x8 keypad interface, optical thumbwheel interface, ATA/ATAPI-6 interface, and an SD/SDIO interface. The ADSP-BF548 EZ-KIT Lite includes a QVGA touch screen LCD and a 40-Gbyte hard drive.

ADSP-BF542, ADSP-BF544, ADSP-BF547, ADSP-BF548, and ADSP-BF549 Blackfin processors, which are pin-compatible, have similar memory maps. Software development for any of these devices can be performed on the ADSP-BF548 EZ-KIT Lite evaluation system.

Features

- ADSP-BF548 Blackfin processor
- 64 Mbytes SDRAM (8 M x 16 bits)
- Flash memory (32 Mbytes burst, 2 Gbytes NAND, 16 Mbit SPI)
- USB-based debugger interface
- JTAG ICE 14-pin header
- SPORT0 connector
- Evaluation suite of VisualDSP++
- 10 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 6 general-purpose (amber), and 1 USB monitor (amber)
- CE certified
- Hard drive: 40 Gbytes 2.5 inch 5 V drive
- 5 push buttons with one reset
- 4 programmable flags
- µClinux distribution CD

ADSP-BF538F EZ-KIT Lite From Analog Devices

Part Number: ADZS-BF538F-EZLITE

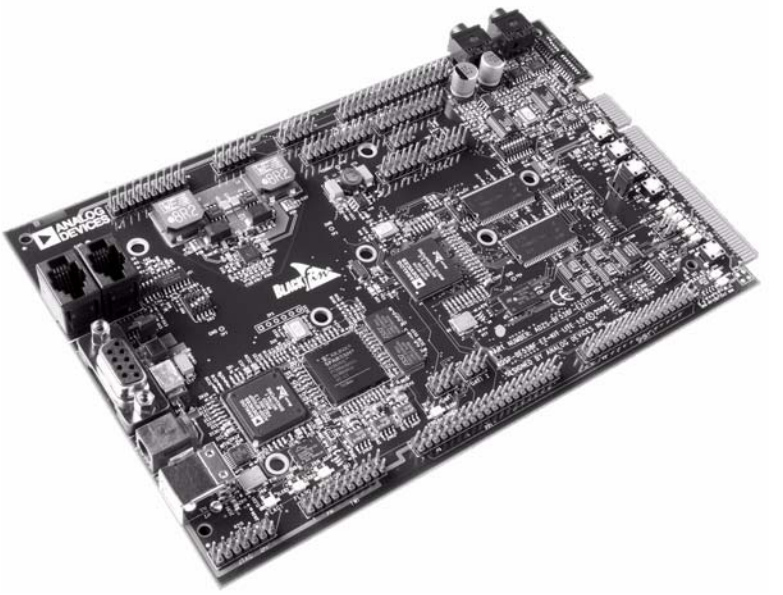


Figure 2-5. ADSP-BF538F EZ-KIT Lite Evaluation System

The ADSP-BF538F EZ-KIT Lite evaluation system, as shown in Figure 2-5, provides developers with a cost-effective method for initial evaluation of ADSP-BF538F Blackfin processors via a USB-based, PC-hosted tool set. With this EZ-KIT Lite, users can learn more about the Analog Devices (ADI) ADSP-BF538F hardware and software development, and quickly prototype a wide range of applications.

The EZ-KIT Lite includes an ADSP-BF538F Blackfin processor desktop evaluation board along with an evaluation suite of the VisualDSP++ development and debugging environment, including the C/C++ compiler, assembler, and linker. The evaluation suite of VisualDSP++ is designed to be used with the EZ-KIT Lite only.

Additionally, the ADSP-BF538F EZ-KIT Lite contains the National Instruments Educational Laboratory Virtual Instrumentation Suite (ELVIS) interface. This interface allows using the DC voltage and current measurement modules, oscilloscope and bode analyzer modules, function generator, arbitrary waveform generator and digital I/O.

Note that the ELVIS interface is also available on ADSP-BF537 EZ-KIT Lite.

Features

- Analog Devices ADSP-BF538F processor
  - Core performance up to 600 MHz
  - External bus performance to 133 MHz
  - 182-pin mini-BGA package
  - 25 MHz crystal
- Synchronous dynamic random access memory (SDRAM)
  - MT48LC32M8 – 64 MB (8M x 8-bits x 4 banks) x 2 chips
- Flash memory
  - 4MB (2M x 16-bits)
- Analog audio interface
  - AD1871 96 kHz analog-to-digital codec (ADC)
  - AD1854 96 kHz digital-to-audio codec (DAC)

- 1 input stereo jack
- 1 output stereo jack

- Controller Area Network (CAN) interface
  - Philips TJA1041 high-speed CAN transceiver
- National Instruments Educational Laboratory Virtual Instrumentation Suite (ELVIS) interface
  - LabVIEW™-based virtual instruments
  - Multifunction data acquisition device
  - Bench-top workstation and prototype board
- Universal asynchronous receiver/transmitter (UART)
  - ADM3202 RS-232 line driver/receiver
  - DB9 female connector
- LEDs
  - 10 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 5 general-purpose (amber), and 1 USB monitor (amber)
- Push buttons
  - 5 push buttons: 1 reset, 4 programmable flags with debounce logic
- Expansion interface
  - All processor signals
- Other features
  - JTAG ICE 14-pin header
  - µClinux distribution CD

ADSP-BF537 EZ-KIT Lite From Analog Devices

Part Number: ADZS-BF537-EZLITE

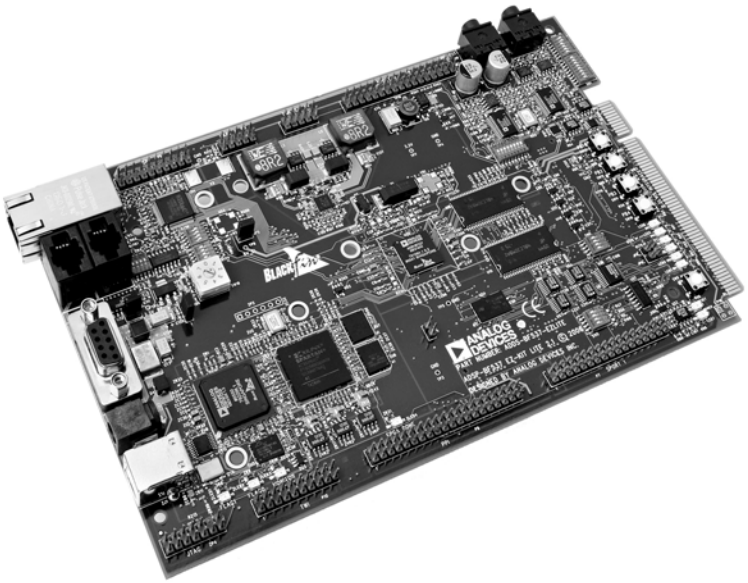


Figure 2-6. ADSP-BF537 EZ-KIT Lite Evaluation System

The ADSP-BF537 EZ-KIT Lite evaluation system, as shown in Figure 2-6, provides developers with a cost-effective method for initial evaluation of the ADSP-BF537 Blackfin processor. The EZ-KIT Lite includes an ADSP-BF537 Blackfin processor desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a USB-based PC-hosted tool set. With this EZ-KIT Lite, users can learn more about ADSP-BF537 Blackfin processor hardware and software development and prototype applications. The ADSP-BF537 EZ-KIT Lite provides an evaluation suite of the VisualDSP++ development environment with the C/C++ compiler, assembler, loader, and linker. All software tools are limited to use with the EZ-KIT Lite.

Features

- ADSP-BF537 Blackfin processor
- 64 Mbytes SDRAM (8 M x 8 bits x 4 banks) x 2 chips
- 4 Mbytes (2 M x 16 bits) flash memory
- AD1854 96 kHz digital-to-audio codec (DAC)
- Philips TJA1041 high-speed CAN transceiver
- USB-based debugger interface
- JTAG ICE 14-pin header
- SPORT0 connector
- Evaluation suite of VisualDSP++
- 10 LEDs: 1 power, 1 board reset, 1 USB reset, 1 USB monitor, and 6 general-purpose
- CE certified
- Standalone operation
- 4 programmable flags
- µClinux distribution CD

The ADSP-BF537 EZ-KIT Lite is also used for evaluation of the ADSP-BF536 and ADSP-BF534 Blackfin processors.

ADSP-BF561 EZ-KIT Lite From Analog Devices

Part Number: ADZS-BF561-EZLITE

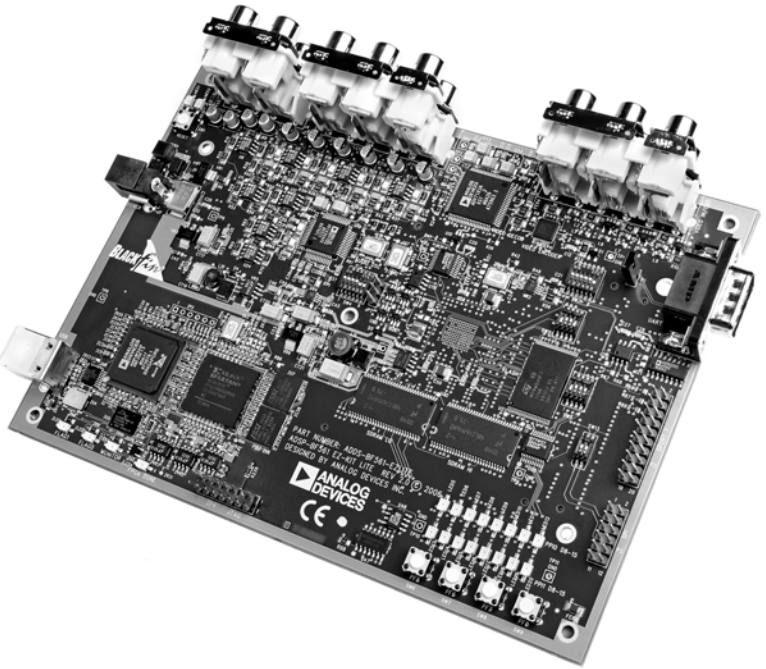


Figure 2-7. ADSP-BF561 EZ-KIT Lite Evaluation System

The ADSP-BF561 EZ-KIT Lite, as shown in Figure 2-7, provides a cost-effective method for initial evaluation of the ADSP-BF561 Blackfin processor for audio and video applications via a USB-based, PC-hosted tool set. Evaluation of analog audio applications is achieved by using the on-board AD1836 multichannel 96-kHz audio codec. By utilizing the on-board ADV7183A advanced 10-bit video decoder and ADV7179 chip-scale NTSC/PAL video encoder, you can evaluate video applications such as simultaneous input and output video processing enabled by the

dual-core architecture of the ADSP-BF561 Blackfin processor. Use this development system to learn more about ADSP-BF561Blackfin processor hardware and software development and to quickly prototype applications.

The EZ-KIT Lite includes an ADSP-BF561 Blackfin processor desktop evaluation board along with an evaluation suite of the VisualDSP++ development and debugging environment with the C/C++ compiler, assembler, loader, and linker. It also includes sample processor application programs, a CE-approved power supply, and a USB cable.

Features

- ADSP-BF561 Blackfin processor
- 64 Mbytes (16 M x 16 bits x 2 chips) SDRAM
- 8 Mbytes (4 M x 16 bits) flash memory
- AD1836 A – Analog Devices 96-kHz audio codec
- 5 push buttons with debounce logic: 1 reset and 4 programmable flags
- USB-based debugger interface
- JTAG ICE 14-pin header
- SPORT0 connector
- Evaluation suite of VisualDSP++
- 20 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 16 general-purpose (amber), and 1 USB monitor (amber)
- CE certified
- Standalone operation
- µClinux distribution CD

ADSP-BF533 EZ-KIT Lite From Analog Devices

Part Number: ADZS-BF533-EZLITE

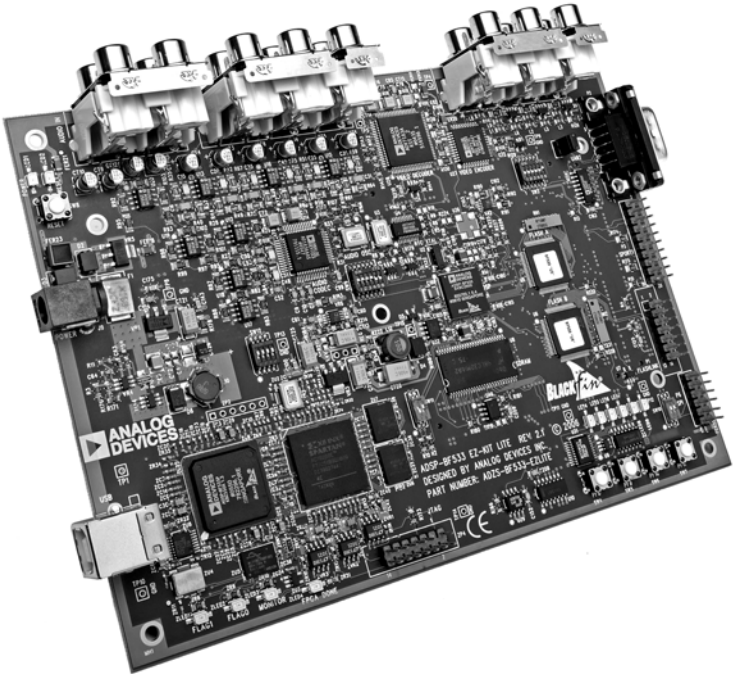


Figure 2-8. ADSP-BF533 EZ-KIT Lite Evaluation System

The ADSP-BF533 EZ-KIT Lite evaluation system, as shown in Figure 2-8, provides developers with a cost-effective method for initial evaluation of the ADSP-BF533 Blackfin processor for a wide range of applications including audio and video processing.

This evaluation system includes an ADSP-BF533 Blackfin processor desktop evaluation board and fundamental debugging software to facilitate architecture evaluations by using a USB-based PC-hosted tool set. With

this EZ-KIT Lite, you can learn more about Analog Devices ADSP-BF533 Blackfin processor hardware and software development and prototype applications. The EZ-KIT Lite provides an evaluation suite of the VisualDSP++ integrated development and debug environment (IDDE) with the C/C++ compiler, advanced plotting tools, statistical profiling, and the VisualDSP++ kernel (VDK). Other features include: assembler, linker, libraries, loader, and splitter. VisualDSP++ offers programmers a powerful programming tool with flexibility that shortens time to market.

Features

- ADSP-BF533 Blackfin processor
- 32 Mbytes (16 M x 16 bits) SDRAM
- 2 Mbytes (512 Kbytes x 16 bits x 2) flash memory
- AD1836 96-kHz audio codec with 4 input and 6 output RCA jacks (24 bits)
- ADV7183 video decoder with 3 input RCA jacks
- ADV7171 video encoder with 3 output RCA jacks
- ADM3202 RS-232 line driver/receiver
- DB9 male connector
- USB-based debugger interface
- JTAG ICE 14-pin header
- SPORT0 connector
- Evaluation suite of VisualDSP++
- 10 LEDs: 1 power, 1 board reset, 1 USB reset, 1 USB monitor, and 6 general-purpose
- 5 push buttons with debounce logic: 1 reset, 4 programmable flags

- Three 90-pin connectors providing PPI, SPI, EBIU, timers 0-2, UART, programmable flags, SPORT0, and SPORT1 expansion interfaces for analyzing and interfacing
- CE certified
- Standalone operation

The ADSP-BF531, ADSP-BF532, and ADSP-BF533 Blackfin processors, which are pin-compatible, have similar memory maps. (The ADSP-BF532 is a memory subset of the ADSP-BF533, and the ADSP-BF531 is a memory subset of the ADSP-BF532.) Software development for any of these devices can be performed on the ADSP-BF533 Blackfin processor. Thus, this EZ-KIT Lite evaluation system may be used for any of these devices.

EZ-KIT Lite Expansion Boards

EZ-KIT Lite expansion boards enhance and extend EZ-KIT Lite features and functionalities. The following EZ-KIT Lite expansion boards are currently available.

Blackfin EZ-Extender

Part Number: ADZS-BF-EZEXT-1

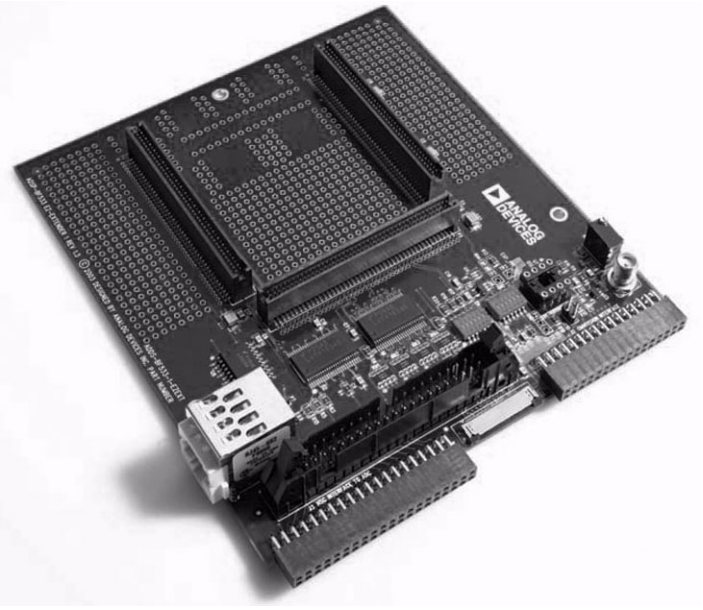


Figure 2-9. Blackfin EZ-Extender

The Blackfin EZ-Extender, as shown in Figure 2-9, is a separately sold assembly that plugs into an ADSP-BF533 EZ-KIT Lite evaluation system's expansion interface.

The board extends the capabilities of the EZ-KIT Lite evaluation system by providing a connection between the parallel peripheral interface (PPI) of the ADSP-BF533 EZ-KIT Lite, an Analog Devices high-speed converter (HSC) evaluation board, an OmniVision camera evaluation board, and an LCD display device. Moreover, the extender broadens the range of EZ-KIT Lite applications by providing surface-mounted (SMT) footprints for breadboard capabilities and access to all pins on the EZ-KIT Lite board's expansion interface.

The Blackfin EZ-Extender features include:

- OmniVision camera interface
- High-speed converter (HSC) evaluation board interface
- LCD interface
- SMT footprint area

Blackfin USB-LAN EZ-Extender Board

Part Number: ADZS-USBLAN-EZEXT

Figure 2-10. Blackfin USB-LAN EZ-Extender Board

The Blackfin USB-LAN EZ-Extender board, as shown in Figure 2-10, provides a solution for users to evaluate different peripherals on ADSP-BF533 and ADSP-BF537 Blackfin processors. The EZ-Extender connects to ADSP-BF533 EZ-KIT Lite or ADSP-BF537 EZ-KIT Lite evaluation systems.

The card includes peripherals that support USB 2.0 and ethernet. The card also supports USB bus power and includes a µClinux distribution CD. The components for bus power on the ADZS-USBLAN-EZEXT card are not populated during shipping. For bus power to work, the card must be connected to an EZ-KIT Lite evaluation system that also supports USB bus power. Currently, the ADSP-BF561 EZ-KIT Lite and the ADSP-BF533 EZ-KIT Lite do not support USB bus power.

The Blackfin USB-LAN EZ-Extender card is a small (approximately 4.5" x 3.5") printed circuit board that connects directly to an EZ-KIT Lite board. The card includes the hardware, USB cable, USB software, and ethernet software to begin evaluating the card immediately. Power is derived by plugging the card into the EZ-KIT Lite board.

Blackfin FPGA EZ-Extender Daughter Board

Part Number: ADZS-BFFPGA-EZEXT

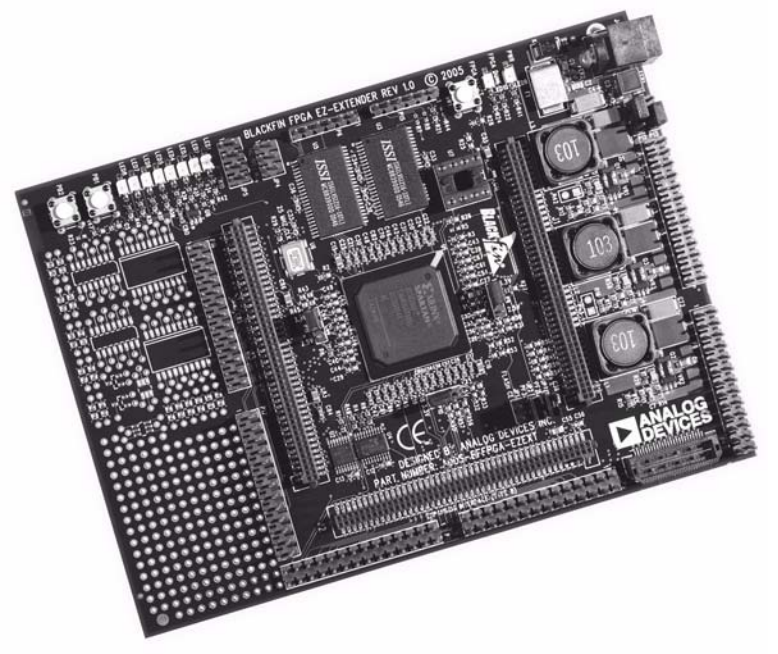


Figure 2-11. Blackfin FPGA EZ-Extender Daughter Board

The Blackfin FPGA EZ-Extender daughter board, as shown in Figure 2-11, aids the design and prototype phases of ADSP-BF533, ADSP-BF537, or ADSP-BF561 processor-targeted applications. The EZ-Extender connects to the ADSP-BF527 EZ-KIT Lite, ADSP-BF533 EZ-KIT Lite, ADSP-BF537 EZ-KIT Lite, and the ADSP-BF548 EZ-KIT Lite. The board extends the evaluation system by providing a Xilinx FPGA with external memory, IDC connectors for off-board connections,

and a small breadboard area. Applications and information about the use and connection of the various interfaces on the Blackfin FPGA EZ-Extender are available from Analog Devices.

The Blackfin Landscape FPGA EZ-Extender features:

- µClinux distribution CD
- Xilinx Spartan III Field-Programmable Gate Array
  - XC3S1000
  - FG456 package
- Asynchronous static random access memory (SRAM)
  - Directly connected to FPGA
  - 2 MB (512K x 16 bits x 2 chips)
  - TSOP44 package
- 25 MHz oscillator
  - Directly connected to global clock of FPGA
- Socket for auxiliary oscillator
  - Directly connected to global clock of FPGA
- IDC through-hole connectors
  - Allows quick access to Blackfin and FPGA pins for probing
  - Allows access to Blackfin and FPGA pins for off-board connections
- High-speed connector
  - Allows access to Blackfin and FPGA pins for high-speed application

- Expansion interface connectors
  - Allows access to Analog Devices family of Blackfin EZ-Extenders
- 2 push buttons
  - Directly connected to FPGA
  - 1 with external debounce circuitry and 1 without
- 8 flag LEDs
  - Directly connected to FPGA

Blackfin Landscape LCD EZ-Extender Daughter Board

Part Number: ADZS-BFLLCD-EZEXT

The Blackfin Landscape LCD EZ-Extender daughter board extends the capabilities of the EZ-KIT Lite by allowing you to connect to a landscape LCD on Blackfin ADSP-BF52x, ADSP-BF53x, and ADSP-BF54x processors. The Landscape LCD EZ-Extender connects to the ADSP-BF526 EZ-KIT Lite, ADSP-BF537 EZ-KIT Lite, ADSP-BF538 EZ-KIT Lite, and the ADSP-BF548 EZ-KIT Lite evaluation systems.

The Landscape LCD EZ-Extender supports a 3.5" landscape QVGA (320x240) display from SHARP. This LCD display can operate at VDDIO from 1.6 V to 3.6 V, allowing this LCD to be a good fit for normal use as well as for low-power applications. The Analog Devices AD7879 is used as the low-cost touchscreen controller for the LCD display. The AD7879 on the Landscape LCD EZ-Extender is a small 16-pin LFCSP package and is ideal for low-power applications.

The Landscape LCD EZ-Extender also has an Analog Devices AD7147-1 programmable controller for compacitive touch sensors. The compacitive controller interfaces to the Blackfin processor via a simple TWI (two-wire interface). The other end of the controller interfaces to external capacitance sensors, implementing functions such as capacitive buttons and scroll wheel.

The following lists Blackfin Landscape LCD EZ-Extender interfaces.

- LCD display with touch capabilities:
  - Sharp LQ035Q1DH02 3.5-inch LCD with resistive touch
  - 320 (horizontal) x 240 (vertical) landscape
  - 1.8 V to 3.6 V I/O operation
  - LCD backlight

- LCD touch controller:
  - Analog Devices AD7879 touchscreen controller
  - 1.8 V to 3.3 V I/O operation
- Capacitive touch controller:
  - Analog Devices AD7147 capacitive touch controller
  - 4 push buttons and 1 scroll wheel
  - 1.8 V to 3.3 V I/O operation
- No power supply required: power is derived from the EZ-KIT Lite/EZ-Board
- µClinux distribution CD
- CE certified
- Dimensions: 3.75 in. (height) x 3.5 in. (width)

Blackfin Audio EZ-Extender Daughter Board

Part Number: ADZS-BFAUDIO-EZEXT

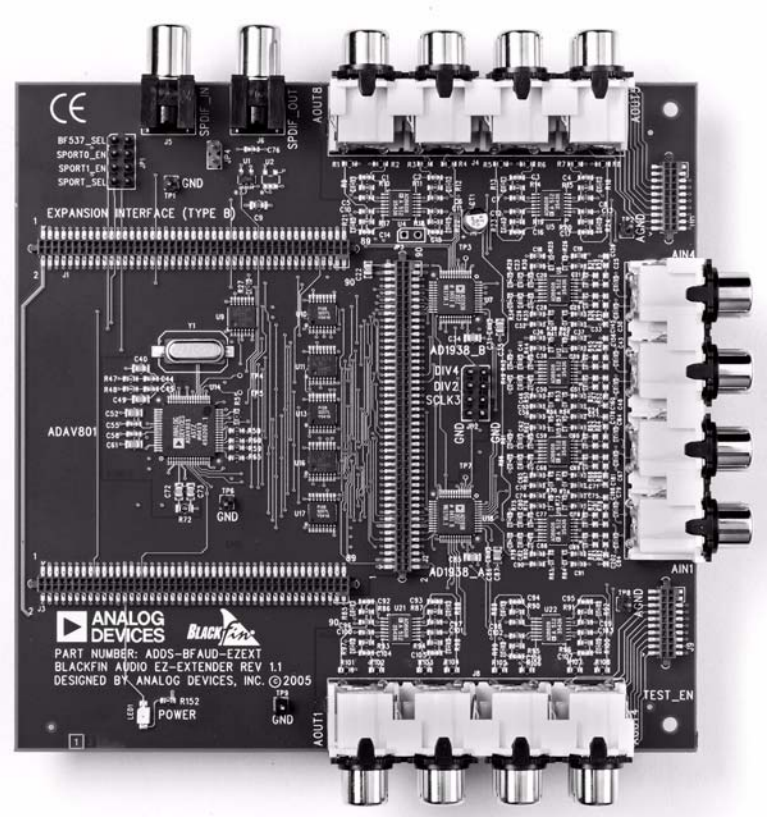


Figure 2-12. Audio EZ-Extender Daughter Board

The Blackfin Audio EZ-Extender daughter board, as shown in Figure 2-12, aids the design and prototype phases of ADSP-BF533 and ADSP-BF537 processor-targeted audio applications. The Audio EZ-Extender connects to the ADSP-BF533 EZ-KIT Lite and the

ADSP-BF537 EZ-KIT Lite evaluation systems. The board extends the capabilities of the evaluation system by providing a connection to thee audio codecs, including two analog audio codecs and one dual analog/digital audio codec with an interface to digital Sony Philips Digital Interface (SPDIF) audio. Applications and information about the use and connection of the various interfaces on the Blackfin Audio EZ-Extender are available from Analog Devices.

The following is a list of the Blackfin Audio EZ-Extender board interfaces.

- Analog audio interface
  - 2 AD1938 – Analog Devices 192-kHz audio codecs
  - 4 stereo analog audio inputs via RCA jacks
  - 8 stereo analog audio outputs via RCA jacks
- Digital audio interface
  - 1 ADAV801 – Analog Devices SPDIF transceiver with sample rate converter
  - 1 SPDIF input via a RCA jack
  - 1 SPDIF output via a RCA jack
- Expansion interface on both sides of the board for stacking other EZ-Extender boards

Blackfin A-V EZ-Extender Board

Part Number: ADZS-BFAV-EZEXT

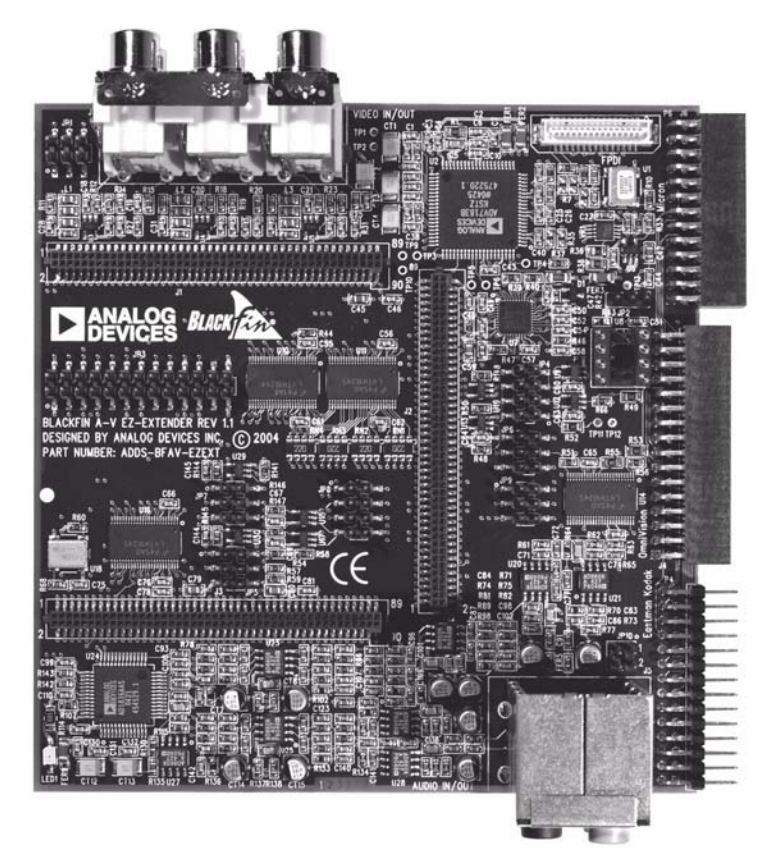


Figure 2-13. A-V EZ-Extender Board

The Blackfin A-V EZ-Extender board, as shown in Figure 2-13, provides a solution for users to evaluate audio and video peripherals and CMOS image sensors for the ADSP-BF533, ADSP-BF537, ADSP-BF538F, and

ADSP-BF561 Blackfin processors. The A-V EZ-Extender connects to the ADSP-BF527 EZ-KIT Lite, ADSP-BF533 EZ-KIT Lite, ADSP-BF537 EZ-KIT Lite, and the ADSP-BF548 EZ-KIT Lite.

The card includes peripherals that support video encoders, video decoders, and multichannel audio codecs. The card also supports connectivity to three different CMOS image sensors: Micron, Omnivision, and Kodak. The A-V EZ-Extender card is a compact board that connects directly to an EZ-KIT Lite board.

ADSP-BF537 STAMP Board Support Package (BSP)

Part Number: ADDS-BF537 STAMP

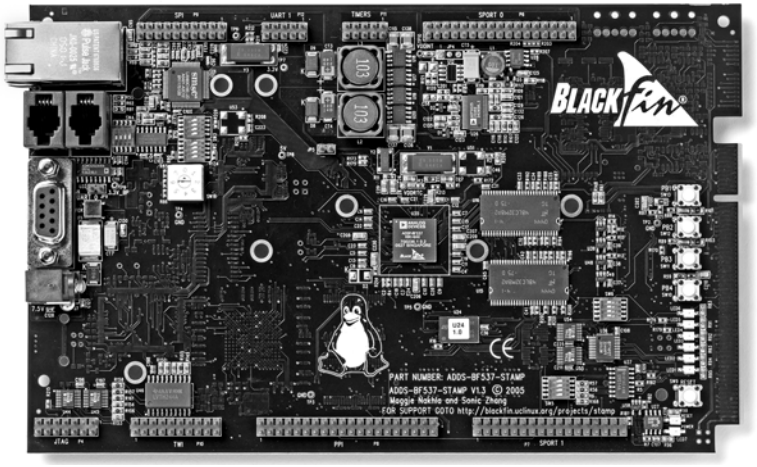


Figure 2-14. ADSP-BF537 STAMP Board

The ADSP-BF537 STAMP µClinux kernel board support package, as shown in Figure 2-14, provides a cost-effective environment to develop embedded systems around ADSP-BF537 Blackfin processors. The STAMP board connects to the ADSP-BF537 EZ-KIT Lite evaluation system. The STAMP board is specifically designed to support the development and porting of open source µClinux applications and includes the full complement of memory along with serial and network interfaces. A variety of available daughterboards plug into this board, adding interface functions such as audio, video, and analog input or output.

This product is not available for direct purchase from Analog Devices. For pricing, availability, and purchase information, contact your local Analog Devices distributor.

Besides an ADSP-BF537 500-MHz Blackfin processor, the board includes:

- 64 Mbytes SDRAM (64 M x 16 bits)
- 4 Mbytes flash memory
- Integrated ethernet MAC/PHY
- RS-232 serial interface
- I/O connectors for these Blackfin peripherals: PPI, SPORT0 and SPORT1, SPI, timers, IrDA, and two-wire interface
- JTAG interface for debug and flash programming
- 3 LEDs and 3 push buttons

Together with the ADSP-BF537 STAMP development board, the package includes a recent copy of the open source development tools (GCC 4.x) and the µClinux 2.6.x kernel. It also includes a CD with documentation and the board schematics, Gerbers, and layout files. The latest version of all the tools can be found on the http://blackfin.uclinux.org/ Web site. This Web site also hosts open source application projects based on the STAMP board and daughterboards (such as a networked audio media node), a networked oscilloscope, and a Blackfin XMAME game console.

Standalone Debug Agent Board

Part Number: ADZS-DBGAGENT-BRD

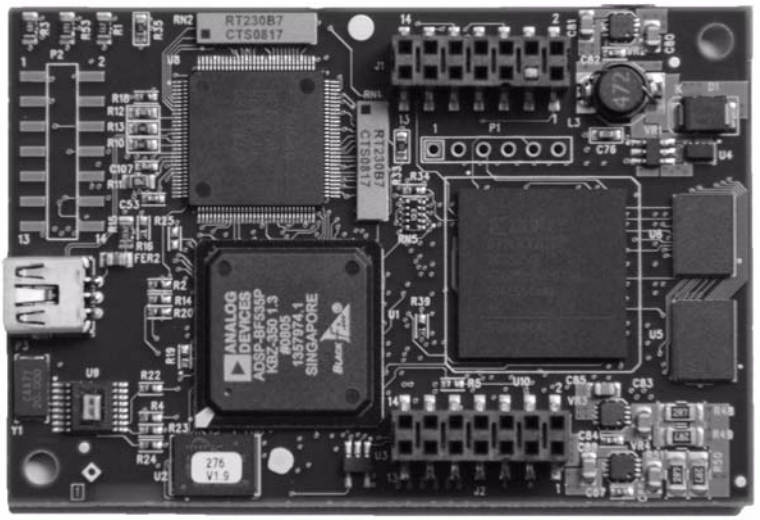


Figure 2-15. Standalone Debug Agent Board

The Standalone Debug Agent board, as shown in Figure 2-15, provides a modular low-cost emulation solution for EZ-Boards as well as evaluation boards designed by third parties. The Standalone Debug Agent is similar to the debug agent that is on existing EZ-KIT Lite evaluation systems, but it has the flexibility to be moved from one board to another.

The Standalone Debug Agent works only on EZ-Boards or approved third-party boards.

JTAG Emulators

JTAG (Joint Test Action Group) is defined by the IEEE 1149.1 standard for a test access port for testing electronic devices. This standard defines a method for serially scanning the I/O status of each pin on the device as well as controlling internal operation of the device.

Boundary-scan testing was developed in the mid 1980s as the JTAG interface to solve physical access problems on PCBs caused by increasingly crowded assemblies due to novel packaging technologies. Boundary-scan embeds test circuitry at chip level to form a complete board-level test protocol. With boundary-scan—industry standard IEEE 1149.1 since 1990—you can access the most complex assemblies for testing, debugging, in-system device programming, and diagnosing hardware problems.

Blackfin processors are equipped with a JTAG port and thus support the IEEE 1149.1 standard for system test.

Through the JTAG port, you can run and halt the processor remotely. The internal and external processor memory can be read or written, and breakpoints can be set.

Most development boards include some built-in JTAG emulation circuitry. Your own hardware, most likely, does not contain this circuitry.

High-Performance USB 2.0 JTAG Emulator

Part Number: ADZS-HPUSB-ICE

Figure 2-16. High-Performance USB 2.0 JTAG Emulator

The Analog Devices high-speed, high-performance, universal serial bus-based emulator (HP-USB), as shown in Figure 2-16, provides a portable, non-intrusive, target-based debugging solution for Analog Devices JTAG processors.

These easy-to-use USB-based emulators perform a wide range of emulation functions, including single-step and full-speed execution with predefined breakpoints, and viewing and/or altering of register and memory contents. With the ability to automatically detect and support multiple I/O voltages, the HP-USB emulator enables you to communicate with all of the Analog Devices JTAG processors using a full-speed USB 1.0 or high-speed USB 2.0 port on the host PC.

Applications and data can be tested and transferred easily (and rapidly, when the HP-USB emulator is connected to a high-speed USB 2.0 port on your host PC) between the emulators and the separately available VisualDSP++ development and debugging environment.

The plug-and-play architecture of USB allows the emulators to be detected automatically and configured by the host operating system. It can also be connected to (and disconnected from) the host without opening the PC or turning off the power to the PC. A 3-meter (9-foot) cable is included to connect the emulators to the host PC, providing abundant accessibility.

Features

- High-speed USB 2.0 (backward compatible with full-speed USB 1.0) interface and connector
- JTAG clock operation from 10 MHz to 50 MHz
- Support for all Analog Devices JTAG processors
- Multiple processor I/O voltage support with automatic detection
- 1.8 V, 2.5 V, and 3.3 V compliant and tolerant

- 5 V tolerant and 3.3 V compliant for 5 V processors
- Multiprocessor support
- 14-pin JTAG connector
- 3-meter USB cable for difficult-to-reach targets

USB-Based JTAG Emulator

Part Number: ADZS-USB-ICE

Figure 2-17. USB-Based 1.1 JTAG Emulator

The cost-effective universal serial bus (USB)-based 1.1 JTAG emulator, as shown in Figure 2-17, from Analog Devices provides a portable, non-intrusive, target-based debugging solution for Analog Devices JTAG processors.

This USB-based emulator performs a wide range of emulation functions, including single-step and full-speed execution with predefined breakpoints, and viewing and/or altering of register and memory contents. With the ability to automatically detect and support multiple I/O voltages, the USB emulator enables users to communicate with all of the Analog Devices JTAG processors using a USB 1.0 or high-speed USB 2.0 port on the host PC. Applications and data can easily be tested and transferred between the emulator and the separately available VisualDSP++ development and debugging environment.

The plug-and-play architecture of USB allows the emulators to be detected automatically and configured by the host operating system. The USB can also be connected to (and disconnected from) the host without opening the PC or turning off the power to the PC. A 3-meter (9-foot) cable is included to connect the emulators to the host PC, providing abundant accessibility.

Features

- Full-speed USB 1.1 compliant (forward compatible with high-speed USB 2.0 interface and connector)
- Support for all Analog Device JTAG processors
- Multiple processor I/O voltage support with automatic detection
- 1.8 V, 2.5 V, and 3.3 V compliant and tolerant
- 5 V tolerant and 3.3 V compliant for 5 V processors
- Multiprocessor support
- 14-pin JTAG connector
- 3-meter USB cable for difficult-to-reach targets

Third-Party Boards

PHYTEC phyCORE®-BF537 SBC

Ordering Information: See below

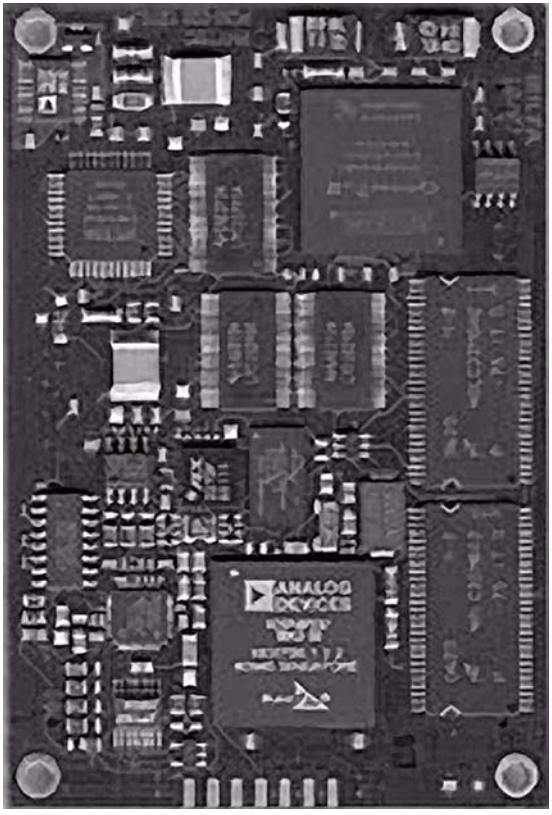


Figure 2-18. PHYTEC phyCORE® Single-Board Computer

The PHYTEC phyCORE-BF537, as shown in Figure 2-18, is an insert-ready, single-board-computer (SBC) subassembly in miniature dimensions, populated with an Analog Devices ADSP-BF537 Blackfin processor. Integrated chip peripherals include: 10/100 ethernet, CAN, PPI and TWI, SPI, UART interfaces, timers, and an RTC.

All applicable data/address lines and signals extend from the underlying logic devices on the phyCORE SBC to two high-density Molex SMT pin header connectors (pin width is 0.635 mm/25 mil) lining the circuit board edges. This enables the phyCORE-BF537 to be plugged like a “big chip” into target hardware.

Primary interfaces include a CAN bus and dual RS-232, as well as an SMSC LAN8700I 10/100BaseT Ethernet PHY and a PLX NET2272 USB transceiver.

The VisualDSP++ integrated development and debugging environment (IDDE) enables easy generation of code and on-board download of user programs to the phyCORE-BF537 target hardware when mounted on the phyCORE-BF537 carrier board.

Features

- Analog Devices ADSP-BF537 Blackfin processor
- 500 MHz core frequency with up to 1,000 MMACs
- Memory management unit (MMU)
- Memory and DMA controllers
- CAN controller
- 10/100 Mbit ethernet MAC
- 10/100 Mbit ethernet PHY
- High-speed USB 2.0 device controller

- PPI supporting ITU-R 656 video data formats
- I²C / 2x I²S
- SPI
- 2 UARTS (RS-232 or IrDA)
- RTC and watchdog timer
- 8-channel / 12-bit (200 kSPS [kilo samples per second]) ADC
- Altera FPGA device (max 8256 logic elements)
- Memory configuration:
    - 132 Kbytes internal memory
    - SDRAM: 16 to 128 Mbytes
    - NOR-flash: 1 to 4 Mbytes
    - I²C EEPROM: 32 K
- JTAG interface
- Single supply 3.3 V with on-board power management
- Module connector: 0.635 mm pitch, 2x 200-pin Molex
- Dimensions: 59 mm x 84 mm
- Extended temperature range (-20° to +85°C)

Rapid Development Kits

Each kit contains an SBC module mounted on an applicable carrier board that features hardware needed for immediate start-up of the module, as well as external break-out of applicable signals from the SBC. The

included PHYTEC Spectrum CD-ROM provides complete electronic documentation, demo programs, and evaluation software development tools.

This PHYTEC rapid development kit provides the necessary ingredients with which to jump-start an embedded design, reduce time-to-market, and move a concept to a prototype and then to finished product.

For ordering information, please visit PHYTEC at this address: http://www.phytec.com/

Selecting the Right Combination of Tools

Knowing which tools to use is critical to ensuring a quick development cycle. There are many options for software and hardware development tools. Two of the most common scenarios described in this section contain circumstances encountered by other developers along with recommended solutions. Your needs may be similar to one of the following scenarios.

Scenario 1

Question. *We are a small design house with one software engineer and one hardware engineer for this project. We cannot afford a substantial initial investment in tools. What do you recommend?*

Answer. Purchase an ADSP-BF533 EZ-KIT Lite evaluation system (p/n: ADZS-BF533-EZLITE).

This hardware platform allows you to begin software development. By interfacing components to the board's expansion headers, the platform can serve as the basis for a hardware prototype. The EZ-KIT Lite evaluation system includes VisualDSP++, but the software license restricts various capabilities (debug agent connectivity only and reduced program size allowance).

Obtain a test drive serial number on the Analog Devices Web site at:
http://www.analog.com/testdrive

When the test drive license expires, consider purchasing a full seat of VisualDSP++ (p/n: VDSP-BLKFN-PC-FULL).

After you have finished constructing your hardware, purchase a low-cost USB emulator (p/n: ADZS-USB-ICE) from Analog Devices.

Scenario 2

Question. *We have a team of seven software engineers who are developing code for the Blackfin processor, but no more than five are likely to be using the tools at any given time. How do we handle licensing? Does each engineer need a license?*

Answer. A floating license may be right for you. VisualDSP++ may be installed on many machines. A developer checks out a floating license from a license server onto any machine. With five floating licenses, up to five people can use VisualDSP++ at the same time.

Order a floating license (p/n: VDSP-BLKFN-PCFLOAT).

3 SUPPORT OPTIONS

As new information, such as data sheets, manuals, online Help, training, Web content, or automatic e-mail notifications are prepared/revised, Analog Devices makes them available to its customers and other interested parties. This chapter addresses the support options available for users during the evaluation process and after you have purchased a Blackfin processor.

This chapter lists the various types of support available to users and prospective users of Blackfin products.

Available Support

The Blackfin processor architecture provides many advanced features. As next-generation processors, these parts are becoming increasingly complex. With that in mind, Analog Devices provides a wide variety of support options in the form of online information, as well as in training. This wealth of information is available to aid evaluators of software/hardware solutions (at the beginning of the evaluation process), design engineers (while developing a system), or support engineers, while resolving compatibility and usability issues (after product release).

This chapter highlights some support, information, and training options available to Analog Devices users at any stage of development.

Since information about Analog Devices products changes and increases rapidly, Analog Devices makes this information readily available and encourages you to keep up to date with new developments, especially with our online options.

Analog Devices Web Site

Your first point of reference for the most recent information is always the Analog Devices Web site. The following kinds of information are available:

- "Processor and Tools Selection Information"
- "Getting Started Information"
- "Applications Notes, EE-Notes, and Other Articles"
- "Communities-Related Information"
- "Platform-Related Information"

Visit the Blackfin processor home page at
`http://www.analog.com/blackfin`

The Analog Devices Embedded Processing and DSP page, which offers access to other processor families, is located at:
`http://www.analog.com/processors`

To visit the knowledge base, use your browser to access:
`http://www.analog.com/processors/knowledgebase`

This information is available to all classes of users, Analog Devices customers, and interested parties.

Processor and Tools Selection Information

For processor-specific information start at the Web site's Blackfin processor page (http://www.analog.com/blackfin), and then check Blackfin processor offerings with regards to package, speed, or temperature specifications. Links provide access to additional processor selection information (such as peripherals and memory), tools selection information, and other materials.

Getting Started Information

The Blackfin processor page (http://www.analog.com/blackfin) provides links under the heading "Getting Started" that instruct you about Blackfin processor architecture and targeted applications. To find out about the processor's core and peripherals, refer to this Web site topic at the Analog Devices Web site. You may also want to check the benchmark data available from independent testers. (See "Benchmarks Against Other Processors" on page 1-33.) A link to training and events provides an up to date list of local training seminars and upcoming events where you can learn more about Blackfin processor products.

Applications Notes, EE-Notes, and Other Articles

Some of the most useful documents available are EE-Notes (engineer-to-engineer notes), sometimes called application notes. These documents provide detailed technical information about using Blackfin processors. Many of these documents include a `.ZIP` file with example code. These materials are available by download from the Analog Devices Web site.

These documents supplement the standard documentation for processors and tools. EE-Notes focus on a very narrow or specific topic. Articles are grouped under the headings "Processor-Specific", "Tools-Specific", and "Application Hints". Note that you can also use VisualDSP++ Help to search, locate, and view this collection of articles, as well as the entire list of EE-Notes.

Additional links are provided to recent articles, many of which have been featured in trade magazines. Please point your browser to the technical library:
http://www.analog.com/processors/technical_library

Communities-Related Information

For information about application-specific development types, refer to the "Communities" topic at the Blackfin processor Web site. Here you can find information about a particular application theme, such as automotive telematics or video/imaging. Visit the following sites:
http://blackfin.org/
http://blackfin.uclinux.org/

Visual Learning and Development (VLD) - On-Demand Video Tutorials

The Analog Devices Web site offers free on-demand video tutorials. Subjects include:

- Blackfin core architecture
- Basics of building a Blackfin application
- Interfacing Blackfin with audio and video peripherals
- Introduction to VDK
- Introduction to VisualDSP++ tools
- Multimedia starter kit
- Lockbox™ secure technology on Blackfin processors
- Blackfin optimizations for performance and power consumption
- Blackfin device drivers

- Blackfin system services
- Introduction to the National Instruments LabVIEW™embedded module for Blackfin processors
- Introduction to VisualAudio®
- Rapid development of a Blackfin-based video application
- Performance tuning on the Blackfin processor
- Programming and optimizing C code on Blackfin

Viewing these Blackfin online learning and development (BOLD) video tutorials requires a free one-time registration. Visit the following site: `http://www.analog.com/en/embedded-processing-dsp/content/blackfin_bold_training/fca.htmlblackfin.org/`

Platform-Related Information

When information about the Blackfin processor and its use with other hardware or software solutions becomes available, we refer to that as "Platform-Related Information." Refer to the "Platform-Related" topic for this information.

Workshops and Seminars

The most efficient way to learn about the Blackfin processor architecture is by attending a 3½-day (or 1-day) Blackfin seminar. A Blackfin seminar provides a mixture of lectures and demonstrations. The 3½-day workshop provides hands-on exercises and serves as an excellent starting point for both hardware and software development.

However, a variety of training options are available in both online and in a classroom setting. For users who prefer live training sessions, a variety of venues is available.

Blackfin Processor Workshops

Blackfin processor workshops are designed to develop a strong working knowledge of Analog Devices processors through lecture and hands-on exercises in a classroom setting.

These practical courses teach how to use the latest software development tools. First, the core elements of the processor, which includes the computational units, the data address generators, and the program sequencer, are examined along with the relevant assembly code instructions. A number of simulator labs help in understanding operation of the individual elements. Memory configuration (both internal and external) is discussed next. Advanced instructions are presented with a follow on lab session about code optimization. The I/O peripherals, which include the SPORTS, link ports, and external port, are discussed in detail along with DMA operation between these peripherals and internal memory.

Workshops are offered through Kaztek Engineering throughout the world. Visit the Kaztek Web site for the schedule of upcoming workshops and pricing information at:
http://www.kaztek.com/

Blackfin Processor Seminars

The Blackfin processor seminar is a subset of the Blackfin Processor Workshop slide set and does not include hands on exercises. A Blackfin seminar is often accompanied by tools and software demonstrations running on hardware (sometimes by key Analog Devices third-party partners).

Contact your local Analog Devices sales office or distribution partner for information on Blackfin seminars or refer to:
http://www.analog.com/processors/learning/index.html

TechOnLine Seminars

If you cannot attend a workshop or seminar, check online Blackfin seminars. To access these seminars go to http://www.techonline.com. select **Courses**, then search on **Blackfin**.

You can also request a copy of the Blackfin seminar and/or workshop material from Analog Devices. This includes all of the slides, associated notes, and exercises. Contact your local Analog Devices sales office for more information.

µClinux on the Blackfin Processor 3-Day Workshop

This course is an introduction to all aspects of programming with µClinux based on the Blackfin processor STAMP board. The course is presented by System Design and Consulting Services in various locations.

The course covers the following subjects: development tools, compiler, linker, Blackfin processor assembler and debugger, bootloader (U-boot), µClinux source distribution, µClinux libraries, Linux boot-up, Linux kernel 2.6.x, flash memory and flash file systems, introduction to device drivers, µClinux debugging, network applications, and example user applications.

Processor Documentation

Three documents accompany each Blackfin processor: a data sheet, a hardware reference, and a programming reference. These documents enable you to design software and hardware.

Blackfin Processor Manuals

Two kinds of manuals provide detailed information about the Blackfin processor: hardware reference manuals and a programming reference.

Hardware Reference Manuals

Each processor's hardware reference manual provides architectural information about that particular Blackfin processor. The descriptions cover functional blocks, buses, and ports, including all features and processes that they support.

Typically, a hardware reference manual (HRM) is available for each processor series. For example, Analog Devices provides one HWR for ADSP-BF531/532/533 devices (entitled *ADSP-BF533 Blackfin Processor Hardware Reference*).

Some processors, such as the ADSP-BF542/544/547/548/549 devices, have two manuals, *ADSP-BF54x Blackfin Processor Hardware Reference* and *ADSP-BF54x Blackfin Processor Peripheral Hardware Reference*.

The VisualDSP++ Help system also includes a copy of each hardware reference manual and provides powerful search facilities to help you locate information.

You can find Blackfin processor hardware reference manuals at:
`http://www.analog.com/processors/technical_library`

Blackfin Processor Programming Reference

The *Blackfin Processor Programming Reference* contains information about the processor architecture and assembly language for Blackfin processors. The manual provides information on how assembly instructions execute on the Blackfin processor's architecture, along with reference information about processor operations.

If you intend to program in C only, this document is of no value to you. However, if you intend to author some assembly code, refer to this book.

The processor core and instruction set, which is common to all Blackfin processors, is documented in this manual.

The VisualDSP++ Help system also includes a searchable version of this manual so you can locate information quickly.

You can find the *Blackfin Processor Programming Reference* at:
http://www.analog.com/processors/technical_library

µClinux Distribution Manual

This manual attempts to provide a quick-and-easy guide to help users get started in the Blackfin/µClinux open source community. It provides details on how to use essential tools such as the STAMP board, the Blackfin toolchain, U-Boot, µClinux, and the µClinux Web site. This manual is not a replacement for a Blackfin hardware reference or programming reference. This document gives an overview of the components essential to working with µClinux for Blackfin devices.

Access this manual by visiting this site:
http://docs.blackfin.uclinux.org/doku.php?id=preface

Data Sheets

Data sheets are created for each Blackfin processor and for each release of a single product. Each Blackfin processor data sheet provides:

- A high-level overview of the processor
- A description of processor pins
- Electrical, power, and timing characteristics/requirements
- Device package dimensions
- Environmental (temperature) information

To obtain data sheets for Blackfin processors, access this site:
http://www.analog.com/processors/blackfin

Anomalies Lists for Processors and Tools

Analog Devices maintains an anomalies list for each Blackfin processor series and also maintains an anomalies list for tools. These lists are updated as new information becomes available.

Processor anomalies represent the currently-known differences between revisions of Blackfin devices and the functionality specified in the Blackfin processor data sheets and hardware manuals. A revision number with the form "-x.x" is branded on all parts to identify them according to silicon revisions.

For processor anomalies, refer to:
http://www.analog.com/processors/technical_library

For tools anomalies, refer to:
http://www.analog.com/processors/tools/anomalies

BSDL Files

Boundary scan description language (BSDL) files are necessary for the application of boundary-scan for board and system-level testing and in-system programming. BSDL files are the electronic data sheets that describe the IEEE 1149.1 or JTAG design within an IC, and are provided by the IC vendors as part of their device specifications. Use BSDL files to describe the test logic and generate a test for a loaded board.

IBIS Models

I/O buffer information specification (IBIS) models are used with various IBIS-based simulators for transmission line simulation of digital systems. These models accurately simulate I/O buffers, termination, and circuit board traces. The simulation time is much faster than SPICE (Simulation Program with Integrated Circuit Emphasis) simulations, because it is a behavioral model that relies on tabulated current versus voltage

characteristics. For more information about IBIS models, see the main ANSI/EIA IBIS home page at:
http://www.eigroup.org/IBIS

CROSSCORE Tools Documentation

Documentation in electronic form describes the various components of the CROSSCORE software and hardware tools. Analog Devices offers a software tools environment (VisualDSP++) and an assortment of hardware development tools.

For software tools, each release of VisualDSP++ includes a complete set of online manuals, describing the entire software development toolchain.

"Hardware Tools Documentation" on page 3-15 describes EZ-KIT Lite evaluation systems, emulators, and extender boards.

VisualDSP++ Documentation

This section briefly describes the VisualDSP++ manual set. Electronic versions of documents are available from the VisualDSP++ installation CD-ROM or via download from the following Web page:
http://www.analog.com/processors/technical_library

VisualDSP++ Help incorporates a searchable version of the VisualDSP++ manual set plus processor documentation and other tools manuals. See "VisualDSP++ Help" on page 3-20 for details.

VisualDSP++ Getting Started Guide

This manual provides step-by-step, 15-minute tutorials that highlight VisualDSP++ features. By completing the tutorials, users can become familiar with the VisualDSP++ environment quickly, and see how easy it is to use several tools in your own digital signal processing (DSP) development projects.

This manual and accompanying software provide an excellent starting point to gain a high level of understanding of the VisualDSP++ suite of project management and application development tools.

VisualDSP++ Licensing Guide

VisualDSP++ is a licensed product from Analog Devices. This manual describes how to manage your license(s) for VisualDSP++ software. For users who purchase floating licenses, this guide describes the license server manager.

This manual describes the licensing options available.For node-locked licenses, it explains how to obtain a serial number, and how to install, register, and validate your license. For floating licenses, it explains how to obtain a serial number, install a floating license server, and register and validate your license. This manual also includes troubleshooting information and FAQs for licensing issues.

If you experience a problem after having tried to solve it using the information in this guide, the manual provides Analog Devices Customer Support contact information for further assistance.

VisualDSP++ C/C++ Compiler and Library Manual for Blackfin Processors

This manual contains information about the C/C++ compiler and run-time libraries for Blackfin processors.

The manual provides information on compiler options, language extensions, and C/C++/assembly interfacing, and shows how to optimize compiler operation. It explains how to use library functions and provides a complete C/C++ library function reference.

The manual describes the DSP run-time library, which contains a broad collection of functions commonly required by signal processing applications. The services provided by the DSP run-time library include support for general-purpose signal processing such as companders, filters, and

Fast Fourier Transform (FFT) functions. All these services are Analog Devices extensions to ANSI standard C. These functions are in addition to the C/C++ run-time library functions.

Additionally, the manual describes the dual-core ADSP-BF561 Blackfin processor architecture, and then two approaches to application development using VisualDSP++. It also offers guidelines for developing systems on ADSP-BF561 Blackfin processors.

VisualDSP++ Assembler and Preprocessor Manual

This manual focuses on assembly programming for Blackfin processors that support a media instruction set computing (MISC) architecture.

The manual provides how-to information for writing assembly programs for Blackfin processors and reference information about related development software. It also provides information on new and legacy syntax for assembler and preprocessor directives and comments, as well as command-line switches.

VisualDSP++ Linker and Utilities Manual

This manual provides information on the linking process and describes the syntax for the linker's command language—a scripting language that the linker reads from the linker description file (`.ldf`). The manual leads you through using the linker, archiver, and loader to produce processor programs. It also provides reference information on file utility software.

The manual also describes how overlays and advanced `.ldf` commands are used for memory management. In addition, it describes the expert linker, an interactive graphical tool to set up and map processor memory.

VisualDSP++ Kernel (VDK) User's Guide

This manual contains information about the VisualDSP++ kernel, a real-time operating system kernel integrated with the VisualDSP++ development tools. The VDK incorporates state of the art scheduling and

resource allocation techniques tailored specifically for the memory and timing constraints of DSP programming. Using frameworks of template files, the kernel facilitates development of performance-structured applications. The kernel is designed for effective operations on Analog Devices processors.

The majority of the information in this manual is generic. Information applicable to a particular target processor, or to a particular processor series, is provided in Appendix A, "Processor-Specific Notes." This manual explains the kernel internal structure and operation.

VisualDSP++ Loader and Utilities Manual

This manual contains information on how to use the loader/splitter to convert executable files into boot-loadable (or non-bootable) files. These files are then programmed/burned into an external memory device within your target system.

The manual begins by examining where loading/splitting fits in the typical program development activities. It discusses boot modes, boot streams, and second stage kernels. This manual contains the details you need to know about booting each particular series of Blackfin processors.

VisualDSP++ Device Driver and System Service Libraries Manual for Blackfin Processors

This manual describes device drivers and system services. Included is an overview and detailed description of the device driver model. It covers the device driver API and the various data flow methods that devices use to transfer data into and out of the processor. Included are examples of both DMA-driven and interrupt-driven drivers, and tutorials that show how to quickly write efficient device drivers that comply with the model.

Also included in this manual are the details of powerful system services that are available to applications through the system services library. This manual describes how applications can use the system services library to

control the Blackfin processor's dynamic power management capabilities, control external asynchronous and synchronous memories, and manage interrupt processing. The manual also describes how applications can utilize the services of the DMA and callback to easily schedule both peripheral and memory DMA transfers, and defer non-critical event-driven processing to a lower priority. Details on the APIs for the system services are provided as well as examples that demonstrate how applications can leverage these services.

VisualDSP++ Licensing Guide

This manual describes how to manage your license for VisualDSP++ software. For users who purchase floating licenses, this guide describes the VisualDSP++ Floating License Server.

Hardware Tools Documentation

Each hardware tool (EZ-KIT Lite evaluation system, emulator, extender board, or STAMP board) available from Analog Devices includes electronic documentation. Typically this documentation contains schematics, a short description of switch and jumper settings, and a bill of materials.

Download electronic versions of the documentation (`.pdf` file format) from the following Web page:
`http://www.analog.com/processors/technical_library`

Getting Started With the ADSP-BF537 EZ-KIT Lite Manual

This manual provides exercises for the ADSP-BF537 Blackfin processor while working within the VisualDSP++ development system. In half a day, you can:

- Connect the EZ-KIT Lite (or EZ-Board) to your PC and write your first program
- Measure the performance and the impact of memory hierarchy and voltage on performance
- Use the TCP/IP peripheral of the ADSP-BF537 Blackfin processor
- Connect to your network and build the LwIP stack tailored to your application
- Create a Caesar Cipher application using VDK and LwIP
- Connect to the application with telnet
- Create an audio talk-through application with TCP/IP
- Change the audio and control volume via telnet
- Change clock frequency via telnet

Getting Started With the ADSP-BF548 EZ-KIT Lite Manual

This manual familiarizes users with the hardware capabilities of the evaluation system and demonstrates how to access these capabilities in the VisualDSP++ environment.

EZ-KIT Lite users should use this manual in conjunction with the *ADSP-BF548 EZ-KIT Lite Evaluation System Manual*, which describes the evaluation system's components in greater detail.

ADSP-BF526 EZ-Board Evaluation System Manual

This manual provides instructions for installing the product hardware (board) and software on your PC. The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF526 EZ-Board. Finally, a schematic and a bill of materials are provided as a reference for future designs.

This manual provides information on the EZ-Board from a programmer's perspective and provides a memory map of the board.

ADSP-BF527 EZ-KIT Lite Evaluation System Manual

This manual provides instructions for installing the product hardware (board) and software on your PC. The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF527 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

This manual provides information on the EZ-KIT Lite from a programmer's perspective and provides a memory map of the board.

ADSP-BF533 EZ-KIT Lite Evaluation System Manual

This manual provides instructions for using the hardware and installing the software on your PC. This manual also provides guidelines for running your own code on the ADSP-BF533 EZ-KIT Lite. In addition, the manual describes the operation and configuration of the evaluation board's components. Finally, a schematic and a bill of materials are provided as a reference for future ADSP-BF533 Blackfin processor board designs.

This manual provides information on the EZ-KIT Lite from a programmer's perspective and provides a memory map of the board.

ADSP-BF537 EZ-KIT Lite Evaluation System Manual

This manual provides instructions for using the hardware and installing the software on your PC. This manual also provides guidelines for running your own code on the ADSP-BF537 EZ-KIT Lite. In addition, the manual describes the operation and configuration of the evaluation board's components. Finally, a schematic and a bill of materials are provided as a reference for future ADSP-BF537 Blackfin processor board designs.

This manual provides information on the EZ-KIT Lite from a programmer's perspective and provides a memory map of the board.

ADSP-BF538F EZ-KIT Lite Evaluation System Manual

This manual provides instructions for using the hardware and installing the software on your PC. This manual also provides guidelines for running your own code on the ADSP-BF538F EZ-KIT Lite. In addition, the manual describes the operation and configuration of the evaluation board's components. Finally, a schematic and a bill of materials are provided as a reference for future ADSP-BF538F Blackfin processor board designs.

This manual provides information on the EZ-KIT Lite from a programmer's perspective and provides a memory map of the board.

ADSP-BF548 EZ-KIT Lite Evaluation System Manual

This manual provides instructions for using the hardware and installing the software on your PC. This manual also provides guidelines for running your own code on the ADSP-BF548 EZ-KIT Lite. In addition, the manual describes the operation and configuration of the evaluation board's components. Finally, a schematic and a bill of materials are provided as a reference for future ADSP-BF548 Blackfin processor board designs.

This manual provides information on the EZ-KIT Lite from a programmer's perspective and provides a memory map of the board.

ADSP-BF561 EZ-KIT Lite Evaluation System Manual

This manual provides instructions for using the hardware and installing the software on your PC. This manual also provides guidelines for running your own code on the ADSP-BF561 EZ-KIT Lite board. In addition, the manual describes the operation and configuration of the evaluation board's components. Finally, a schematic and a bill of materials are provided as a reference for future ADSP-BF561 Blackfin processor designs.

This manual provides information on the EZ-KIT Lite from a programmer's perspective and provides a memory map of the board.

EZ-Extender Manuals

The following manuals provide information about the capabilities of the EZ-Extender boards.

Blackfin EZ-Extender Manual

This manual describes the operation and configuration of the components on the extension board. A schematic and a bill of materials are provided as a reference for future ADSP-BF533 and ADSP-BF561 Blackfin processor board designs.

Blackfin A-V EZ-Extender Manual

This manual describes the operation and configuration of the components on the extension board. A schematic and a bill of materials are provided as a reference for future Blackfin processor board designs.

Blackfin USB-LAN EZ-Extender Manual

This manual describes the operation and configuration of the components on the extension board. A schematic and a bill of materials are provided as a reference for future Blackfin processor board designs.

Blackfin Audio EZ-Extender Manual

This manual describes the operation and configuration of the components on the extension board. A schematic and a bill of materials are provided as a reference for future Blackfin processor board designs.

Blackfin FPGA EZ-Extender Manual

This manual describes the operation and configuration of the components on the extension board. A schematic and a bill of materials are provided as a reference for future Blackfin processor board designs.

Blackfin Landscape LCD EZ-Extender Manual

This manual describes operation and configuration of the extender board's components. A schematic and a bill of materials are provided as a reference for future Blackfin processor board designs.

VisualDSP++ Help

VisualDSP++ online Help is a powerful search tool. It combines the following documents and much more in one place:

- Complete VisualDSP++ manual set
- Processor hardware manuals and hardware tools manuals
- Over 200 hundred technical articles (EE-Notes)

The Help system is integrated into the VisualDSP++ graphical user interface and also provides context information (for debugging windows, tools, and dialog boxes). Each task is described in clear step-by-step detail.

Best of all, VisualDSP++ Help provides a single access point to just about every processor hardware and tools document produced by Analog Devices.

The search engine in Help enables you to find information quickly.

VisualDSP++ Help, built around the familiar Microsoft HTML Help standard, enables you to:

- Copy code examples from Help into your source documents
- Bookmark and print topics
- Perform a full text search, or refine a search with wildcards, nested expressions, or Boolean operators

The Collaborative

The Collaborative is a network of processor/DSP third-party developers for Analog Devices. The Collaborative consists of companies all over the world that provide hardware products, software products, algorithms, and design services for a wide variety of applications and markets. Our partners offer consulting services as well as commercial off the shelf products specifically for parts from Analog Devices. To learn more, go to: `http://dspcollaborative.analog.com/developers/DSP_LearnMore.html`

MyAnalog.com

`MyAnalog.com` is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information on products you are interested in. You can also choose to receive weekly e-mail notifications containing updates to the Web pages that meet your

interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration

Visit http://www.myanalog.com to sign up. Click **Register** to use the site. Registration takes about five minutes and serves as a means to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your e-mail address.

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