Underwater Acoustic QPSK Receiver Implementation and Its Test Results at the Very Shallow Water

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Abstract- **In this paper, we describe an DSP based implemented QPSK receiver prototype for 25kHz carrier frequency and 5 kHz symbol rate with excess bandwidth 0.35, and its test results at the very shallow water of the South Sea of Korea. The implemented digital receiver prototype for underwater communication is composed of analog and digital signal processing parts. The analog part, composed of an implemented omni-directional acoustic sensor and a bi-directional deriving unit, is in charge of acquiring the acoustic signal and of converting the acoustic signal into an electric signal. The sampled passband signal should be converted into a baseband signal and then the baseband signal is further processed to enhance the signal quality and reduce decision error by synchronizer, equalizer, and Viterbi decoder. The joint synchronizer detects the packet synchronization and estimates the coarse symbol timing and phase offset at the same time. After synchronization, the received baseband signal is decimated to take 4 samples per symbol which is the input of channel equalizer. The channel equalizer improves the quality of signal by reducing the multipath interference and tracking the phase and frequency offsets. The Viterbi decoder decides the transmitted information using the output of equalizer. The implemented QPSK receiver prototype is tested the BER performance by transmitting 160pixel*100pixel*8bit/pixel images with horizontal transmission distances of 1km, 2km and 3km at the very shallow water (approximately 25m water depth). Test result shows that BER is 0, 2.3×10^{-5}, and 1.8×10^{-3} for the 1km, 2km and 3km transmission distance, respectively.**

I. INTRODUCTION

For a long time, non-coherent transmission scheme, such as FSK, was commonly considered as a unique scheme for underwater acoustic transmission because of a time-varying multipath channel with fast fading and Doppler effect. After, however, Stojanovic, Catipovic and Proakis demonstrated in 1994 the feasibility of phase coherent transmission technique in the underwater, many researchers concentrate on the phase coherent transmission schemes, such as DPSK, PSK, QAM due to the bandwidth efficiency [1-3]. Since late 1990s, communication systems among multiple nodes are developed for oceanographic monitoring such as off-shore monitoring system[4] and exchanging information among multiple AUVs[5][6].

MOERI, KORDI has also developed an underwater acoustic-based communication network (UA-Net) since 2004. This project aims at the development of an underwater acoustic modem platform and underwater acoustic Ad-hoc network among mobile and fixed underwater communication nodes using developed acoustic modem as a PHY. The network covers not only acoustic network among underwater nodes, but also RF network for exchanging data among underwater nodes and nodes on the surface or ground. UA-Net consists of underwater acoustic communication system, gateway, and a control center for management and monitoring the operation of nodes and gathering oceanic data from underwater nodes.

In this paper, we describe an DSP based implemented QPSK receiver prototype for 25kHz carrier frequency and 5 kHz symbol rate with excess bandwidth 0.35 which will be used as a PHY of UA-Net under developing.

II. HARDWARE IMPLEMENTATION

The prototype hardware of underwater acoustic modem is composed of three parts, that is, DSP system, acoustic sensor and acoustic sensor deriving unit as shown in Fig. 1 In this section, each hardware parts will be described.

DSP system

The DSP system is equipped with a PC board, two DSP boards, one ADC board, and one DAC board. The boards of the DSP system exchanges their data via shared PCI bus. A PC board controls the operation mode to be one of transmitting and receiving mode and monitors underwater acoustic modem by periodically acquiring the intermediate data of signal processing blocks from the DSP boards. One TS-C43 DSP board, which has 4 floating point DSP devices, providing up to 2.4 billion 40-bit MACs (multiply-accumulate) per second, is used for transmitter and the other DSP board for receiver. Although the operation mode is controlled by the PC board and two DSP boards are required for transmitting and receiving operation in the current implementation, all operation will be implemented within one DSP board in the near future.

ADC board supports simultaneous sampling upto 8 input channels and each channel can take upto 200k samples per second with 16-bit resolution. It has 8-bit bidirectional digital port and two control lines. The implemented receiver used only one channel with 100k sampling rate among 8 input

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channels and one control line for switching the operation mode of sensor deriving unit.

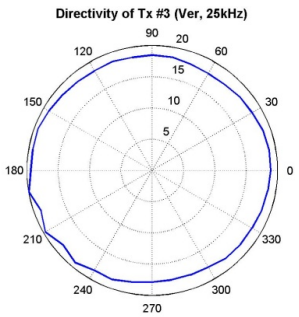
DAC board supports simultaneous sampling upto 12 output channels and each channel can take 400k samples per second with 16-bit resolution. The implemented transmitter uses only one channel with 200k sampling rate.

Sensor and deriving unit

The sensor and the sensor deriving unit are in charge of transmitting the modulated electric waveform into an acoustic waveform and converting the acoustic waveform presented in the channel into an electric one to supply to the input of ADC. We have implemented an omni-directional acoustic sensor and its deriving unit. The photos of implemented omni-directional sensor and deriving unit are shown in Fig. 1. The implemented acoustic sensor and its bi-directional deriving unit are used as the analog part of the implemented acoustic modem which operates in half duplex mode.

Figure 1. Photos of implemented omni-directional acoustic sensor(left) and transmitting and receiving amplifier to derive omni-directional sensor (right)

The implemented acoustic sensor has a cylindrical shape with the length of 13.6cm and the diameter of 6.7cm, which includes a spherical shaped ceramic and a pre-amplifier, and it connects deriving unit via 20m long cable. The beam pattern of omni-directional acoustic sensor measured at 25kHz is shown in Fig. 2 and Fig. 3 where the positive angle means a rotate angle of sensor to the reference point to the count clock wise direction. In horizontal direction, the beam pattern shows relatively even level as expected. In vertical direction, a large energy of signal is measured at the bottom part of 260°~100°, no energy of signal is measured at the top part for the cable, and about 6dB lower beam energy is



measured at the 30° and 330°.

Figure 2. Beam pattern of omni-directional acoustic sensor in the horizontal direction

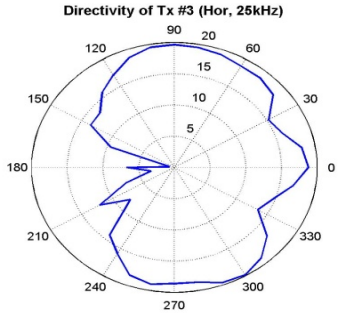


Figure 3. Beam pattern of omni-directional acoustic sensor in the vertical direction

The measurements of the TVR(transmit voltage response) and RVS(receive voltage sensitivity) of implemented sensor are depicted in Fig. 4 and Fig. 5. As you can see in the figures, there are three measurement results are shown since 3 sets of sensor and deriving units are implemented. The sensor has 140dB~150dB TVR and -155dB~-147dB RVS within the frequency range of 20kHz and 30kHz. The TVR and RVS performance improve as the frequency increases.

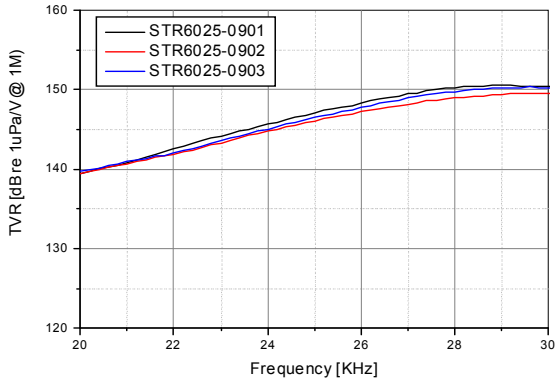


Figure 4. Measured TVR characteristics of implemented omni-directional acoustic sensors

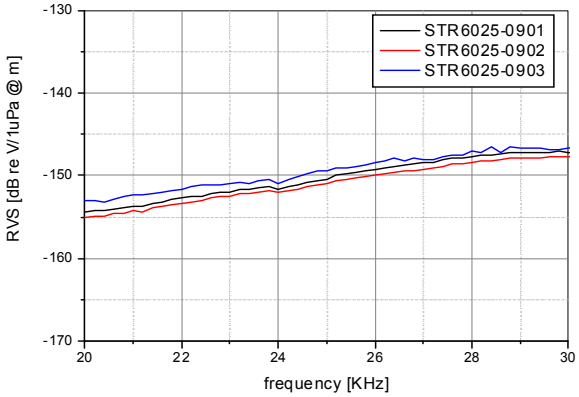


Figure 5. Measured RVS characteristics of implemented omni-directional acoustic sensors

The deriving unit has a power amplifier for signal transmission and an amplifier for signal reception. One of amplifiers is activated by the control signal according to the operation mode of half-duplex modem. The gain of power amplifier can be manually controlled continuously from 0dB to 25dB. The receiving amplifier supports not only manual gain control but also automatic gain control by the switch on the connection panel. The automatic gain control range is 0dB~40dB. In the manual gain control mode, unlike the continuous gain control of power amplifier, the gain of receiving amplifier can be selected among stepwise gains of -20dB, -6dB, 0dB, 14dB and 20dB. The measured frequency response functions of amplitude and phase are shown in Fig. 6 according to the selection of receiving gain.

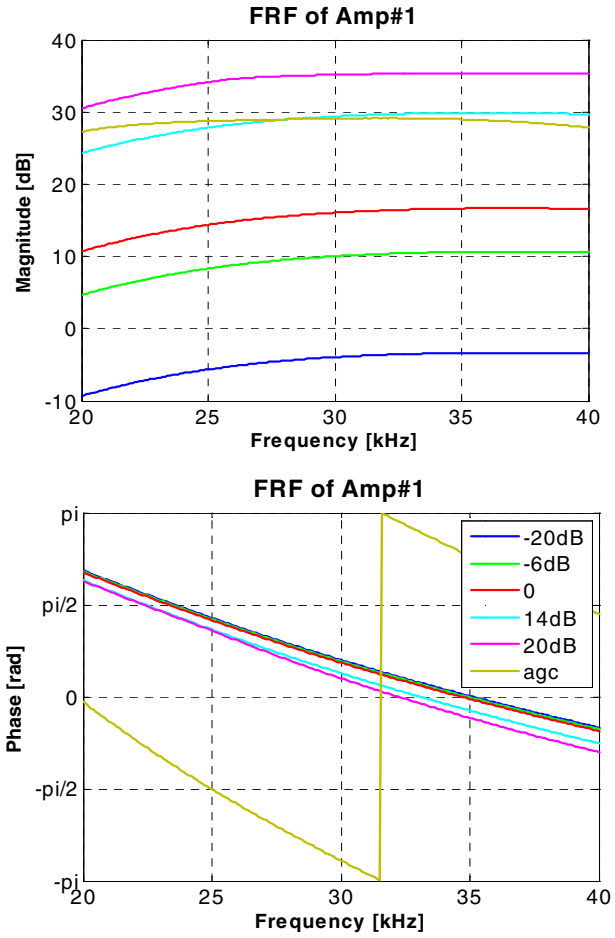


Figure 6. Frequency response function of implemented receiving amplifier: amplitude response(upper) and phase response (lower)

III. Software Implementation

Packet structure and transmitting signal

The implemented modem sends the information data using packet transmission. The structure of packet is shown in Fig. 7. One packet can be divided into a 100-QPSK-symbol-length preamble and a 400-QPSK-symbol-length payload. The preamble part of each packet is used for the detection of signal existence in the current received signal, the estimation of synchronization parameters, such as packet timing, symbol timing and phase offset, and the initial training the adaptive channel equalizer in the receiver. The payload part contains the encoded information data to be sent. The information data is encoded using convolutional encoder with rate 1/2 and K=7 (generate polynomial : 247, 371), and then the encoded data is interleaved via 20x40 block interleaver to scatter the consecutive errors into random errors. The interleaver output is mapped into QPSK symbols. Equivalently, one information bit is encoded into 2 encoded bits and 2 encoded bits are mapped into one QPSK symbol. Therefore, one packet can carry 50 bytes (400 bits) source data.

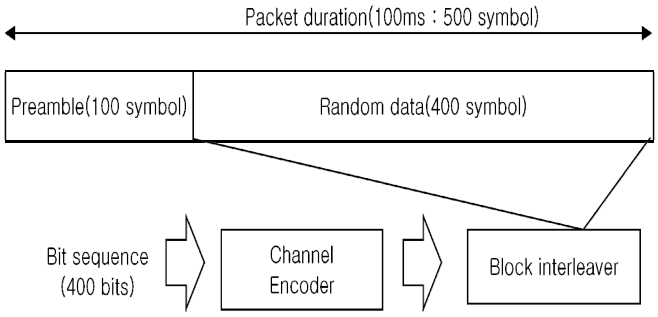


Figure 7. Packet structure and procedures of mapping payload data from information bit sequence

The mapped QPSK symbol sequence is pulse-shaped using a root-raised cosine filter with excess bandwidth of 0.35 and then the filtered sequence is modulated to the passband sequence with the carrier frequency of 25kHz in the digital signal processing domain. The passband sequence is transmitted via DAC and analog signal processing part. The transmitting signal is a QPSK signal with 5kHz symbol rate and 25kHz carrier frequency.

Receiver signal processing procedures

The received analog signal is sampled at 100kHz rate, which is 20 times oversamples to symbol rate and 4 times to the carrier frequency. The signal processing procedures of receiver is shown in Fig. 8. The sampled passband signal is converted into a baseband signal by frequency shifting and lowpass filtering. The joint packet time, symbol time and phase estimator determines whether the packet is or not in the received signal, and then estimates a coarse symbol time and a phase offset if it determines there is a packet. The packet detection turns on the switch to send the lowpass filtered sequence to the decimator. The decimator decimates even spaced samples with the reference of the symbol time estimate into a 4 times oversampling sequence to be used as an input of joint equalizer. The equalizer is used to cope with ISI (inter symbol interference) due to the multipath. The joint equalizer combines an equalizer with a PLL (phase locked-loop)[7]. The

equalized signal is block de-interleaved and then Viterbi decoded to decide the transmitted data.

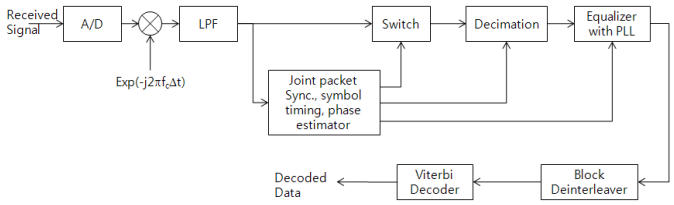


Figure 8. Functional block diagram of digital signal processing of receiver

The output of frequency shifter can be represented as (1).

$$r_{demix}(k) = r(k) \cdot \exp\left(-j\pi\frac{k}{2}\right) \quad (1)$$

where r(k) is the k-th sample of received analog signal, r(t). Since $\{\exp(-j\pi k/2)\}$ is a periodic sequence of {1, -j, -1, j}, $r_{demix}(k)$ can be represented according to k as follows

$$r_{demix}(k) = \begin{cases} r(k) & \text{for } k = 4N \\ -jr(k) & \text{for } k = 4N+1 \\ -r(k) & \text{for } k = 4N+2 \\ jr(k) & \text{for } k = 4N+3 \end{cases}, \quad (2)$$

where N is any integer. From (1) and (2), the frequency shifting can be performed without any complex multiplication and the half of real and imaginary sample sequences of frequency shifter output becomes zero which reduce more than 50% computational complexity for frequency shifting and lowpass filtering.

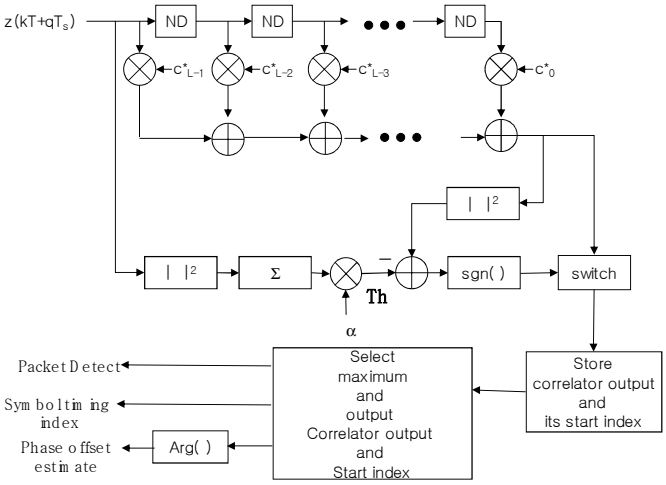


Figure 9. Functional block diagram of joint packet detection and coarse symbol timing and phase offset estimation

The joint packet detector, symbol timing estimator and phase offset estimator, shown in Fig. 9, jointly determines packet timing and symbol timing at the same time by comparing some threshold value with the energy (the square of absolute) of the output of correlator, which computes a correlation between the complex conjugate of some part of the known preamble, c_k^*, and the symbol spaced received sample sequence at each sample points. The threshold value is computed by multiplying a scaling constant by the energy of the received samples used for computing correlation value at this time. If the energy of the correlator output is not less than the threshold value, joint detector and estimator stores the correlator output value and the start sample index of the received samples used for computing correlation. This store process is performed for one packet time. Among the stored sets of the correlator output and the start index, joint packet and symbol timing estimator searches one set which has the biggest energy of the correlator output, and then determines the start index of the searched set as the symbol time of the packet start symbol. That is, one of sample indexes for one symbol becomes the estimate of the symbol time. Since the implemented receiver takes 20 samples per symbol, the symbol timing error of this symbol timing estimate is less than 1/40 symbols if the selected sample index is correctly selected. Furthermore, this residual small symbol timing error is compensated at the fractionally spaced equalizer. The phase offset is estimated by computing the phase of the correlator output of the searched set, which is used for packet detection and symbol timing estimation. If there is no correlator output not less than the threshold value, the packet detector decides that there is not a packet in the received signal at this moment and the samples data are discarded.

The estimated symbol time is used as the start sample index of the packet and the estimated phase offset is used as the initial value of phase offset at the phase tracker at the joint equalizer and phase tracker unit shown in Fig. 10[7].

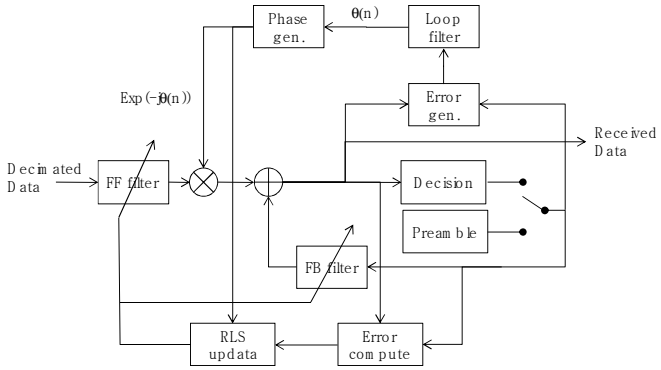


Figure 10. Block diagram of equalizer with PLL

The received sampling sequence is decimated into an even spaced 4 times over sampling sequence started at the symbol timing of the packet. The decimated sequence is enforced into a fractional spaced decision-feedback equalizer with PLL (phase-looked-loop). The data-aided equalizer trains its tap weights using the known preamble symbols at the beginning part of packet and then using the decided symbol on the equalized signal. To update the tap weights, RLS algorithm [8] is used since it shows very fast convergence speed, which is

suitable for relatively short packet burst transmission. We use just a 20-tap FF filter and a 10-tap FB filter for equalizer.

For tracking the phase of received signal, 2nd order loop filter is used which can trace the phase offset and small frequency offset[9]. The phase of PLL is initialized by the phase offset estimate.

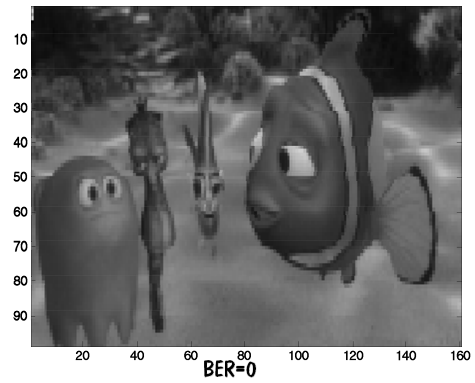
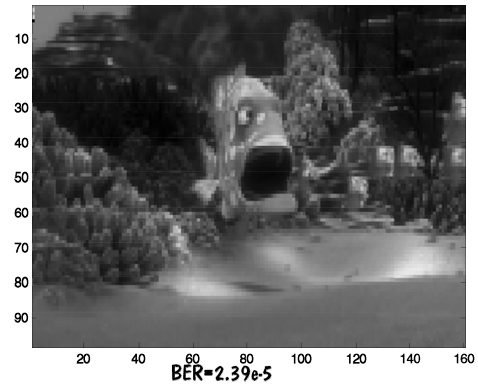
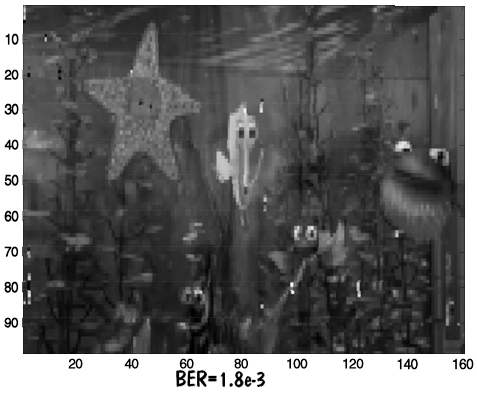


Figure 11. Received images and their BER measurements for 1km(upper), 2km(middle) and 3km(buttom) horizontal transmission distance





The equalized symbol sequence is de-interleaved to be used as a input sequence of Viterbi decoder. Note that only the payload data in a packet is used as the input of de-interleaver. Viterbi decoder corrects errors induced in the channel. Viterbi decoder initializes its state metric and path metric at the beginning of each packet decoding and determines the transmitted payload data at the end of packet. A decoded packet data is saved at the temporal buffer to be sent to control processor for upper layer process such as network layer, session layer and so on.

IV. TEST RESULTS AT SHALLOW WATER

The implemented QPSK receiver prototype is tested at the very shallow water in January 2010 at the Jinhea Bay in the South Sea of Korea, where the water depth is about 25m. We use two fishing boats for test. The receiving boat anchors and acoustic sensor is fixed at the 6m depth from the surface. The transmitting boat also anchors when test is performed at one point and after finishing test it moves another point. The transmission distances are 1km, 2km and 3km. The transmitting acoustic sensor is fixed at the 12m from the surface.

In the test, we measure the BER performance of implemented QPSK receiver prototype by comparing the received 160pixel*100pixel*8bit/pixel images with transmitting ones. Since we do not use any image compression scheme, it takes 32 seconds to send one image. To detect the start packet of image, we replace first 4 bytes of the image data with a pre-determined data.

Receiving images according to the propagation distances are shown in Fig. 11 with the measured BER. For 1km transmission distance case, most of receiving images are error free and some of images shows burst error, which means most of decoded information bits of one packet are error. Burst error occurs when the packet start detection is wrong. For 2km and 3km cases, the BER of receiving images are 2.39×10^{-5} and 1.8×10^{-3}, respectively. Therefore, implemented QPSK receiver prototype works well upto 3km in shallow water.

V. CONCLUSION

An QPSK receiver prototype for 25kHz carrier frequency and 5 kHz symbol rate with excess bandwidth 0.35 is implemented using an implemented omni-directional acoustic sensor, a bi-directional deriving unit and DSP system on which signal processing processes are performed to recover the transmitted information data correctly. This paper reports the characteristics of the implemented omni-directional acoustic sensor and its deriving unit. Furthermore, the implemented receiver structure and the packet structure are described. The implemented QPSK receiver prototype is tested the BER performance by transmitting 160pixel*100pixel*8bit/pixel images with horizontal transmission distances of 1km, 2km and 3km at the very shallow water (approximately 25m water depth). Test results show that BER is 0, 2.3×10^{-5}, and 1.8×10^{-3} for the 1km, 2km and 3km transmission distance, respectively.

In the current implementation, although the operation mode is controlled by the PC board and two DSP boards are

required for transmitting and receiving operation, all operation will be implemented within one DSP board and sophisticated MAC and routing protocols are designed and integrated with physical layer to support an Ad-hoc network in the near future.

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