SA.45s Chip-Scale Atomic Clock

098-00055-000 User Guide

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Power Matters.™

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1 Revision History

The following table shows important changes made in this document for each revision.

Revision	Changes
Revision C (July 2016)	Updated to reflect 1.08 and 1.09 firmware implementation. Per EC11049
Revision B (May 2014)	Updated to reflect 1.06 and 1.07 firmware implementation and Microsemi branding. Per EC09876
Revision A (July 2011)	Initial release per EC06053.

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2 Preface

2.1 About this document

The SA.45s User's Guide provides basic recommendations for designing products to use Microsemi's SA.45s Chip-Scale Atomic Clock (CSAC). The guidelines in the document are generic because specific product requirements vary from one application to the other.

This material consists of a brief description of SA.45s design supported by block diagrams, description of environmental issues, installation guidelines, and unit operation.

2.2 Intended Audience

This document is intended for engineers and telecommunications professionals who are designing, installing, operating, or maintaining time, frequency, and synchronization systems having a requirement for a low profile and highly precise frequency generator.

To use this document effectively, you should have a good understanding of digital telecommunications technologies and analog frequency generation and synthesis techniques.

2.3 Warnings, Cautions, Recommendations, and Notes

Warning: To avoid serious personal injury or death, do not disregard warnings. All warnings use this symbol. Warnings are installation, operation, or maintenance procedures, practices, or statements, that if not strictly observed, may result in serious personal injury or even death.

Caution: To avoid personal injury, do not disregard cautions. All cautions use this symbol. Cautions are installation, operation, or maintenance procedures, practices, conditions, or statements, that if not strictly observed, may result in damage to, or destruction of, the equipment. Cautions are also used to indicate a long-term health hazard.

ESD Caution: To avoid personal injury and electrostatic discharge (ESD) damage to equipment, do not disregard ESD cautions. All ESD cautions use this symbol. ESD cautions are installation, operation, or maintenance procedures, practices, conditions, or statements that if not strictly observed, may result in possible personal injury, electrostatic discharge damage to, or destruction of, static-sensitive components of the equipment.

Note: All notes use this symbol. Notes contain installation, operation, or maintenance procedures, practices, conditions, or statements that alert you to important information, which may make your task easier or increase your understanding.

Note: Microsemi offers training courses designed to enhance your knowledge of the SA.45s Cesium Frequency Standard. Contact your local representative or sales office for a complete list of courses and outlines.

2.4 Reference Documents

For additional information about the products described in this guide, please contact your Microsemi representative or your local sales office. You can also contact us on the web at www.microsemi.com.

- *CSAC Developer's Kit (990-00123-000)*
- *CSACdemo Software (084-00365-000)*

3 SA.45s Chip Scale Atomic Clock

3.1 Introduction

The Microsemi Quantum™ Model SA.45s Chip-Scale Atomic Clock (CSAC) is the world's smallest, lowest power atomic clock technology. This User's Reference Guide provides the basic guidelines and recommendations for designing products with the SA.45s reference. These are generic, and should be tailored for each application.

This document is intended for engineers, technicians, and technologists who are designing, installing, operating or maintaining time, frequency and synchronization systems. The SA.45s is a low profile, highly precise frequency generator. To use this document effectively, an understanding of digital communication technologies is required. It is advantageous to have a background in frequency generation and synthesis techniques.

3.2 SA.45s Overview

The Microsemi SA.45s CSAC is the world's first commercially available chip scale atomic clock, providing the accuracy and stability of atomic clock technology while achieving true breakthroughs in reduced size, weight and power consumption. The small size (less than 17 cc) and low power consumption of the CSAC (less than 125 mW) enables atomic timing accuracy in portable, battery-powered applications.

Figure 1 • **Microsemi Quantum SA.45s Chip Scale Atomic Clock (CSAC)**

The SA.45s provides RF and 1 PPS outputs at standard CMOS levels. It accepts a 1 PPS input to synchronize the output to within 100 ns of a reference clock. It can also discipline its phase and frequency to within 1 ns and 1e-12, respectively.

This user guide provides engineering information for use of the SA.45s. It also provides supporting information for use of the developer's kit (p/n 090-44300-000). Furthermore, the design details of the developer's kit can be used to assist with host system design (for example, power conditioning, signal buffering). This guide must be used in conjunction with the current data sheet for SA.45s, which is available on the Microsemi web site at www.microsemi.com.

3.2.1 Precautions

ESD Caution: To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the CSAC.

3.2.2 Packaging

Retain the original CSAC ESD-safe packaging material in the event that the device needs to be returned to Microsemi for service.

3.2.3 Absolute Minimum and Maximum Ratings

Table 1 indicates the absolute minimum and maximum ratings to which the CSAC can be subjected without permanent unrecoverable damage.

Note: The CSAC cannot be expected to perform normally when operated outside of the recommended operating conditions. All ratings apply at 25°C, unless otherwise noted.

Table 1 • **Absolute Maximum Ratings**

Parameter	Rating
Supply voltage (Vcc)	0 - 4.1 V
Analog tuning voltage	0 - Vcc
Maximum current draw	1 PPS input, RS232, BITE: +/- 2 mA 1 PPS output, RF output:+/- 20 mA
Storage temperature	-55°C to +90°C
Note: *Refer SA.45s datasheet for updated parameters.*	

3.2.4 Mechanical Interface and Mounting Considerations

The physical dimensions of the SA.45s CSAC are 1.6" x 1.4" x 0.45" H. Figure 2 shows the detailed dimensions of CSAC.

Figure 2 • **CSAC Mechanical Drawing**

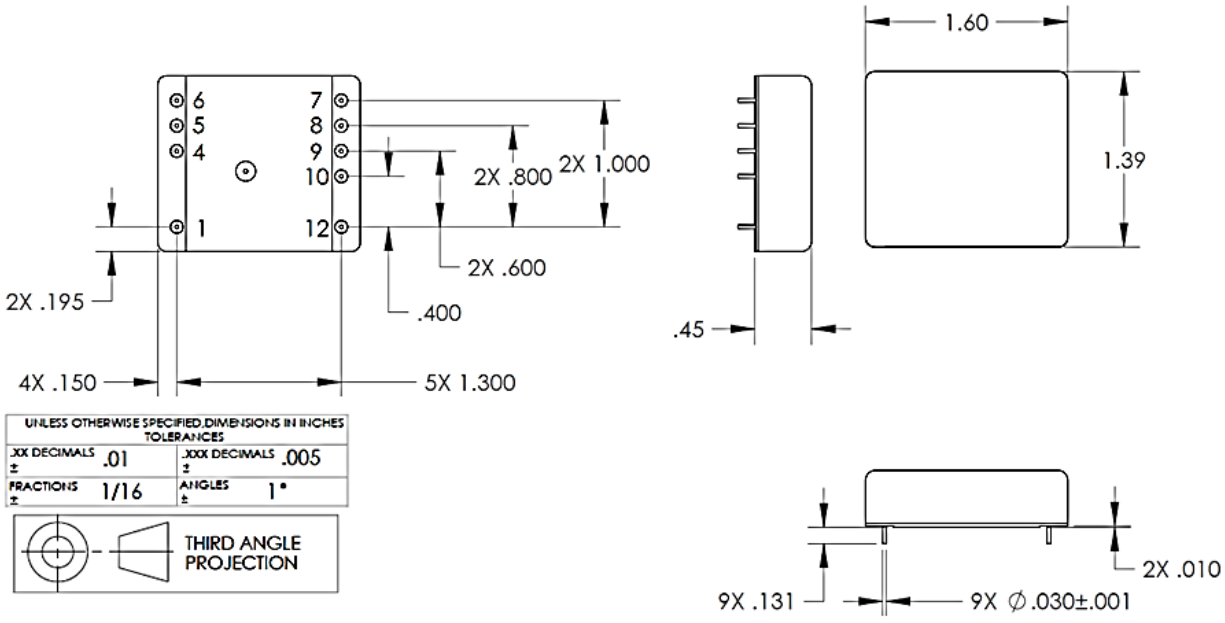
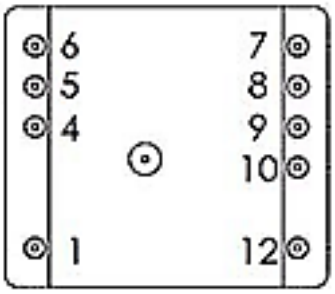


Table 2 shows the pin-out of the SA.45s CSAC.

Table 2 • **SA45s CSAC Pin out**

PIN	I.D.	
1	Tune	 Bottom view
2	N/A	
3	N/A	
4	BITE	
5	Tx	
6	Rx	
7	VCC	
8	GND	
9	1 PPS input	
10	1 PPS output	
11	N/A	
12	RF output	
Note: *Pins labeled N/A are not present in the SA.45s.*		

3.2.5 Recommended Operating Characteristics

The SA.45s pin-out is shown in Table 2. The electrical function of each pin is shown in Table 3.

Table 3 • **Recommended Operating Characteristics**

PIN	Function	Level	Notes	Ref. Section
1	Analog Tuning Input	0-2.5 V	1	"Analog Tuning" section on page 19
4	BITE	Logic H >2.8 V Logic L < 0.3 V	2	"Built-In Test Equipment (BITE)" section on page 13
5, 6	RS232	2.8 V < Logic H < Vcc 0 V < Logic L < 0.3 V	–	"Programmers Reference" section on page 22
7	VCC	3.3 VDC ± 0.1 VDC	–	–
8	Ground	-	–	–
9	1 PPS in	2.5 V < Logic H < Vcc 0 V < Logic L < 0.5	3	–
10	1 PPS out	2.8 V < Logic H < Vcc 0 V < Logic L < 0.3V	4, 5	"1 PPS Output" section on page 15
12	RF Out	2.8 V < Logic H < Vcc 0 V < Logic L < 0.3V	–	"RF Output Characteristics" section on page 13

Notes:

1. Analog Tuning Sensitivity is: $\Delta f/f = (V_{tune} - 1250\ mV) \times 1.77 \times 10^{-11}\ /mV$

   EQ 1

2. Built in Test Equipment:
   0 = Normal Operation
   1 = Unlock Condition
3. Timing reference is rising edge of input pulse on Pin 9.
4. Output 1 PPS is 100 µs in duration for option 001; Refer to data sheet for other options. (400 µs for firmware versions 1.06 and earlier).
5. Timing reference is the rising edge of Pin 10. Rise time < 10 ns at a load capacitance of 10 pF.
6. See *SA.45s datasheet* for updated parameters.

3.3 Functional Description

3.3.1 Principle of Operation

The CSAC is a passive atomic clock, incorporating the interrogation technique of coherent population trapping (CPT) and operating on the D1 optical resonance of atomic cesium. A complete description of passive atomic clocks, CPT, and the CSAC architecture is beyond the scope of this user guide.

Figure 3 • **Simplified CSAC Block Diagram**

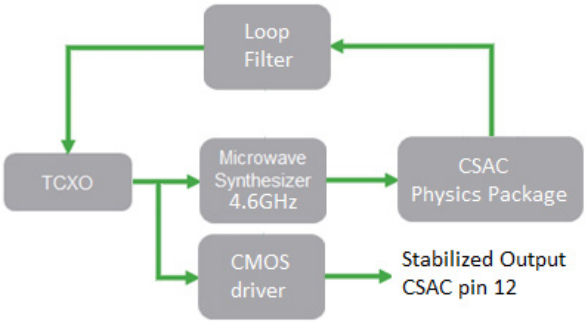


Figure 3 shows a simplified block diagram of the CSAC. The principal RF output from the CSAC is provided by a temperature-compensated crystal oscillator (TCXO), which is buffered by a CMOS logic gate and provided on the CSAC output pin 12. In normal operation, the frequency of the TCXO is continuously compared and corrected to ground state hyperfine frequency of the cesium atoms, contained in the physics package, which thereby improves the stability and environmental sensitivity of the TCXO by 4-5 orders of magnitude. In addition to the TCXO and the physics package, which is described in detail in [1], the essential components of the CSAC are the microwave synthesizer and the microprocessor (see [2]). The microwave synthesizer generates 4596.3x MHz with microprocessor-controlled tuning resolution of approximately 1 part in 10^{12}. The microprocessor serves multiple functions, including implementation of the frequency-lock loop filter for the TCXO, optimization of physics package operation, state-of-health monitoring, and command and control via RS232.

When the CSAC is initially powered on, it performs an acquisition sequence, which includes stabilizing the temperature of the physics package, optimizing physics package operating parameters, and acquiring frequency lock to the atomic resonance. The acquisition process may be monitored via the status field of the telemetry (see "Telemetry (6 and ^)" on page 25). On power-up, the status begins at 8 (oven warm-up). The status value decrements numerically through the acquisition until normal operation (status=0) is achieved.

1. R. Lutwak, et. al., The Chip-Scale Atomic Clock - Low-Power Physics Package, Proceedings of the 36th Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting, December 7-9, 2004, Washington, DC.
2. R. Lutwak, et. al., The MAC - A Miniature Atomic Clock, Proceedings of the 2005 Joint IEEE International Frequency Control Symposium and Precise Time & Time Interval Systems & Applications Meeting, August 29-31, 2005, Vancouver, BC.

3.3.2 Start-up Sequence

Caution: To avoid severe damage to the unit, do not apply power to the incorrect terminals. The SA.45s does not have reverse voltage protection.

When power is connected to Pin 7, the SA.45s unit begins its warm-up cycle. A signal appears at the output once power is applied to the unit. This output signal is not stable until the oscillator is locked (indicated by the BITE pin at CMOS_low).

After 3 minutes, the CSAC achieves Lock and BITE = 0 (See "Built-In Test Equipment (BITE)" on page 13). Power consumption during warm-up is greater than during normal operation; it is specified on the *CSAC datasheet*.

It is recommended to always allow CSAC to remain powered on for >102s after it acquires LOCK. 102s is the minimum amount of time necessary to save CSAC set points to memory. Otherwise, upon the next power up, the unit may go in to a mode of operation where it re-acquires all of its set points; warm-up time will then be out of specification.

3.3.3 Built-In Test Equipment (BITE)

CSAC state-of-health can be monitored electronically on Pin 4 (BITE) of the SA.45s CSAC. Frequency lock is indicated both by status = 0 in the status field of telemetry and by the electrical state of the BITE output pin, which is high (logic 1) upon initial power-on and whenever status ≠ 0. The BITE pin is a high-impedance CMOS logic output.

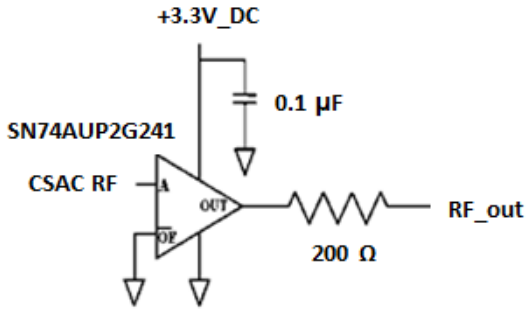
Note: When not locked, BITE = 1 and also status ≠ 0 in the `status` field of the telemetry output string.

At the conclusion of the acquisition sequence (status = 0), BITE remains high for an additional 5 seconds in order to avoid false indication in the event of acquisition failure. Subsequently, BITE provides an immediate (within 1 second) indication of lock failure or alarm.

3.3.4 RF Output Characteristics

The buffered CMOS RF output is provided on Pin 12 of the SA.45s CSAC. The output series impedance is 200 Ω. For reference, the output driver circuit of the SA.45s is shown in Figure 4.

Figure 4 • **CSAC RF Output Driver Circuit**



The SA.45s is designed for embedded low-power applications, that is it is expected to drive a high impedance input, not a 50 Ω measurement instrument or transmission line.

Note: Driving a 50 Ω line at 13 dBm consumes nearly as much power as the CSAC itself. If a high- level (high-power) output driver is required, a driver circuit must be implemented external to the CSAC, such as the one implemented on the Evaluation Board (see "Notes on the Evaluation Board" on page 41).

The RF output appears on Pin 12 after the CSAC is powered ON and is always present, regardless of the lock status. When the CSAC is out of lock (BITE=1, status ≠ 0), the output frequency is provided by the free-running TCXO, which has frequency accuracy specification of +/- 20 ppm and temperature sensitivity of ≈ +/- 30 ppb/°C. Typically, the unlocked frequency accuracy during acquisition is significantly better than this (<1 part in 10^8) as the CSAC memorizes its last-known-good tuning voltage and restores this voltage upon power-up and/or subsequent recovery from loss-of-lock.

3.3.5 Frequency Steering

Note: CSACdemo is a graphical interface used to communicate and control a CSAC. To display the functionality of CSAC, screen shots of CSACdemo are included in the sections that follow. For more information on CSACdemo, see "CSACdemo Operation" on page 35.

For external steering and/or calibration, the CSAC internal microwave synthesizer may be adjusted by the user via the RS232 `!F` command (see "Frequency Adjustment (F)" on page 27). Steering values are entered in (integer) units of parts in 10^{15}, though the resolution realized by the CSAC hardware is approximately 1 part in 10^{12}. Steering commands may be entered as either absolute steers (`!FA`) or as relative steers (`!FD`). In the case of an absolute steer, the contents of the steer register are replaced with the new value. In the case of a relative steer, the new value is summed with the existing value in the steer register. In either case, the maximum steer that can be entered in a single `!F` command is +/- 2 $pp10^8$ (+/- 20000000 $pp10^{15}$). If a larger correction is sent to the CSAC, the maximum allowed steer is applied. The maximum total steering (including cumulative relative steering commands) is also limited at +/- 2 $pp10^8$. For instance, if a number of relative steers are applied such that the total steering exceeds +/- 2 $pp10^8$ the total steering is clamped to the maximum correction.

Note: Steering commands may be entered during acquisition (Status ≠ 0) but will not take effect until lock is achieved.

Frequency steering is volatile. Upon reboot, the CSAC returns to its nominal (calibrated) frequency setting. To update the non-volatile calibration, use the frequency Latch command (see "Frequency Adjustment (F)" on page 27).

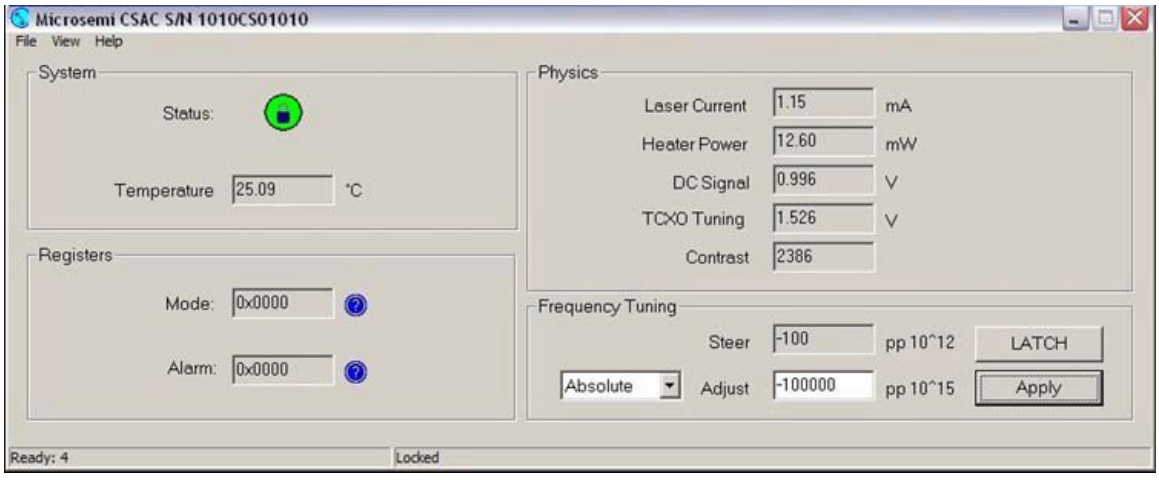
The current steering value appears in the telemetry string as `Steer`.

Note: Steer reports the actual hardware steering, in units of $pp10^{12}$, even though the software registers maintain resolution of $pp10^{15}$, so that many small relative corrections may be applied. As a result, the reported value may appear to disagree with the applied correction by one unit or so due to roundoff error. An example is provided in "Frequency Adjustment (F)" on page 27.

To apply a frequency correction from the main panel of CSACdemo, select relative or absolute from the pull down menu and enter the desired steering into the Adjust field in $pp10^{15}$.

Figure 5 shows an example where an absolute correction of -100000 $pp10^{15}$ is entered. The correction is applied to the CSAC when the **Apply** is selected.

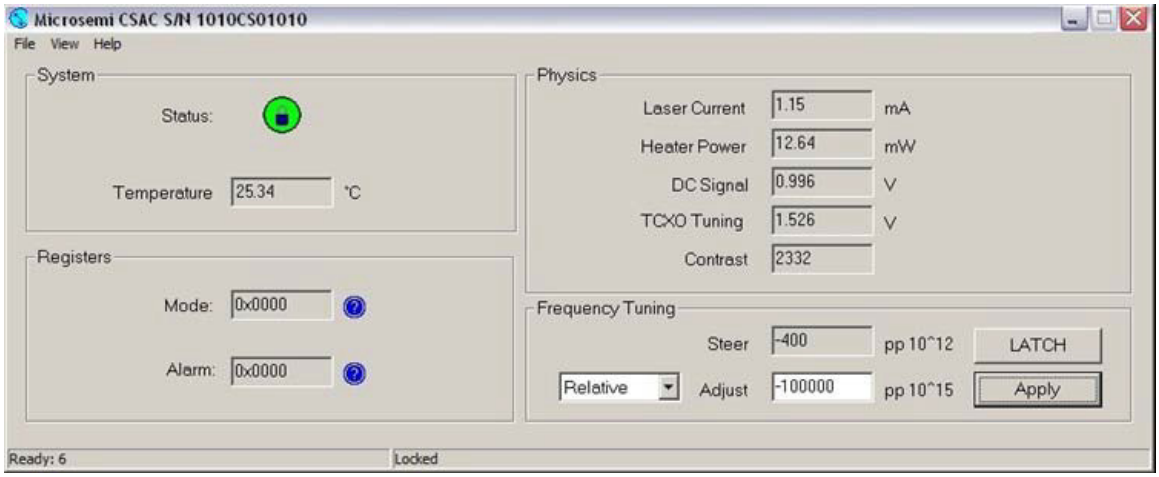
Figure 5 • **Absolute Frequency Adjustment**



As shown in Figure 5, after **Apply** is clicked, the correction is applied to the CSAC and the value of `Steer` changes (on the next polling update) to indicate the internal correction of -100 $pp10^{12}$.

Figure 6 shows an example of relative frequency tuning after absolute steer is reset to 0. In this example, each time **Apply** is clicked, an additional correction of -100000 $pp10^{15}$ is applied to the CSAC. In Figure 6, **Apply** is clicked a total of four times. The resultant value of Steer is -400 $pp10^{12}$.

Figure 6 • **Relative Frequency Adjustment**



3.3.5.1 Frequency Calibration

The internal frequency calibration of the CSAC is set prior to shipment. It is sometimes desirable (and likely) that the calibration needs to be updated from time to time to remove cumulative frequency aging offsets.

Calibration of the CSAC is a two-step process—First, the CSAC is steered onto frequency, either via an external `!F` command (see "Frequency Steering" on page 14), through 1 PPS disciplining (see "1 PPS Disciplining" on page 17), or with analog tuning (see "Analog Tuning" on page 19). Second, the present value of steer is summed into the non-volatile calibration register via the RS232 frequency Latch command (see "Frequency Adjustment (F)" on page 27). Following a Latch command, the value of steer is reset to zero.

Note: The Latch command is only valid when the CSAC is locked (Status = 0).

To Latch the current steer value to non-volatile storage from CSACdemo, click **LATCH**.

Warning: It may be tempting, particularly in disciplining applications, to frequently Latch the steering value into calibration in the event of unforeseen power outage. This is HIGHLY DISCOURAGED for the following reason. The lifetime of the CSAC's NV memory is finite; updating it >10,000 times will DAMAGE it and render the CSAC INOPERABLE.

3.3.6 1 PPS Output

A CMOS level 1 pulse-per-second (1 PPS) output is available on Pin 10 upon power up. The output series impedance is 200 Ω. The output driver circuit is similar to that of the RF output (see Figure 4 on page 13). Nominal levels are 0 - 3.3 VDC. For synchronization purposes, the on-time point is the rising edge of Pin 10.

The 1 PPS output is derived by digital division of the RF reference frequency. The frequency stability and accuracy of the 1 PPS output reflects that of the RF output. Consequently, when unlocked (BITE=1, status ≠ 0), the 1 PPS stability reflects that of the free-running TCXO.

3.3.7 1 PPS Synchronization

The 1 PPS output is synchronous with one rising edge of the RF output (Pin 12). The 1 PPS output may be synchronized with a particular cycle of the RF by applying a synchronization pulse to Pin 9. When synchronized, the counters are reset such that the 1 PPS output occurs on the RF rising edge, which is nearest to the externally-applied rising edge. In this way, the CSAC 1 PPS can be synchronized to within one clock cycle (+/- 100 ns) of the external reference.

The CSAC provides two modes for 1 PPS synchronization, Manual and Automatic, which are selected via a bit in the Mode Register (see "Set/clear Operating Modes (M)" on page 28).

Note: The configuration of the Mode Register is non-volatile (preserved across power cycles).

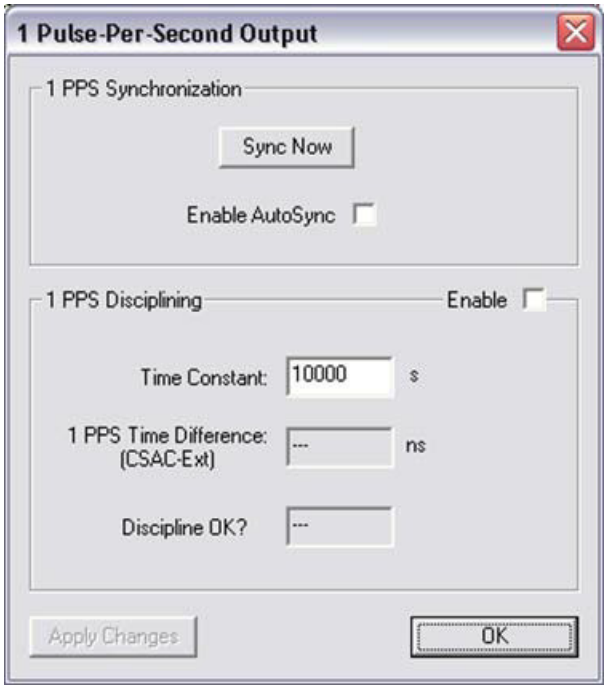
3.3.7.1 Manual Synchronization

In Manual Synchronization mode (default), the CSAC ignores any signal present on the 1 PPS input line (Pin 9) until commanded via RS232. When a synchronization command is received (see "1 PPS Synchronization (S)" on page 29), the CSAC 1 PPS is synchronized to the next rising edge to appear on Pin 9.

This mode is applicable to configurations where the CSAC is embedded in a system where a 1 PPS signal is always present, but not always reliably accurate or stable (such as a GPS receiver). The host microprocessor may command the CSAC to synchronize after it has verified the state-of-health of the 1 PPS reference source (for example: after querying lock state of the GPS receiver.

To perform manual synchronization from CSACdemo, open the 1 PPS… panel from the View menu. The 1 PPS panel is shown in Figure 7.

Figure 7 • **CSACdemo 1 Pulse-Per-Second Output Panel**



To manually synchronize the CSAC from CSACdemo, make sure that a valid 1 PPS reference is connected to the 1 PPS reference input and click **Sync Now** on the 1 PPS panel. The CSAC synchronizes to the next rising edge detected on the 1 PPS reference input.

3.3.7.2 Automatic Synchronization

In Automatic Synchronization mode, the CSAC synchronizes its 1 PPS output to every rising edge that appears on Pin 9. In this mode, synchronization may be performed by connecting a reference 1 PPS signal to Pin 9 without needing to issue the RS232 synchronization command. Automatic synchronization can be enabled/disabled via bit 3 (0x0008) in the Mode Register (see "Set/clear Operating Modes (M)" on page 28).

This mode can be useful, for example, in cases where the host system does not communicate with the CSAC or in which the host system has no method or need to determine the state-of-health of the reference source.

Note: Automatic Synchronization mode and Disciplining mode (see 1 PPS Disciplining) are mutually exclusive. Enabling either in the Mode register disables the other.

To enable Automatic Synchronization from CSACdemo, select the **Enable Autosync** checkbox on the 1 PPS panel and click **Apply Changes** (see Figure 7 on page 16).

3.3.8 1 PPS Disciplining

A high-resolution phase meter is implemented within the CSAC for improved synchronization (< 100 ns) as well as for frequency calibration of the CSAC. The phase meter measures the time difference between the internal CSAC 1 PPS (Pin 10) and the externally applied reference 1 PPS (Pin 9). The phase meter measures the relative phase between the CSAC and the reference once per second with a resolution of 450 ps.

Based on the measurements of the phase meter, internal steering algorithms adjust the frequency of the CSAC's microwave synthesizer so as to simultaneously steer both the phase and frequency to that of the external reference, ultimately achieving accuracies of < 5 ns and 5 $pp10^{13}$, respectively.

Disciplining can be enabled/disabled via bit 4 (0x0010) in the Mode Register (see "Set/clear Operating Modes (M)" on page 28). The time constant of the steering algorithm is user selectable via the ID command (see "Set 1 PPS Disciplining Time Constant (D)" on page 29).

Note: Both mode setting and time constant are non-volatile, that is, preserved across power cycles.

Prior to the onset of steering, the disciplining algorithms first perform an initialization sequence in which the variables of the steering algorithm are reset to defaults and a 1 PPS synchronization operation (see "1 PPS Synchronization (S)" on page 29) is executed to bring the 1 PPS output within 100 ns of the reference, thereby avoiding large frequency excursions. Initialization is performed when Disciplining is first enabled in the Mode Register and, in the case where Disciplining is already enabled after the CSAC achieves frequency lock (BITE = 0, status = 0).

In the event that the 1 PPS reference is removed from Pin 9 while Disciplining, the CSAC remains in holdover and preserves the most recent steering value. If the 1 PPS reference subsequently reappears, Disciplining continues where it left off, without reinitializing. The notable exception to this is the case in which the CSAC 1 PPS has drifted significantly in phase (> 1 µs) from the reference 1 PPS during the outage. In this case a synchronization is performed, though the Disciplining variables are not reinitialized.

If it is necessary to force re-initialization of the disciplining variables, perhaps because the reference source is subsequently deemed untrustworthy and subsequently recovers, this can be accomplished by disabling and re-enabling Disciplining in the Mode Register (see "Set/clear Operating Modes (M)" on page 28).

When Disciplining is enabled, the most recent phase meter measurement, rounded to the nearest nanosecond, is reported in the standard telemetry (see "Telemetry (6 and ^)" on page 25). The sign of the reported value reflects the measurement of (1PPS_EXT - 1PPS_CSAC), that is if the CSAC 1PPS rising edge occurs after the external 1PPS rising edge, then the sign is negative.

The status of Disciplining is indicated by the DiscOK parameter in the telemetry. DiscOK = 0 upon startup. DiscOK = 1 when magnitude of phase measurement is less than phase threshold (see "Set 1 PPS Phase Threshold for Discipline Status OK Check (m)" on page 31) for two time constants of duration. DiscOK = 2 when in holdover (disciplining enabled but no 1 PPS present).

Note: Automatic Synchronization mode (see "Automatic Synchronization" on page 17) and Disciplining mode are mutually exclusive. Enabling either in the Mode register disables the other.

In CSACdemo, enabling/disabling Disciplining and setting the discipline time constant are both accomplished on the 1 PPS panel, accessible from the View menu (See Figure 7 on page 16). To modify the discipline time constant, enter the new value in the field (10 - 10000) and click **Apply Changes**.

3.3.8.1 Cable length Compensation

The zero point of disciplining can be adjusted to accommodate cable and other instrumentation delays (or advances) which impact the arrival time of the 1 PPS at the CSAC 1 PPS input pin. The compensation value can optionally be stored in the CSAC non-volatile RAM for one-time calibration.

The maximum compensation adjustment is +/- 100 ns, with resolution of 100 ps. The compensation value is entered into the CSAC as a signed integer in units of 100 ps, where positive sign indicates phase advancement of the input 1 PPS. For example, if there is 45 ns of delay (approximately 33 feet of RG-58 coaxial cable) between the on-time point and the CSAC 1 PPS input then the compensation value would be +450.

Note: Cable length compensation can also be employed to correct for dynamic known errors in the 1 PPS reference provided, for example, from an external measurement system. For this reason, upon application the compensation is subsequently applied to the previous 1 PPS measurement.

Note: Compensation is implemented in the disciplining algorithm, not in the phase measurement itself. The phase measurement, as reported via telemetry, reports the actual phase measurement, that is, if the CSAC is disciplined with +50 ns of compensation, the phase meter reports -50 ns of phase error.

Compensation is set with the `!DC` command (see "Set 1 PPS Disciplining Cable Length Compensation (DC)" on page 29)

3.3.9 Time-of-day

The CSAC maintains time-of-day (TOD) as a 32-bit unsigned integer, which is incremented synchronously with the rising edge of the 1 PPS output. Until set otherwise, TOD begins counting from zero when the CSAC is powered on.

TOD is retrieved from the CSAC over RS232 with the `!T?` command (see Time-of-day). When the `!T?` command is received, the CSAC waits for the next rising edge of 1 PPS before replying with the TOD of the current epoch, that is, if the command is received during epoch N, then the reply N+1 appears immediately following the next 1 PPS. This strategy provides the host system with minimum ambiguity in interpreting the response.

TOD can be set with the `!T` command via the RS232 interface. The `!T` command includes provision both for setting an absolute number or for a differential (+/-) adjustment of the present TOD. An example is provided in Time-of-day section. To avoid ambiguity in setting the TOD, it is recommended that the host system wait for 1 PPS and transmit the setting/adjustment immediately thereafter.

The CSACdemo program shows TOD on the Time-Of-Day… panel, accessed from the View menu (see Figure 8).

Figure 8 • **CSACdemo Time-Of-Day panel**

The raw CSAC TOD value is shown in the lower field of the panel (here 1260881710). The upper display of the TOD panel realizes the time-keeping convention of the C Programming language (in UNIX and Microsoft Windows), which counts time in seconds from midnight on January 1, 1970. Upon clicking **Send**, it sets the CSAC time according to the host PC's TOD counter (either local time or UTC depending on the setting of the pull-down menu to the left of the **Send**). The + and - buttons for hours and seconds adjustment will increment or decrement the CSAC TOD by +/- 3600 or +/-1 second respectively.

3.3.10 Analog Tuning

To enable analog frequency tuning for implementation in legacy (quartz crystal) applications, the frequency of the CSAC can be tuned with an external voltage applied to Pin 1. This functionality can be enabled/disabled via a bit in the Mode Register (see "Set/clear Operating Modes (M)" on page 28). The applied voltage is digitized by an internal analog-to-digital converter and the correction is applied to the microwave synthesizer at a rate of once per second, that is, the maximum tuning rate is 1 Hz.

When analog tuning is enabled, the voltage applied at Pin 1 and the resultant steering are reported in the standard telemetry stream (see "Telemetry (6 and ^)" on page 25). The tuning voltage input range is 0 – 2.5 VDC, which corresponds to a full scale tuning range of 4.4 $pp10^8$. Nominal zero-correction tuning occurs at a tuning input voltage of 1250 mV. The fractional frequency correction, for a given applied voltage, is given by EQ 2.

$$\Delta f/f = (V_{tune} - 1250\ mV) \times 1.77 \times 10^{-11}\ /mV$$

EQ 2

Note: This formula is accurate for the standard (-001) SA.45s CSAC, operating at 10.0 MHz output frequency. Consult the datasheet for tuning curves of CSACs at alternate frequencies. The tuning input pin is nominally biased at ≈1250 mV, that is, approximately zero correction.

Note: Bias voltage may vary due to component variations and/or exhibit temperature sensitivity. Therefore, analog tuning should NOT be enabled unless the functionality is necessary and the analog tuning input pin is connected to a low noise, low impedance voltage source. For non-legacy applications, it is recommended that this feature remain disabled, and that corrections be applied via the digital communications interface (see "Frequency Steering" on page 14) to avoid degradation of the CSAC short-term stability due to voltage noise applied to the tuning pin.

Analog tuning can be enabled/disabled and monitored from the CSACdemo application from the Analog Tuning… panel (accessible from the View menu).

Figure 9 • **CSACdemo Analog Tuning panel**

When analog tuning is enabled, the voltage present on Pin 1 is displayed in the Analog Tuning field and also reflected in the current reported value of steer on the main panel. To enable or disable analog tuning, select **Enable Analog Tuning** checkbox and click **Apply Changes**.

3.3.11 Ultra-low Power Operating Mode

The majority of the power in the CSAC is consumed by the physics package and microwave synthesizer. In ultra-low power (ULP) mode, the physics package and synthesizer can be disabled for a user-specified length of time, during which the CSAC operates as a free-running TCXO. Periodically, the atomic clock portion of the CSAC is powered ON (again for a user-specified amount of time) and the TCXO is re-calibrated to the atomic frequency. Operating in this mode, the CSAC exhibits the short-term performance of a TCXO with good long-term stability at significantly lower power compared to standard mode. For example, if the atomic clock portion is only powered on for 5 minutes out of every hour (2 minutes for lock acquisition + 3 minutes of run time), then the time-averaged power of the CSAC may be < 30 mW.

Between calibration cycles, the CSAC in ULP mode exhibits the performance characteristics of a free-running TCXO and therefore exhibits significantly higher short-term frequency drift and environmental (temperature and vibration) sensitivity than a normally-operating CSAC. For this reason, ULP mode is principally recommended only for applications that:

- Require long-term timing performance, rather than short-term frequency or time stability.
- Have a very stable environment (temperature and vibration).

Warning: Due to the unique behavior and configurability of ULP, the datasheet performance specifications for the SA.45s CSAC cannot be guaranteed while in ULP mode. The CSAC has short-term drift performance of a low cost low performance TCXO. Contact Microsemi for additional assistance in evaluating and optimizing ULP for your specific application.

Figure 10 • **Frequency record of CSAC in ULP mode.**

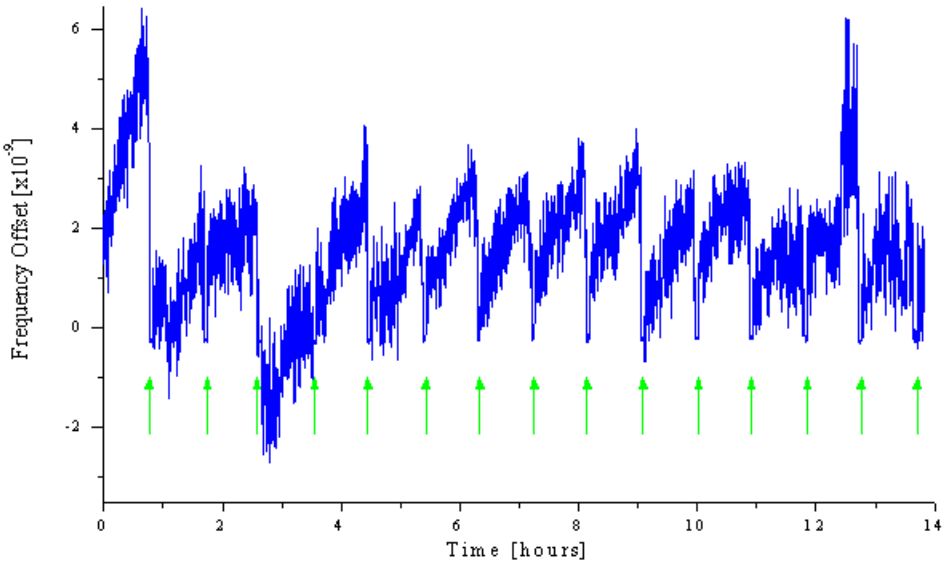


Figure 10 shows an example of a CSAC operating in ULP mode, with wake-time = 300 s (5 min) and sleep-time = 3300 s (55 min). The green arrows indicate the on time calibrations. Note the relatively poor TCXO drift and temperature behavior between calibrations.

ULP is an unusual operating mode for an atomic clock and it is important for the user to understand exactly how the clock is behaving to effectively implement this feature in a system. In particular, note the following:

- When operating in ULP mode, the Status Register indicates Status = 9 (asleep) when the atomic clock portion of the CSAC is asleep. Each wake cycle is indicated by the usual lock process (Status = 8, 7, 6, …) followed by wake-time seconds of operation at Status = 0 before the cycle repeats. This cycle is also reflected on the BITE pin, which is 1 (high) whenever the CSAC is unlocked (or asleep) and only 0 (low) during the locked periods.
- When using Disciplining (see "1 PPS Disciplining" on page 17) in conjunction with ULP, disciplining functionality is disabled during sleep and unlocked cycles, though steering information is preserved and updated across wake cycles.
- Frequency Steering commands may be entered when the CSAC is asleep or unlocked but do not affect the output frequency until lock is achieved, typically on the next wake cycle (see "Frequency Steering" on page 14). Also, the Latch command is only valid when the CSAC is locked (Status = 0).
- If enabled, Analog Tuning (see "Analog Tuning" on page 19) is only active during wake cycles.

ULP is enabled via bit 5 (0x0020) in the Mode Register (see "Set/clear Operating Modes (M)" on page 28) and the sleep-time and wake-time are set via the `!U` command (see "Set Ultra-low Power Mode Parameters (U)" on page 30). These values are non-volatile; they persist across power cycles. Note that the wake-time begins counting after the CSAC achieves lock, so the actual time that the atomic clock portion of the CSAC is powered on is the sum of the time to lock and the user-configured wake-time. The minimum allowed values of wake-time and sleep-time are 10 seconds and 1800 seconds, respectively.

To configure ULP parameters via CSACdemo, select **Ultra-Low Power Mode** from the View menu to access the panel shown in Figure 11.

Figure 11 • **CSACdemo Ultra-Low Power Mode Configuration Panel**

Enter the desired settings and click **Apply Changes** to upload new settings to the CSAC.

3.3.12 1 PPS Phase Measurement Mode

For firmware versions 1.08 and later, an additional phase meter is implemented with extended range (+/- 500 ms) to measure the time difference between the internal CSAC 1 PPS (Pin 10) and the externally applied reference 1 PPS (Pin 9). Measurement resolution is approximately 100 ns.

Note: 1 PPS phase measurement mode utilizes both the extended-range phase meter and the high- resolution phase meter (450 ps resolution) used in 1 PPS Disciplining (see "1 PPS Disciplining" on page 17). In this mode, the phase measured by the high-resolution meter is reported if phase is in the range +/- 1 µs (approximate), otherwise the extended-range meter is reported.

Phase measurement mode may be enabled/disabled via bit 2 (0x0004) in the Mode Register (see "Set/clear Operating Modes (M)" on page 28). Phase Measurement mode, Automatic Synchronization and Disciplining are all mutually exclusive, so enabling a 1 PPS-related option in the Mode register disables the other 1 PPS-related options.

3.4 Programmers Reference

Pins 5 and 6 provide a serial interface for communication with the CSAC. The protocol is fundamentally similar to RS232, with the exception that the voltage levels are CMOS (0-VCC), rather than +/- 12 V.

The data rate and word structures are:

- 57,600 Baud
- 8 data bits
- No Parity
- 1 Stop Bit (8-N-1)
- No flow control

For interfacing with a standard RS232 controller interface, which requires +/- 12 V logic levels, an external level shifter must be employed, such as the Maxim MAX202 employed on the Evaluation Board (see "Notes on the Evaluation Board" on page 41).

3.4.1 Overview of Telemetry Interface

The CSAC communicates exclusively with printable (non-binary) ascii characters.

In general, commands are to be preceded by an exclamation point (`!`) and followed by a carriage-return/linefeed [CRLF] pair (ascii 0x0D 0x0A). For convenience and efficiency, most commands also provide a single-character shortcut, which is executed immediately, that is without bracketing by `!` and [CRLF]. For example, the single character shortcut `^` is functionally identical to `!^[CRLF]`.

After transmitting `!` but prior to sending [CRLF], a command may be aborted by sending the escape character (ASCII 0x1B).

All commands produce a response from the CSAC, which are human readable, with individual lines ending in [CRLF]. If an unsupported or improperly formatted command is received, the CSAC responds with `?[CRLF]`.

3.4.1.1 Checksum (error-checking option for telemetry interface communications)

For improved communications reliability, an NMEA-style checksum may be enabled via bit 6 (0x0040) of the Mode Register (see "Set/clear Operating Modes (M)" on page 28). When enabled, the checksum is required for all input commands and is present on all replies from the CSAC.

The checksum is a two-byte ASCII representation (in hexadecimal) of the XOR of all characters in the command between - but not including - the `!` and the [CRLF] characters. The checksum is preceded by a * character and appended to the command immediately prior to the [CRLF]. Because commands including checksum are inherently multi-character, single-character shortcuts are not available when checksum is enabled.

Example (Enable analog tuning via Mode register):

Command: `!MA*0C[CRLF]`

Unit Response: `0x0041*4D[CRLF]`

Example (Disable checksum via Mode register):

Command: `!Mc*2E[CRLF]`

Unit Response: `0x0000[CRLF]`

If the checksum is not present or if the checksum value is invalid, then the command is not executed and the CSAC responds with *[CRLF].

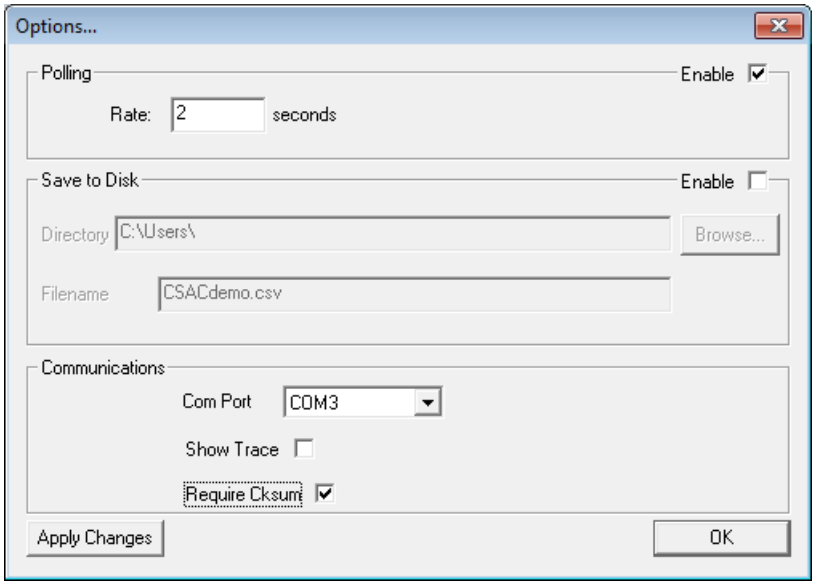
Example (Malformed checksum):

Command: `!Mc*2D[CRLF]`

Unit Response: `*[CRLF]`

To experiment with checksum in CSACdemo and observe the calculated checksums in the Trace window, select **Require Cksum** checkbox on the **Options…** panel (see Figure 12).

Figure 12 • **CSACdemo Options… Panel**



3.4.2 Command Summary

Table 4 summarizes the CSAC commands.

Note: The `m` and `>` commands are only available for firmware versions 1.08 and later.

Table 4 • **Command Summary**

Shortcut	Description	Command	Reference Section
`6`	Return telemetry headers as comma-delimited string	`!6[CRLF]`	"Telemetry (6 and ^)" section on page 25
`^`	Return telemetry as comma-delimited string	`!^ [CRLF]`	"Telemetry (6 and ^)" section on page 25
`F`	Adjust frequency	`!F?[CRLF]`	"Frequency Adjustment (F)" section on page 27
`M`	Set operating mode register bits	`!M?[CRLF]`	"Set/clear Operating Modes (M)" section on page 28
`S`	Sync CSAC 1 PPS to external 1 PPS	`!S[CRLF]`	"1 PPS Synchronization (S)" section on page 29
`D`	Set 1 PPS disciplining time constant	`!D?[CRLF]`	"Set 1 PPS Disciplining Time Constant (D)" section on page 29
`U`	Set ultra-low power mode parameters	`!U?[CRLF]`	"Set Ultra-low Power Mode Parameters (U)" section on page 30
`T`	Set/report time-of-day	`!T?[CRLF]`	"Time-of-Day (TOD)" section on page 30

Table 4 • **Command Summary**

Shortcut	Description	Command	Reference Section
m	Set 1PPS Phase Threshold for Discipline Status OK Check	!m?[CRLF]	"Set 1 PPS Phase Threshold for Discipline Status OK Check (m)" section on page 31
>	Set 1PPS Out Pulse Width as multiple of default width	!>?[CRLF]	"Set 1 PPS Out Pulse Width as an integer multiple of default Width (>)" section on page 31
@	Deferred Command	!@?[CRLF]	"Deferred Command (@)" section on page 32
?	Help	!?[CRLF]	"Help (?)" section on page 32

3.4.3 Detailed Command Descriptions

3.4.3.1 Telemetry (6 and ^)

CSAC supports two commands, !6 and !^ to retrieve the telemetry headers and values, respectively. Both responses are comma-delimited strings, suitable for importing into spreadsheet programs.

Example:

Telemetry headers command: !6[CRLF]

Unit Response:
Status,Alarm,SN,Mode,Contrast,LaserI,TCXO,HeatP,Sig,Temp,Steer,ATune,Phase,DiscOK,TOD,LTime,Ver[CRLF]

Example:

Telemetry data command:!^[CRLF]

Unit Response: 0,0x0000,1209CS00909,0x0010,4381,0.86,1.573,17.62,0.996,28.26,-24,---,-1,1,1268126502,586969,1.0[CRLF]

Note: The single-characters 6 and ^ are shortcuts for !6[CRLF] and !^[CRLF], respectively.

Table 5 lists the telemetry parameters and their associated header identifiers.

Table 5 • **Telemetry Parameters**

Identifier	Description	Notes
Status	Unit Status	See Note 1 and Table 6 on page 26
Alarm	Pending Unit Alarms	See Note 2 and Table 7 on page 26
SN	Unit serial number	See Note 3
Mode	Mode of operation	See Table 8 on page 28.
Contrast	Indication of signal level	Typically > 2000 when locked, and ≈ 0 when unlocked.
LaserI	Laser current (mA)	Typically 0.6 - 1.3 mA
TCXO	Tuning Voltage (V)	0 - 2.5 VDC tuning range ≈ ±10 $pp10^6$
HeatP	Physics package Heater Power (mW)	Typical 6 - 20 mW under normal operating conditions and 25°C ambient
Sig	DC Signal Level (V)	Typical 0.8 - 1.7 V under normal operating conditions
Temp	Unit temperature (°C)	Absolute accuracy is +/- 2°C

Table 5 • **Telemetry Parameters *(continued)***

Identifier	Description	Notes
Steer	Frequency adjust	In $pp10^{12}$
ATune	Analog tuning voltage input	--- when analog tuning is disabled, 0 - 2.5 V when enabled
Phase	Difference between CSAC and External 1PPS (ns)	Only present if discipline or phase-measure mode enabled, otherwise **---** or NEEDREFPPS
DiscOK	Discipline status (0-2)	0 = acquiring, 1 = locked, 2 = holdover when disciplining enabled, otherwise **---**
TOD	Time (seconds)	Starts at 0 upon power up unless set by command
LockT	Time since lock (seconds)	Starts at 0 upon lock
FWver	Firmware version	Two digit number M.m where M is major revision and m is minor revision.

Notes:

1. Status reflects the steps of the clock initialization process. It starts at 8 on boot and decreases to 0 as acquisition proceeds. When Status ≠ 0, BITE = 1. When Status = 0, BITE = 0.
2. Alarms indicate detection of anomalous operating conditions while locked. Alarm is the logical OR of all pending alarms (see Table 7). If any alarm is tripped (Alarm ≠ 0x000), the CSAC returns to Status = 8.
3. CSAC serial numbers are of the form YYMMCSXXXXX where YYMM is the year and month of production and XXXXX is the serialized production unit number.

Table 6 • **Status Codes of CSAC**

Status	Acquisition Stage
9	Asleep (ULP mode only)
8	Initial warm-up
7	Heater equilibration
6	Microwave power acquisition
5	Laser current acquisition
4	Laser power acquisition
3	Microwave frequency acquisition
2	Microwave frequency stabilization
1	Microwave frequency steering
0	Locked

Note: If CSAC returns a status code other than shown in Table 6, then it is re-acquiring its set points. In this case, warm-up time takes longer than stated on the *SA.45s datasheet*. To avoid this, it is recommended to always allow CSAC to remain powered on for >102s after it acquires LOCK. 102s is the minimum amount of time necessary to save CSAC set points to memory, thus avoiding set-point re-acquisition upon its next power up.

Table 7 • **Alarm Codes of CSAC**

Alarm	Definition	Alarm Limit
0x0001	Signal contrast low	Contrast < 1000
0x0002	Synthesizer tuning at limit	Synthesizer detuned from calibration by > +30 kHz or < -15 kHz
0x0004	Temperature bridge unbalanced	Bridge - Set-point > +/- 20 mV

Table 7 • **Alarm Codes of CSAC *(continued)***

Alarm	Definition	Alarm Limit
0x0010	DC light level low	Set-point - DCL > 1.5V
0x0020	DC light level high	DCL - Set-point > 1.5V
0x0040	Heater voltage low	< 30 mV
0x0080	Heater voltage high	> 2.48 V
0x0100	µW power control low	< 20 mV
0x0200	µW power control high	> 2.48 V
0x0400	TCXO control voltage low	< 0.1 V
0x0800	TCXO control voltage high	> 2.4 V
0x1000	Laser current low	< 0.5 mA
0x2000	Laser current high	> 2.3 mA
0x4000	Stack overflow (firmware error)	–

3.4.3.2 Frequency Adjustment (F)

The output frequency of the CSAC may be adjusted (steered) via RS232. The internal resolution of the fractional frequency correction is approximately 1 $pp10^{12}$. The correction is entered as integer $pp10^{15}$. The maximum allowed correction, in a single command, is ±20000000 (2 $pp10^{8}$). Corrections may be applied as either Absolute or Relative, depending on the first character following the `!F`, that is `!FA` or `!FD` for absolute or relative (delta) respectively. In the case of absolute steering, the value of the Steer register is replaced with the new value. In the case of relative (delta) steering, the new value is summed with the existing value in the Steer register, that is two relative corrections of -10000 result in a total offset of -2 $pp10^{11}$. The current steering value is reported in the Steer field of the telemetry in units of $pp10^{12}$.

The format for the Adjust frequency command is: `!FYXXXXX[CRLF]`

where Y is either A or D and XXXXX is the new correction in $pp10^{15}$.

Example (Apply absolute tuning correction of -1.23 $pp10^{10}$):

Command: `!FA-123000[CRLF]`

Unit Response:Steer = `-123[CRLF]`

Example (Apply delta tuning correction of -1.23 $pp10^{10}$):

Command: `!FD-123000[CRLF]`

Unit Response:Steer = `-246[CRLF]`

Example (Report current value of steer):

Command: `!F?[CRLF]`

Unit Response:Steer = `-246[CRLF]`

Note: That the single-character `F` is a shortcut for `!F?[CRLF]`.

The contents of the Steer register are volatile, that is the Steer is reset to 0 when power is cycled to the CSAC. In many cases it is desirable to preserve the steer upon power-down, for example calibration of the CSAC. This is accomplished by sending a Frequency Latch command to the CSAC, which updates the internal calibration (stored in non-volatile memory) according to the current value of the Steer register and resets Steer to zero. Note that the Latch command is only valid when the CSAC is locked (Status = 0).

Example:

Command: `!FL[CRLF]`

Unit Response:`Steer Latched [CRLF] Steer = 0[CRLF]`

Warning: The frequency steering command (`!F`) is recommended for real-time disciplining of CSACs, but the value should NOT be latched (`!FL`) on every steer due to the physical limit on the number of times the non-volatile memory may be written before damage (10,000). For example, if an `!FL` command was applied to the CSAC, accompanying a steer (`!F`), at a rate of 1/sec, the CSAC is expected to fail within 4 hours.

3.4.3.3 Set/clear Operating Modes (M)

Operating modes of the CSAC are enabled/disabled via individual bits in the Mode register. The `!M` command provides access to set/clear each of the bits independently. The Mode register is non-volatile; settings persist across power cycles.

The unit responds by reporting the current value of the mode register in hexadecimal. Each bit in the mode register is associated with enabling/disabling a particular operating mode. The bit assignments are shown in Table 8.

Table 8 • **Operating Modes of CSAC**

Enable Bit Assignment	Enable Argument to !M_	Definition	Disable Argument to !M_
0x0001	A	Analog tuning	a
0x0002		Reserved	-
0x0004	M	1 PPS phase measurement (only available on firmware versions 1.08 and later)	m
0x0008	S	1 PPS auto-sync	s
0x0010	D	Discipline	d
0x0020	U	Ultra-low power mode	u
0x0040	C	Require checksum on ! command	c
0x0080	-	Reserved	-
-	?	Report Current Settings	-

Example (Enable and then Disable analog tuning):

Command: `!MA[CRLF]`

Unit Response: `0x0001[CRLF]`

Command: `!Ma[CRLF]`

Unit Response: `0x0000[CRLF]`

The current value of the mode register is returned in the standard telemetry query (see "Telemetry (6 and ^)" on page 25) or may be queried independently with the `!M?` command.

Example (query Mode register):

Command: `!M?[CRLF]`

Response: `0x0001[CRLF]`

Note: That the single-character `M` is a shortcut for `!M?[CRLF]`.

Autosync mode, discipline mode and Phase measurement mode (if mode available in the firmware version) are mutually exclusive. Setting a 1PPS-related option automatically disables the other 1 PPS-related options.

3.4.3.4 1 PPS Synchronization (S)

To synchronize the 1 PPS output (Pin 10) to an externally applied 1 PPS synchronization input (Pin 9), connect the external 1 PPS signal to Pin 9 and send the `!S` command. The rising edge of the 1 PPS output will synchronize to within +/- 100 ns (approximately) of the next rising edge of the 1 PPS input. If a valid 1 PPS input does not appear at the 1 PPS input within 3 seconds, the operation is aborted and an error is returned.

Example (Synchronize 1PPS):

Command: `!S[CRLF]`

Unit Response: `S[CRLF]`

or: `E[CRLF]`

The unit response (S or E) occurs after either successful synchronization or 3-second timeout. This permits the host system to verify successful synchronization.

Note: The single-character S is a shortcut for `!S[CRLF]`.

3.4.3.5 Set 1 PPS Disciplining Time Constant (D)

The time constant for disciplining to an externally-supplied 1 PPS reference source may be selected to provide optimal performance in a given application (see "The Art of Disciplining" on page 38).

The time constant can range between 10 to 10000 seconds. The 1 PPS disciplining time constant is set with the `!D` command. The format for setting the time constant is: `!DX[CRLF]`

where X is the new time constant in seconds.

Example (set disciplining time constant to 80 seconds):

Command: `!D80[CRLF]`

Response: `80[CRLF]`

To query the current time constant setting, without modifying the value, use the command `!D?`

Example (query current disciplining time constant):

Command: `!D?[CRLF]`

Response: `80[CRLF]`

Note: The single-character `D` is a shortcut for `!D?[CRLF]`.

3.4.3.6 Set 1 PPS Disciplining Cable Length Compensation (DC)

Cable length compensation can be applied to allow for known delay (or advance) in the arrival time of the reference 1 PPS at the CSAC (see "Cable length Compensation" on page 18). Cable length compensation is represented as a signed integer in units of 100 ps, with a maximum value of +/- 1000 (100 ns).

The sign of the compensation is such that a positive value reflects known DELAY in the arrival time of the 1 PPS. For instance, 33 feet of RG-58 cable requires compensation of +45 ns.

The format for setting the cable length compensation value is: `!DCX[CRLF]`

where X is the new compensation value.

Example (set cable length compensation to +15 nanoseconds):

Command: `!DC150[CRLF]`

Response: `150[CRLF]`

To query the current compensation setting, without modifying the value, use the command `!DC?`

Example (query current compensation setting):

Command: `!DC?[CRLF]`

Response: `150[CRLF]`

To store the current compensation setting in non-volatile RAM, use the command `!DCL`

Example (Latch current value of compensation to power-up default):

Command: `!DCL[CRLF]`

Response: `Phase comp latched[CRLF]`

3.4.3.7 Set Ultra-low Power Mode Parameters (U)

Note: Placing the CSAC in ULP mode results in short-term drift performance of its internal TCXO.

The ultra-low power operating mode is defined by two parameters, Sleep-Time and Wake-Time, which may be set with the `!U` command in this format: `!USSS, WWW[CRLF]`

where SSS is the sleep time in seconds and WWW is the wake-time in seconds.

Example (set sleep-time = 55 minutes, wake-time = 5 minutes):

Command: `!U3300,300[CRLF]`

Response: `3300,300[CRLF]`

The allowed ranges of Sleep-time and Wake-time are 1800 – 65535 seconds and 10 – -65535 seconds, respectively.

To query the ULP settings, without modifying their values, use the command `!U?`.

Example (query current ULP settings):

Command: `!U?[CRLF]`

Response: `3300,300[CRLF]`

Note: The single-character `U` is a shortcut for `!U?[CRLF]`.

3.4.3.8 Time-of-Day (TOD)

TOD is maintained internally within the CSAC, represented by a single unsigned long integer value, which begins counting up from 0 when the CSAC is powered on. The TOD is synchronized with the 1 PPS output. TOD is routinely transmitted in the telemetry string (see "Telemetry (6 and ^)" on page 25).

TOD may be set externally with the `!T` command in this format: `!TYXXXX[CRLF]`

where Y is either A for absolute setting or D for a delta adjustment of TOD and XXXX is either the unsigned integer TOD (typically either UNIX/Windows time or GPS time) or a signed integer adjustment to the TOD.

Example (Absolute setting TOD to 1221578499):

Command: `!TA1221578499[CRLF]`

Unit Response: `TimeOfDay = 1221578499[CRLF]`

Example (retard TOD by 3600 seconds = 1 hour):

Command: `!TD-3600[CRLF]`

Unit Response: `TimeOfDay = 1221574902[CRLF]`

The TOD may be reported synchronous with the 1 PPS output:

Example (Retrieve TOD command):

Command: `!T?[CRLF]`

Unit Response: `XXXX[CRLF]`

where XXXX is the current TOD.

Note: This response does not occur until the next 1PPS output pulse.

When queried with the `!T?` command, the first character of TOD appears on RS232 within 20 ms of the rising edge of the next 1 PPS output pulse. Because this necessarily creates a delay of up to a second between sending the `!T?` command and receiving a response from the CSAC, the host system must allow for an RS232 receive timeout of at least 1000 ms when anticipating a response to the `!T?` command. For less critical timing applications, the TOD can be somewhat ambiguously parsed from the standard telemetry string (see "Telemetry (6 and ^)" on page 25).

Note: The single-character `T` is a shortcut for `!T?[CRLF]`.

3.4.3.9 Set 1 PPS Phase Threshold for Discipline Status OK Check (m)

The 1 PPS phase threshold (for discipline status OK check) when disciplining to an externally-supplied 1 PPS reference source may be configured to provide optimal performance in a given application.

For applications with a long disciplining time constant and a noisier 1PPS reference (such as GPS) there could be large variations in the reported 1 PPS phase of a CSAC disciplined ok (checked via ADEV measurement) but the phase threshold being set to a larger value ensures the DiscOK=1 indication is set correctly (see "1 PPS Disciplining" on page 17).

For applications with a short disciplining time constant the phase threshold can be set to a smaller value.

The range of 1PPS Phase Threshold for Discipline Status OK Check is 1 nanosecond to 10^9 nanoseconds (absolute values), with a default of 20 nanoseconds.

To set the phase threshold (for Discipline Status OK Check) the command has this format: `!mX[CRLF]`

where X is the new phase threshold's magnitude/absolute value in nanoseconds.

Example (set 1 PPS phase threshold for discipline status OK Check to +/-20 nanoseconds):

Command: `!m20[CRLF]`

Response: `20[CRLF]`

To query the 1 PPS phase threshold setting, without modifying the values, use the command `!m?`

Example (query current 1 PPS Phase Threshold setting):

Command: `!m?[CRLF]`

Response: `20[CRLF]`

Note: The single-character `m` is a shortcut for `!m?[CRLF]`.

3.4.3.10 Set 1 PPS Out Pulse Width as an integer multiple of default Width (>)

CSAC's 1 PPS output (Pin 10) has a default pulse width which may not be sufficiently long for certain applications. In such cases the pulse width can be set to an integer times the default pulse width by using the `!>` command with this format: `!>X[CRLF]`

where X is the unsigned integer used as a multiple of the default 1PPS Out Pulse Width to set the desired 1PPS Out's Pulse Width.

The allowed range of 1 PPS Out Pulse Width integer multiple of default Pulse Width is from 1 to 4.

Example (set 1PPS Out Pulse Width as a 2x multiple of default Pulse Width):

Command: `!>2[CRLF]`

Response: `PPS Pulse Width = 2 times ~100 usec [CRLF]`

Note: The default pulse width is dependent on the selected frequency option for RF output (pin 12).

When RF output frequency of 10 MHz (option 001) is selected then the 1 PPS out pulse width default is ~100 microseconds, while for other RF output frequency option's the 1 PPS out pulse width is as specified on the data sheet.

To query the 1 PPS Out Pulse Width setting, without modifying the values, use the command `!>?`.

Example (query current 1 PPS Out Pulse Width setting):

Command: `!>?[CRLF]`

Response: `PPS Pulse Width = 4 times ~100 usec[CRLF]`

Note: The single-character `>` is a shortcut for !>?[CRLF].

3.4.3.11 Deferred Command (@)

Any command can be sent at a deferred time by using the `!@` command with this format: `!T@XXXX,YYYY[CRLF]`

where XXXX is the deferred time in seconds and YYYY is the command that is sent after the deferred time.

Example (Defer sending the 6 command by 10 seconds):

Command: `!@10,6[CRLF]`

Unit Response: `Deferred = 10,6`

Unit Response (after 10 seconds):
`Status,Alarm,SN,Mode,Contrast,LaserI,TCXO,HeatP,Sig,Temp,Steer,ATune,Phase,DiscOK,TOD, LTime,Ver`

3.4.3.12 Help (?)

Table 9 lists all available commands in response to the ? command.

Table 9 • **Unit Response to Help command (?)**

`F-`	Adjust Frequency
`^-`	Telemetry
`6-`	Telemetry Headers
`D-`	Set 1PPS Discipline Tau
`S-`	Sync 1PPS
`U-`	Set parameters for ultra-low power mode
`M-`	Change Mode register
`T-`	Change/Report Time of Day
`?-`	Show this list
`@-`	Delayed Command Execution
`m-`	Set 1PPS Discipline Threshold for Phase in ns
`>-`	Set 1PPS out pulse width as 1-4 times default

For firmware versions 1.08 and later, the response also contains the above lines on `m` and `>` commands.

Note: The single-character `?` is a shortcut for `!?[CRLF]`.

3.5 Developers Kit

The CSAC Developer's Kit includes all of the necessary hardware, and cabling to facilitate validation of performance, brass-board demonstrations, and software interface development.

3.5.1 Package Contents

The Developer's Kit (Part # 990-00123-000) includes:

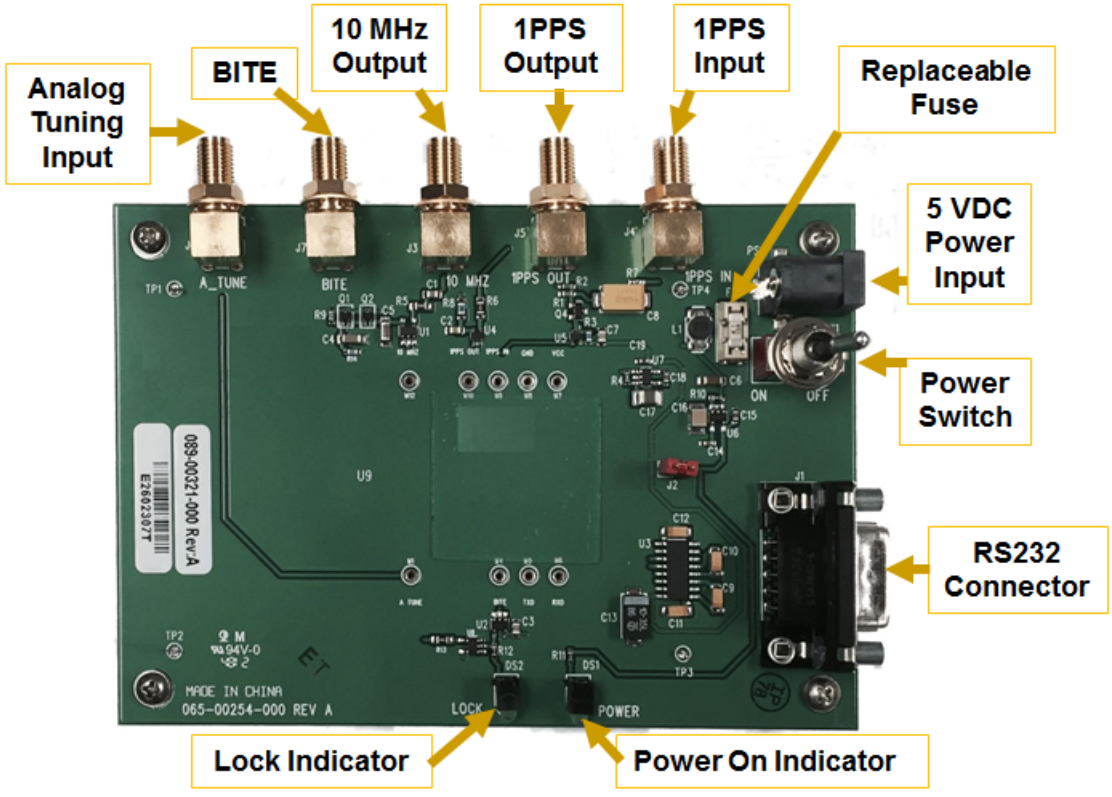
Table 10 • **Contents of CSAC Developer's Kit**

Item	Microsemi Part Number	Notes
Evaluation board	054-00279-000	"Notes on the Evaluation Board" on page 41
Power adapter	140-00041-000	5 VDC 5 mm center positive
RS232 cable	060-00322-000	–

3.5.2 Evaluation Board Overview

Detailed schematics of the evaluation board are provided at the end of this document under see "Notes on the Evaluation Board" on page 41. Figure 13 shows the connections to the evaluation board.

Figure 13 • **Evaluation Board Overview**



The Developer's Kit PCB and power supply consists of:

- **RF Output (SMA)** - The CSAC output is an RF, CMOS 0 – 3.3 VDC waveform. A high-speed buffer (U1) on the evaluation board converts the CMOS output to an AC-coupled output capable of delivering 10 dBm to a 50 Ω load.
- **3.3 VDC Jumper** - The evaluation board provides regulated 3.3 VDC to the CSAC. In order to allow convenient measurement of the CSAC power consumption, a jumper is provided in the Vcc connection to the CSAC. To measure the CSAC current draw, turn off the evaluation board and install a low-impedance current meter in place of the jumper. Observe proper ESD protocols in making this measurement.
- **Replaceable Fuse** - Littel fuse Part No. 0453 01.5
- **5 VDC Input** - Input power to the evaluation board is provided on a 5 mm (center positive) coaxial connector (PS1). To avoid damage to the test fixture, it is highly recommended to use only the power adapter provided by Microsemi with the Developer's Kit.
- **RS232 Connection (DB9M)** -The evaluation board provides a level shifter (U3), which converts the CSAC 0 – 3.3 VDC serial interface to the RS232 standard +/- 12 V for direct interface with a PC COM port. Connect the test fixture (J1) to a PC with a standard (non-Null) DB9F-DB9F RS232 cable. To avoid complication, use the proper cable which is provided by Microsemi with the Developer's Kit.
- **Lock Indicator LED** - Indicates normal operation following initial acquisition of the clock signal.

Note: This is the logical complement of the BITE output (CSAC PIN 4).

- **BITE (SMA)** - This is a buffered output from PIN 4 of the CSAC.
- **Power Switch** - Controls power to the evaluation board and to the CSAC.
- **Power LED** - Indicates the state of the power switch.
- **Analog Tuning Input (SMA)** - This input is directly connected to Pin 1 of the CSAC.
- **1 PPS Input (SMA)** - The 1 PPS input connection to the evaluation board accepts a 1 PPS reference of arbitrary amplitude (logic high: 2 V < Vin < 20 V) and generates a 0 – 3.3 V CMOS pulse to the CSAC.

Note: This input is capacitively coupled to the level-shifting circuit on the evaluation board (see Figure 20 on page 41) and therefore the applied pulse width must be < 10 ms in duration.

- **1 PPS Output (SMA)** - The 1 PPS output is buffered by a CMOS 0 – 3.3 V logic gate on the evaluation board.

3.5.3 Installing the CSAC on the Test Fixture

ESD Caution: To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the CSAC.

Remove the CSAC and evaluation board from their ESD protective bags only in an ESD-safe environment.

Note: The SA.45s pinout is keyed (see Table 2 on page 11) so the CSAC can only be inserted in the proper orientation. Gently insert the CSAC into the socket on the evaluation board.

3.5.4 Cabling

Connect the provided RS-232 cable between the evaluation board and the COM port on the PC. On laptops without an available COM port, a USB-to-RS232 adapter, such as National Instruments USB-232, can be used.

Make sure the power switch is OFF on the evaluation board, as shown in Figure 13 on page 33. Connect the 5 V power adapter between the 5 V power input and a 120 V AC wall outlet.

CSAC signal outputs are available from the evaluation board on connectors J3 (RF) and J5 (1 PPS). Connect either (or both) of these to your test equipment (frequency counter, spectrum analyzer, etc.).

3.5.5 CSACdemo Software Installation

The Microsemi CSACdemo software (Part # 084-00365-000) provides a convenient graphical user interface for monitoring and controlling the SA.45s CSAC. CSACdemo also is used for collecting and archiving monitor data from the CSAC. It can be installed and run on any PC running Microsoft Windows XP, Windows 7 or 10 and having at least one available RS232 (COM) port.

Note: Multiple CSACs can be monitored from a single PC, provided additional COM ports are available.

The software installation is available for download from the Microsemi website.

Upon accepting all of the default installation options (recommended), the CSACdemo software is installed in *c:\Program Files\Microsemi\CSAC*, a startup icon is added to the Start > All > Programs > Microsemi > CSAC menu, and a CSACdemo icon is placed on the desktop.

3.5.6 CSACdemo Operation

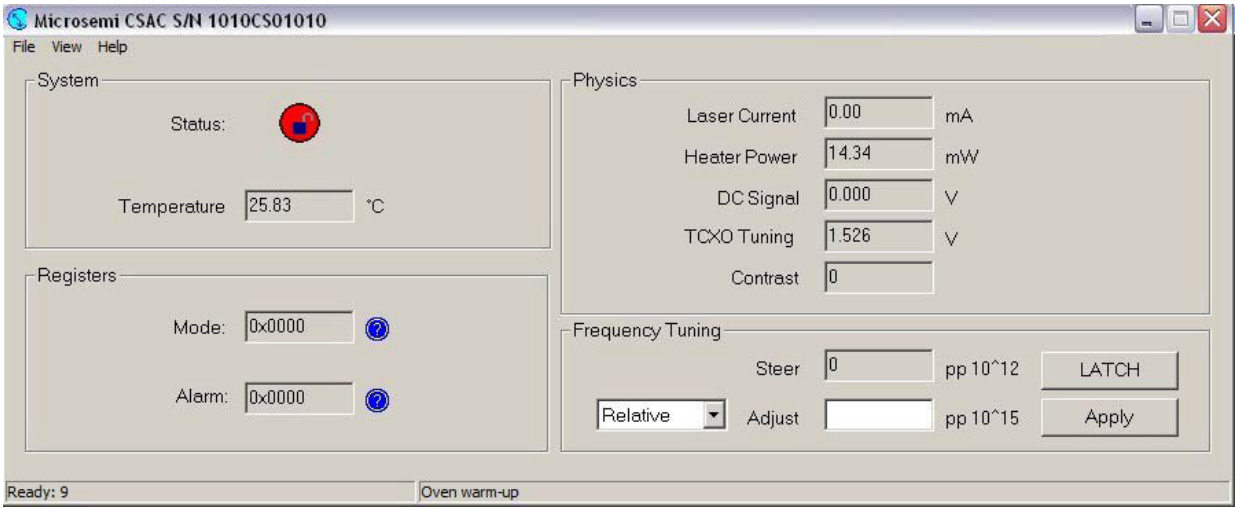
3.5.6.1 Initial Power-On

Connect power and RS232 to the Evaluation Board as described in Cabling. Turn ON the power switch on the Evaluation Board. Double-click the CSACdemo icon on the connected PC.

3.5.6.2 Establishing Communications

When communications are successfully established, the CSACdemo main window appears as shown in Figure 14.

Figure 14 • **CSACdemo Communicating with CSAC During Warm-up**



The title bar of the window indicates the unit serial number (here 1010CS01010). The main body of the window shows most of telemetry values from the unit (see "Telemetry (6 and ^)" on page 25). Initially, upon power-up, the status indicator the reflects CSAC's unlocked condition (BITE=1). The left field of the bottom status bar indicates the number of seconds until the next poll (here 9) and the right field indicates the unit status (here Oven Warm-up).

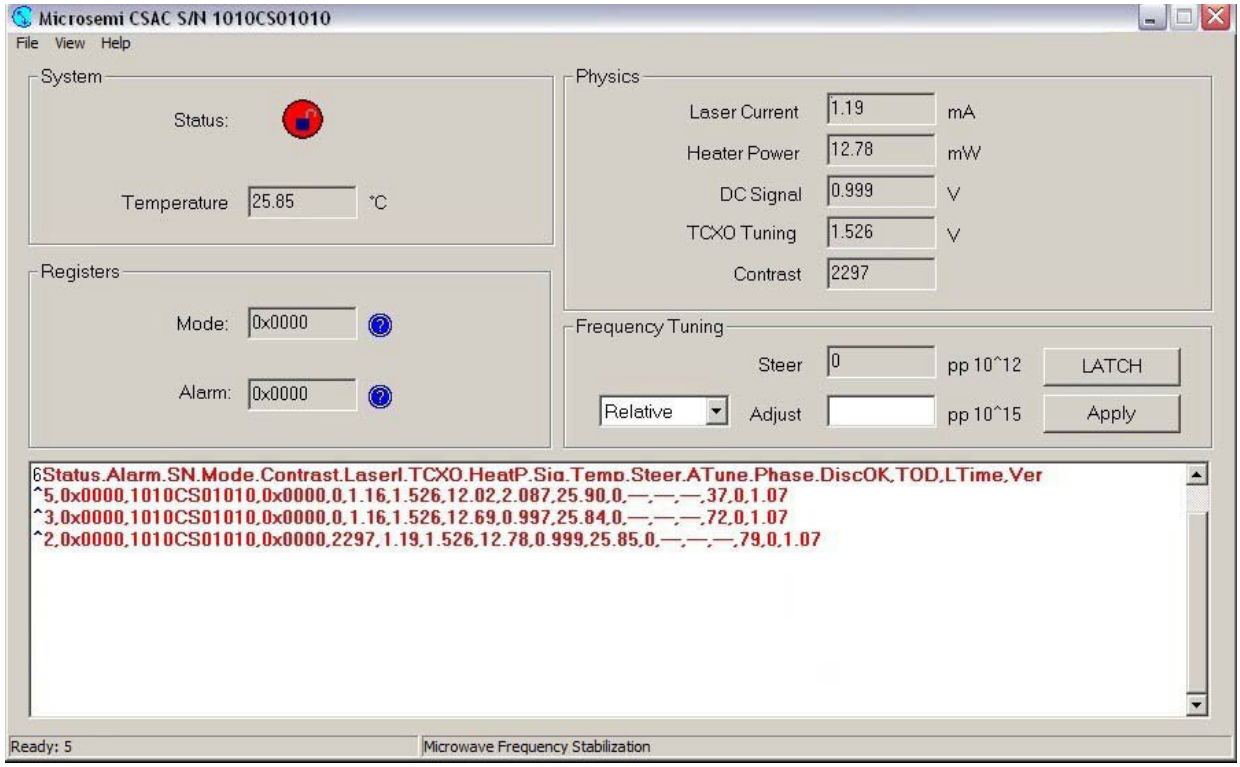
In the event of communication failure, the status indicator appears as . In this case, check the cabling and power supply. The bottom left status bar may also indicate the source of the communication failure. If the COM port is in use by another application, the status bar reports RS232 open failed, otherwise, it will likely indicate Instrument not responding. If you are using a PC serial port other than COM1, select Options… from the File… menu and select a different COM Port as shown in Figure 12 on page 24. Select the correct COM port from the pull-down menu and click **Apply Changes** to re-attempt communications.

3.5.6.3 Monitoring Communications

For development of application-specific embedded firmware for CSAC, it is helpful to observe the communications between the CSACdemo program and the CSAC. Enable the Show Trace checkbox in the Communications section of the Options… panel and click Apply Changes to view the bi-directional protocol.

With the trace visible, the CSACdemo main panel appears as shown in Figure 15.

Figure 15 • **CSACdemo Main Panel with Communications Trace Visible**



Note: Communications from the host PC to the CSAC are shown in blue and communications from the CSAC to the host are shown in red.

3.5.6.4 Observing Acquisition

Initially, when the CSAC is powered up, the LOCK LED on the evaluation board momentarily turns on then off once again. During acquisition the Unit Status field in the lower right corner of CSACdemo will proceed through the stages corresponding to the values of the Status register (see Table 6 on page 26: Status Codes).

Acquisition takes < 3 minutes in a 25°C ambient (up to a maximum of 5 minutes at -10°C). When acquisition is complete, the LOCK LED on the evaluation board illuminates, the CSACdemo right hand status bar indicates Locked, and the status indicator changes from changes from to .

After locked, the main panel of CSACdemo appears as shown in Figure 16.

Figure 16 • **CSACdemo in locked condition**

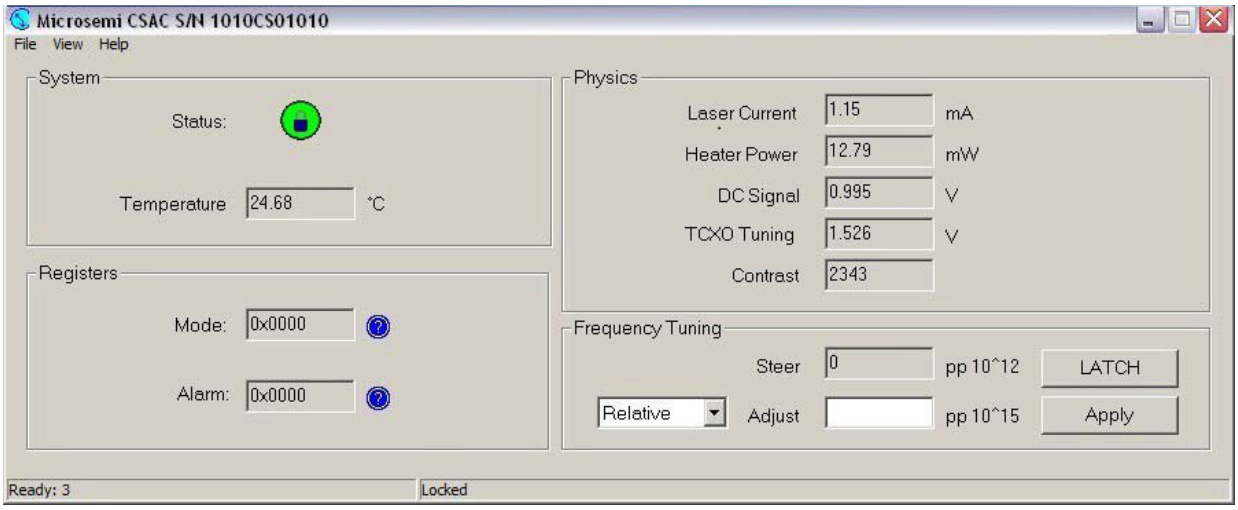


Figure 16 shows typical values for a normally operating CSAC. In this case, the internal case temperature of the CSAC is 24.86°C, the operating mode is 0x0000 (see "Set/clear Operating Modes (M)" on page 28) and there are no alarms. The physics package parameters in Figure 16 are fairly typical as well: The laser current is about 1.15 mA, the physics package heaters are drawing less than 25 mW, and the DC signal level is about 1 V. The TCXO tuning is mid-range on 0 – 2.5 V and the contrast is comfortably above 1000.

3.6 Data Acquisition with CSACdemo

For long-term monitoring of the CSAC, select the Options… panel from the File menu (see Figure 12 on page 24).

Choose a polling rate in seconds. For short-term (1 - 2 day) measurements, a polling rate of 10 seconds is optimal, and accumulates data onto disk at a rate of about 1 MB/day. For longer term measurements (30-100 days), a longer polling rate, such as 60 seconds, reduces the growth of the data file to 150 KB/day.

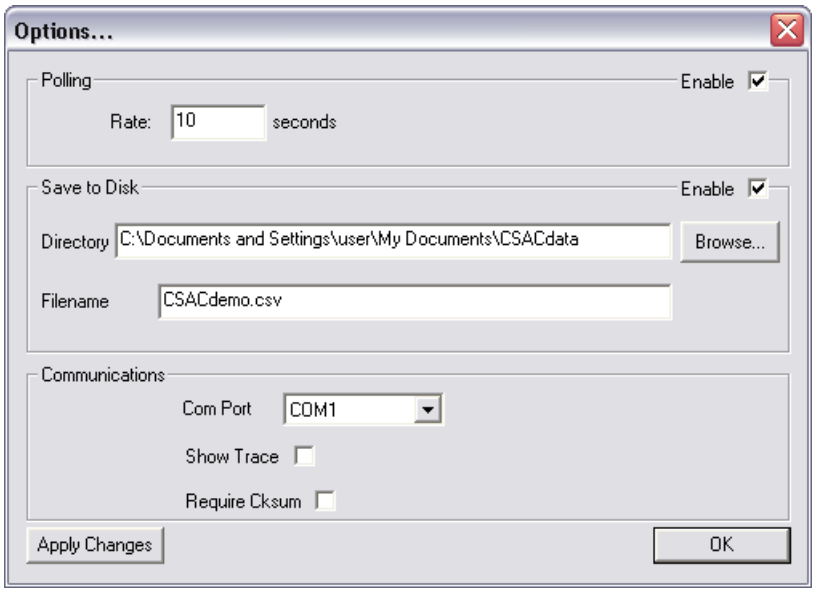
Enable **Save to Disk** with the checkbox in the top right of the panel.

Use the **Browse…** button to select an existing Directory to archive the CSAC data.

Note: You must have write permission to the selected directory. Type in a Filename for the data.

When you are finished, the panel looks like Figure 17.

Figure 17 • **CSACdemo Options for Datalogging to Disk**



Click **Apply Changes** to implement the new options or **OK** to discard changes and exit the panel.

The data is stored in ASCII comma-separated-values (CSV) format, which allows for convenient import into most popular spreadsheet and analysis software. The first line in the file contains the column headers (see "Telemetry (6 and ^)" on page 25). Subsequent lines contain the corresponding periodically-polled data. The first column in the file contains time stamps, derived from the host computer's clock, in mean-Julian day (MJD) format, referenced to universal coordinated time (UTC).

3.7 Design Guide

3.7.1 The Art of Disciplining

Implemented correctly, disciplining can be utilized to calibrate the CSAC frequency in the field, even if a reference source is only occasionally or sporadically available, thereby improving the long-term performance (phase and frequency drift) of the CSAC. At the same time, the disciplined CSAC may be used to clean-up the short-term stability of an accurate, but noisy, reference source, such as GPS.

Implemented incorrectly, disciplining may degrade the performance of the CSAC. For example, the CSAC disciplined with a short time constant to a source that is noisier than CSAC, such as GPS.

Implementing a successful disciplining strategy involves understanding the noise properties of the CSAC, the reference source, and the phase meter, and selecting the appropriate time constant that makes the best use of the available timing information.

Figure 18 • **Frequency Stability (Allan Deviation) versus Averaging Time (τ)**

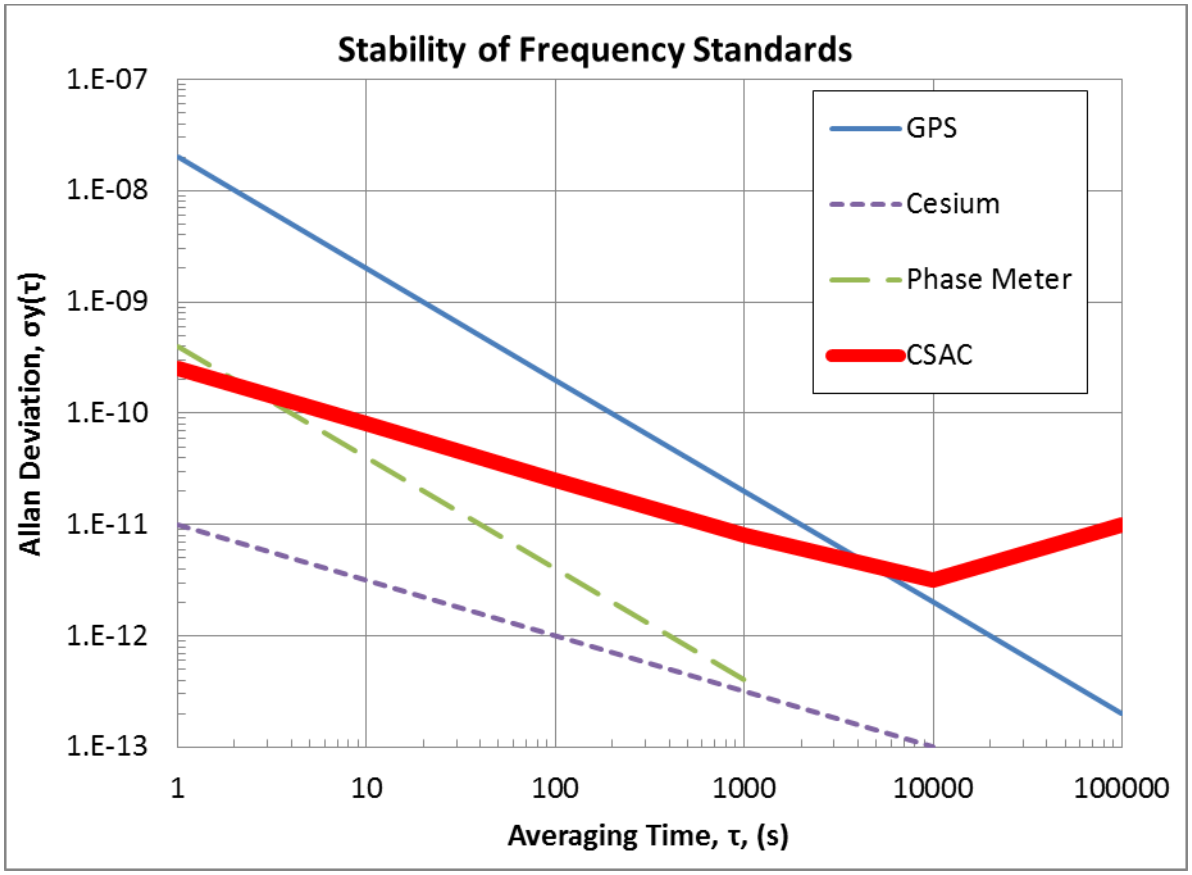
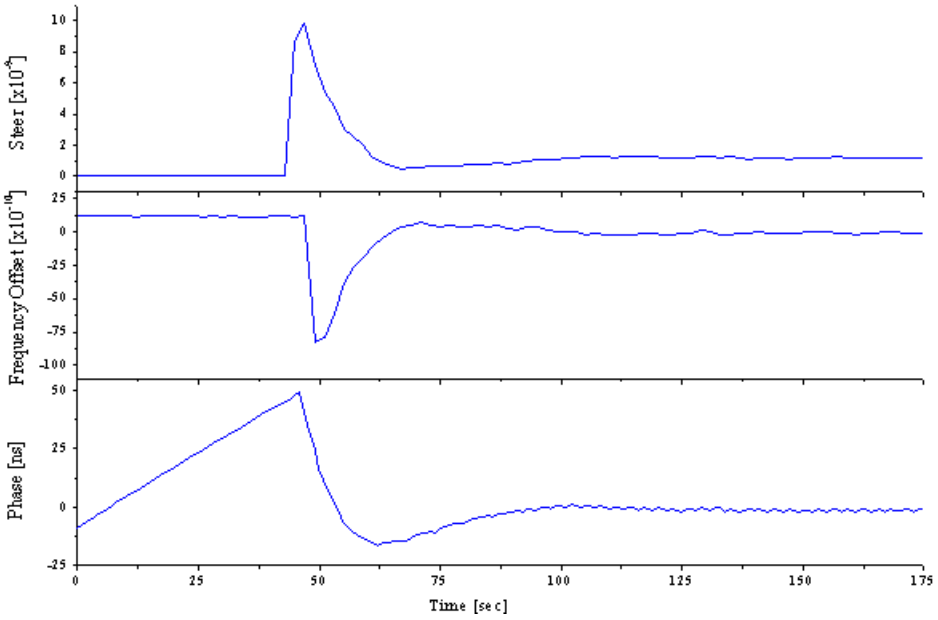


Figure 18 shows typical instability (Allan Deviation) of the CSAC (in red), along with the noise floor of the phase meter (in green). Also shown are the instabilities of typical reference sources, GPS (in blue) and a high-performance cesium beam frequency standard (in purple). When disciplining, the stability of the output of the CSAC (combined clock) at any averaging time, reflects the noise properties of the dominant (most noisy) source. For example, if disciplining the CSAC to a GPS source, which is noisier than the CSAC for averaging times $\tau < 5000$ seconds, the disciplining time constant should be set to $\tau > 5000$ seconds so that the (superior) CSAC stability dominates for $\tau < 5000$ seconds and the (superior) GPS stability dominates for $\tau > 5000$ seconds. On the other hand, consider the case where the CSAC is disciplined to a high-performance cesium clock, which is more stable than the CSAC on all time scales. The noise is dominated by the phase meter for $\tau < 2$ seconds and by the CSAC for $\tau > 2$ seconds. In this case, the disciplining time constant could be set to $\tau = 2$ seconds for optimal performance.

Figure 19 shows an example of a CSAC, which is disciplined to a superior reference (in this case a hydrogen maser) with a time constant of 20 seconds. For this measurement, the CSAC was deliberately mis-tuned in both frequency and phase prior to the measurement, by

$y = 10 \times 10^{-9}$ and $\varphi = 50$ ns

Figure 19 • **CSAC disciplined to a Superior Reference**



In Figure 19, when disciplining was enabled, at T =10 seconds after the event of enabling disciplining, the steering algorithm immediately inserted a frequency offset of -9×10^{-9}, to steer out the 50 ns phase error with 20 second time constant. The steering gradually reduces as the phase approaches zero such that both frequency and phase are corrected to within 1/e of their initial values at one time constant (20 s) and $1/e^2$ within two time constants (40s). After five-six time constants (≈100 s) frequency and phase are corrected to within +/- 5×10^{-13} and +/- 5 ns, respectively.

3.7.2 Heat Sink

The CSAC does not require a heatsink since it consumes low power and therefore produces little heat. Furthermore, the external parts of CSAC are mu-metal (80% Nickel), which is a poor thermal conductor (1/5 that of aluminum). There is no useful thermal path from the inside components to the baseplate or the cover.

3.7.3 Notes on soldering

For initial testing and evaluation, it is recommended that the pins must not be modified or soldered to a PCB. The recommended socket for PCB attachment is Tyco P/N 4-5332070-4.

After evaluation, the pins can be hand soldered to a PCB using 63/37 Tin/Lead solder with a maximum soldering tip temperature of 329°C (625°F).

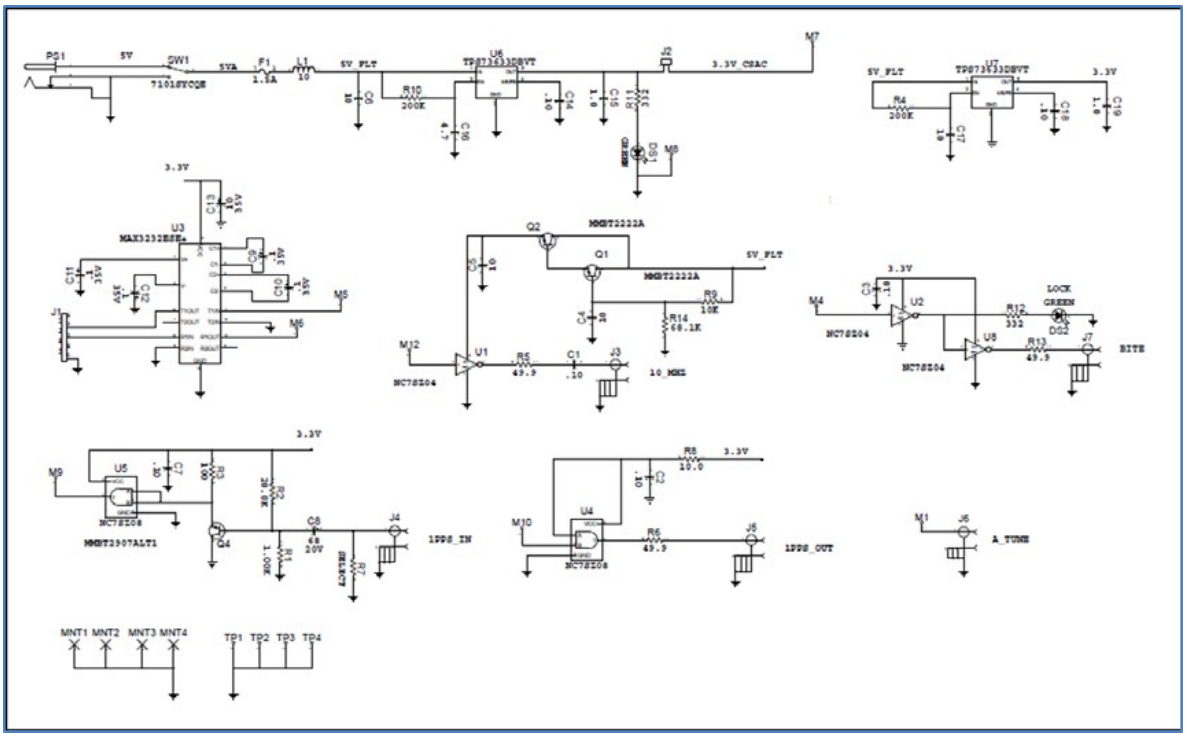
Hand soldering is a necessary requirement for CSAC and solder re-flow is not recommended since the CSAC cannot go above storage temp. It is likely to damage it.

The lead material is 52 Alloy with a plating of 200 µ inches (min.) of tin plate (MIL-T-10727) over 100 µ inches nickel (QQ-N-290).

3.7.4 Notes on the Evaluation Board

Figure 20 shows the reference schematic for the Evaluation Board.

Figure 20 • **Reference Schematic for Evaluation Board**



The 1 PPS input on the evaluation board is capacitively coupled to the CSAC through a Common Collector transistor stage and a UHS inverter. This is to protect the CSAC in the evaluation environment, from 1PPS signals > 5 V.

The 10 MHz output from the CSAC is buffered and cap coupled on the evaluation board. It also offers flexibility to condition the signal as needed by the user

VCC for the UHS inverter is supplied with a resistor divider and Darlington pair to provide a good filter for removing 50 - 60 Hz AC line noise. However, caution must be taken if designed into a circuit elsewhere as the output voltage may vary under higher current loads.

3.7.5 Time Error of a CSAC

Time error of any clock is dependent on its operating conditions (temperature and vibration) and the clocks inherent stability (Aging, ADEV). Time error is given by:

$$E(t) = E_0 + \int_0^t y(t)dt + \varepsilon(t)$$

$$E(t) = E_0 + \left(y_0 t + \frac{1}{2}at^2\right) + \int_0^t y_e(t)dt + \tau\sigma(\tau)$$

where

E(t): Time error accumulation at time t after initial synchronization

E_0: Initial time error at t = 0

y(t): Fractional frequency of the clock at time t, approximated as

$y(t) = y_0 + at + y_e(t)$

y_0: Fractional frequency offset at t = 0

a: Clock aging rate

$y_e(t)$: Fractional frequency offset due to environmental effects (i.e., temperature)

$\varepsilon(t)$: Random fractional frequency fluctuations

$\varepsilon(t) = \tau\sigma(\tau)$

$\sigma(\tau)$: Allan deviation at sampling rate (τ)

A detailed analysis is available in literature [3].

[3] Y. Kim, Holdover Clock Errors In GPS-Disciplined Chip-Scale Atomic Clock, Proc. 2013 Precise Time and Time Interval Systems and Applications Meeting, pp.101-106, 2013

3.7.6 Writes to NVRAM

CSAC has a physical limit to the number of writes to NVRAM < 10,000. To maximize the lifetime of the CSAC, restrict the number of NVRAM writes accordingly.

The following are the scenarios of a write to NVRAM:

- Customer issuing a frequency latch command (format `!FL`) causes an NVRAM write.
- Customer issuing a PPS cable length compensation latch command (format `!DCL`) causes an NVRAM write.
- Customer issuing a PPS disciplining tau set command that changes discipline tau (format `!Dn` where n is a decimal number) causes an NVRAM write.
- Customer issuing a mode command that changes mode register (format `!Mx` where x is an alphabetical character) in list below causes an NVRAM write:
  - RS232 Communications Checksum on/off (`!MC` vs `!Mc`)
  - External oscillator on/off (`!MZ` vs `!Mz`)
  - PPS auto-sync on/off (`!MS` vs `!Ms`)
  - PPS disciplining on/off (`!MD` vs `!Md`)
  - PPS measure on/off (`!MM` vs `!Mm`)
  - Analog tuning on/off (`!MA` vs `!Ma`)
  - ULP on/off (`!MU` vs `!Mu`)
- Customer issuing a ULP configuration command (format `!Un,p` where n and p are decimal numbers) causes an NVRAM write.
- Every ULP cycle, firmware does an automatic NVRAM write.
- Every auto-reset (status 0->8) due to alarm where status reverts from lock state, firmware does an automatic NVRAM write.
- Periodically every 30 days in clock-lock state, firmware does an automatic NVRAM write.
- Customer issuing a PPS pulse width set command that changes pulse width (format `!>N` where N is a decimal number) will cause an NVRAM write. (FW1.08 and later)
- Customer issuing a PPS disciplining status threshold phase command that changes phase threshold (format `!mN` where N is a decimal number) will cause an NVRAM write. (FW1.08 and later)
- Lock set points are saved after each acquisition of a lock state. This write occurs ~102s after Lock is achieved.

4 Technical Support

Microsemi backs its products with various support services including Customer Service, Customer Technical Support Center, a website, electronic mail, and global sales offices. This appendix contains information about contacting Microsemi using these support services. Visit the support webpage for the latest software and documentation: *http://www.microsemi.com/ftdsupport*

To avail the support, login to the Microsemi webpage or create an account if you don't have one already: *http://www.microsemi.com/products/timing-synchronization-systems/support/online-support*

This product contains the software with the latest version at the time of manufacture. Refer to user guides and any system release notices from the website for the latest versions of software and installation procedures: *http://www.microsemi.com/products/timing-synchronization-systems/download-library*

4.1 Customer Service

Contact Microsemi Frequency & Time Division Services and Support at:

4.1.1 Email

Communicate your technical questions to our email address and receive answers back by email:

For USA, Americas, Asia, and Pacific Rim: *ftd.support@microsemi.com*

For Europe, Middle East, and Africa (EMEA) Technical Support: *ftd.emeasupport@microsemi.com*

For EMEA Sales: *ftd.emea_sales@microsemi.com*

4.1.2 Contact

4.1.2.1 USA, Americas, Asia, and Pacific Rim

Microsemi FTD Services and Support

3870 N, First Street

San Jose, CA 95134

Telephone: 408-428-7907

Toll-free in North America: 1-888-367-7966

4.1.2.2 Europe, Middle East, and Africa (EMEA)

Microsemi FTD Services and Support EMEA

Altlaufstrasse 42

Hoehenkirchen-Siegertsbrunn 85635

Germany

Telephone: +49 700 3288 6435

Fax: +49 8102 8961 533