

syn 1588



Single Chip IEEE1588 Clock Synchronization Solution

syn1588[®] VIP Eval Board

Data Sheet

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0 Legals

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1 Overview

The syn1588®VIP enables a cost effective, highly integrated, single chip IEEE1588 based clock synchronization solution. Only a single external Ethernet PHY is required to create a fully functional IEEE1588 node supporting either the default or the telecom profile

The syn1588®VIP is also available as IP core (VHDL source code or technology netlist license) or as an integrated circuit (single chip device) in a BGA256 package.

The entire clock synchronization algorithms are computed in an on-chip 8 bit 8051 microcontroller which runs the complete PTP Stack together with a light weight TCP stack. The syn1588®VIP design offers a standard 10/100/1000 Mbit/s Ethernet network interface with enhancements to provide the system with accurate clock synchronization via Ethernet following the IEEE1588-2008 standard.

The syn1588®VIP delivers a 1PPS output signal as well as a user programmable, synchronized frequency. A NMEA-compatible stream may be generated on the serial interface. An IRIG-B compatible output is optionally available as well.

The operation of the syn1588®VIP evaluation board is controlled remotely via IEEE1588 management messages. Both a command line tool (ptpmmm) as well as a graphical user interface (ptpmmm GUI) is available for managing IEEE1588 nodes remotely.

1.1 Block Diagram

Figure 1 shows the block diagram of the syn1588®VIP evaluation board.

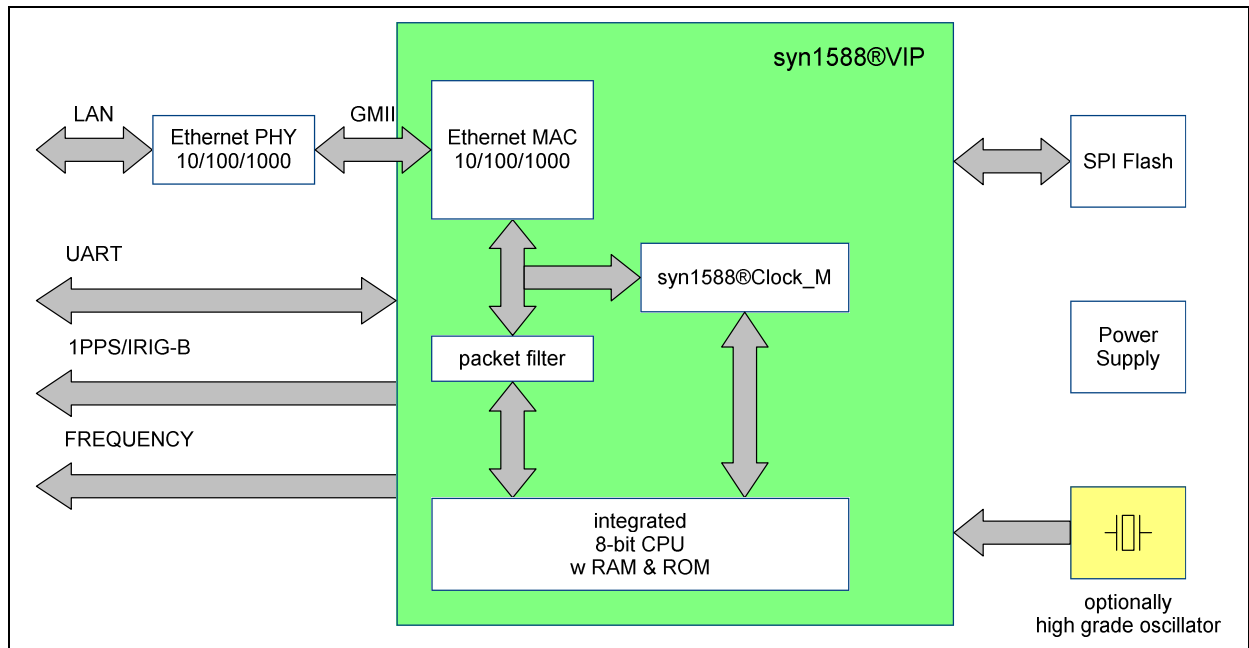


Figure 1 System diagram: syn1588®VIP evaluation board

The syn1588®VIP requires merely an external Ethernet PHY. Optionally a high grade oscillator (TCXO or OCXO) may be mounted onto the syn1588®VIP evaluation board. A SPI flash is used to store the device's configuration as well as the user defined parameters.

1.2 Ordering Information

The syn1588®VIP evaluation board can directly be ordered at Oregano Systems and at our distributors (see our web site <http://oregano.at> for details). There are several options of the syn1588®VIP devices available:

- Standard XO (Ethernet grade 50 ppm) – default option <oscillator type> == ""
- TCXO better than 4 ppm <oscillator type> == "tcxo"
- High accuracy OCXO better than 0,5 ppm <oscillator type> == "ocxo"

1.2.1 Order Code

syn1588vip-evalbrd-<oscillator type>



1.2.2 Example

Ordering the syn1588®VIP evaluation board with a high accuracy OCXO results in an ordering code of “syn1588vip-evalbrd-ocxo”.

2 Features

- Fully IEEE1588-2008 standard compliant network node in a single chip
 - IEEE1588-2008 two-step clock operation
 - Optionally IEEE1588-2008 one-step clock operation
- syn1588[®]PTP stack binary included (running on integrated 8-bit CPU core)
- Single chip solution (except the external Ethernet PHY)
 - No external memory devices required
- Support for both 10/100 Mbit/s (MII mode) or 10/100/1000 Mbit/s operation (GMII mode) following IEEE802.3-2005 standard
- 1PPS output signal (one pulse per second)
 - Optionally IRIG-B data may be transmitted on this signal
- UART outputs time information in GPS compatible NMEA format
 - Suited for GPS replacement via LAN
- 1PPS input received e.g. from a GPS
- Frequency output with a selectable frequency in the range from 1 MHz to 5 MHz
 - Frequency is user selectable
 - Other fixed frequencies (eg. 10 MHz or 25 MHz) can be provided upon request
- Network layer 2 (Ethernet) or network layer 3 (Internet Protocol) operation supported via firmware options
- PTP management interface is supported ([IEEE 1588-2008] Clause 15) allowing remote management
- Configuration of the syn1588[®]VIP node may be stored onto the on-board SPI Flash memory
- Dual boot capability: factory default firmware and user firmware
 - Revert to factory default mechanism available
- Remote update of user firmware
- Clock accuracy better than 50 ns
- Three oscillator options available to allow costs/accuracy trade off
 - Standard XO (50 ppm)
 - TCXO better than 4 ppm
 - High accuracy OCXO better than 0,5 ppm

3 Functional Description

The syn1588®VIP is entirely self contained and does not need any user interaction to operate. There is only one external jumper, which selects the mode of network communication. Via the PTP management interface status information can be gathered in layer 3 mode and clock parameters as well as I/O options can be configured.

Oregano Systems' syn1588®VIP Evaluation Board is a fully functional reference board for the syn1588®VIP IP core or device. Customers may receive all design data of this reference board enabling them to easily adapt this design to their specific needs.

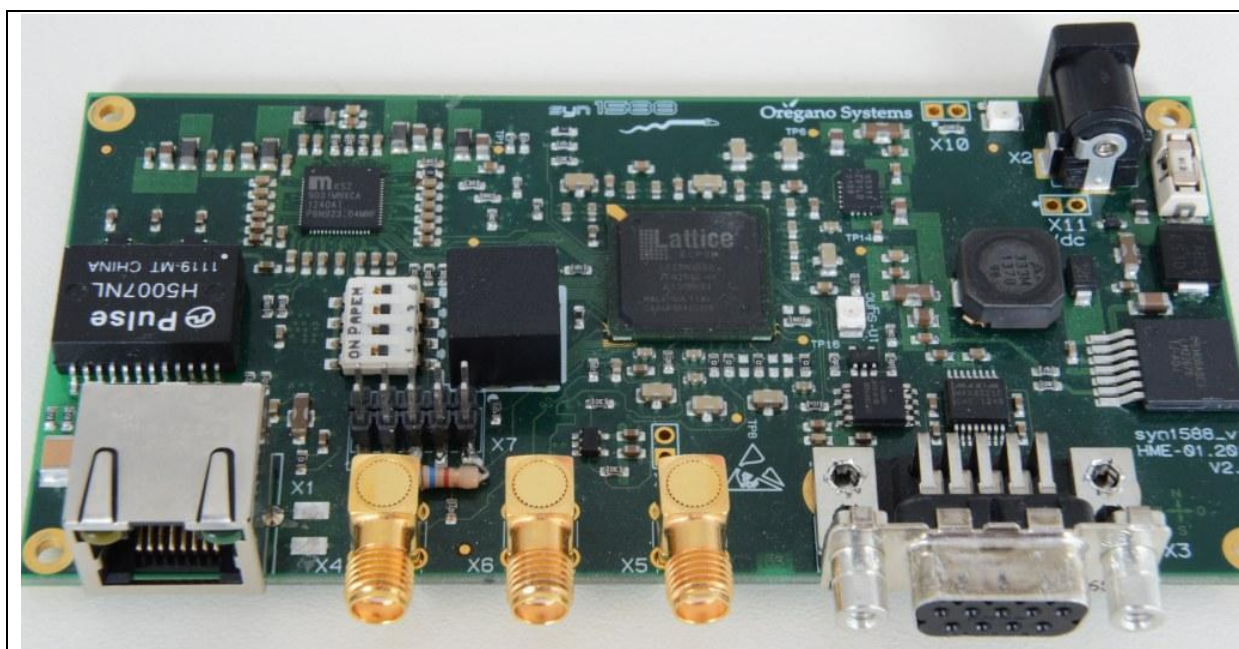


Figure 2 syn1588®VIP Evaluation Board

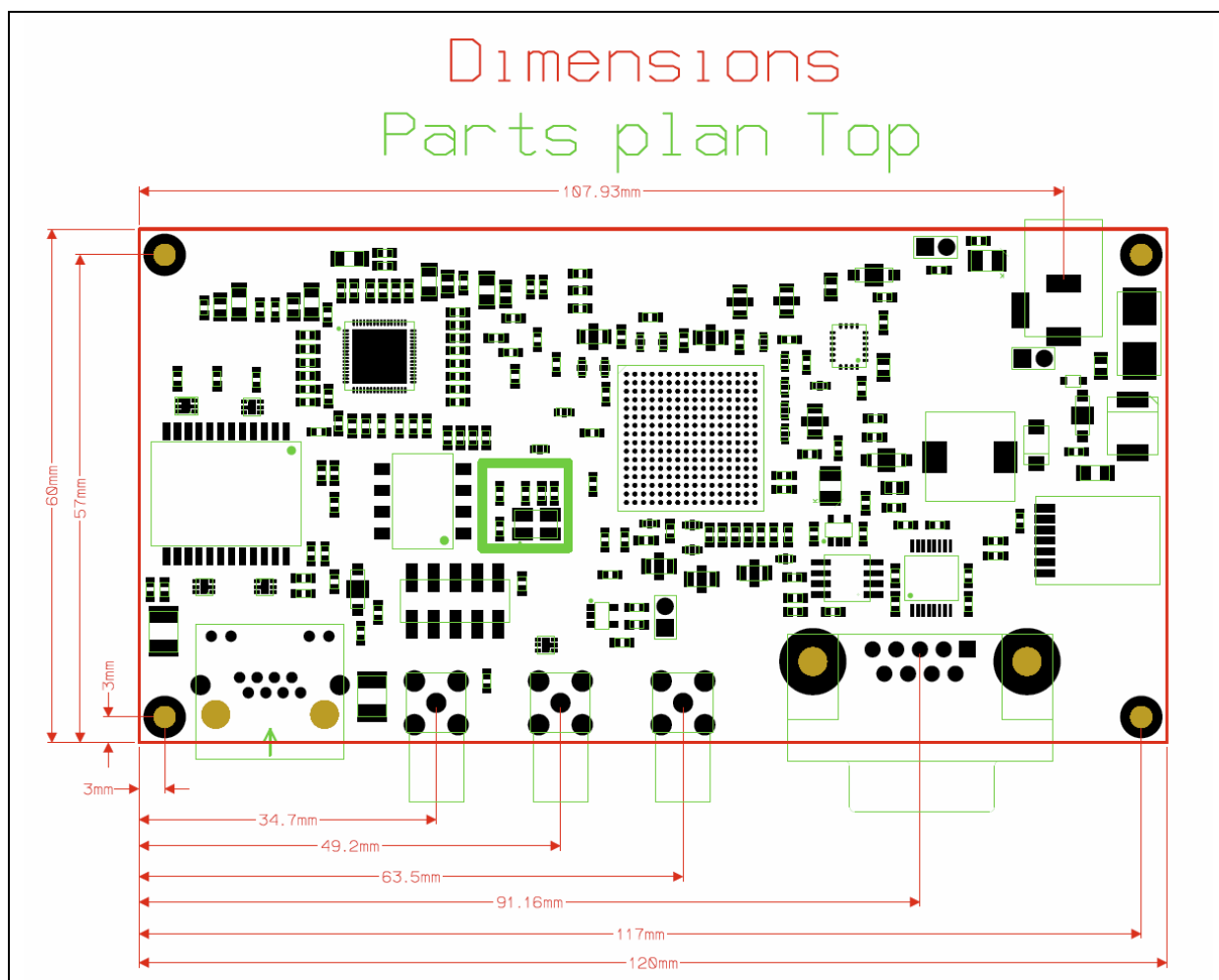


Figure 3 syn1588®VIP Evaluation Board Dimensions

3.1 User I/Os

There are three I/Os - two outputs and one input - for user application purposes.

- 1PPS output
- event input
- frequency output

Note furthermore that all syn1588®VIP evaluation board I/Os are 3V3 tolerant.

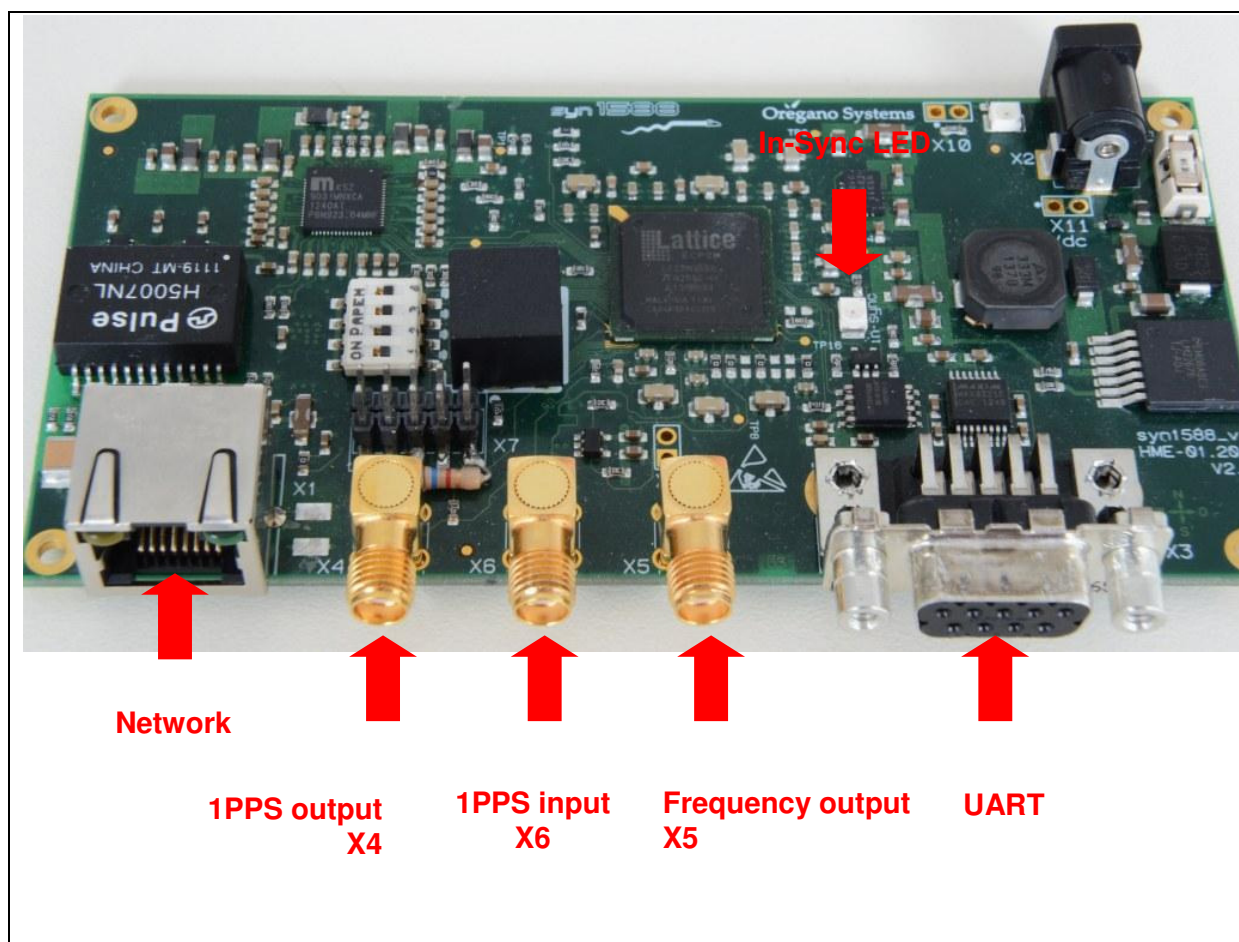


Figure 4 syn1588®VIP Evaluation Board: Connector locations

3.1.1 1PPS Output

The 1PPS signal is available on the IO pin “onepps_o”. A rising edge is output once every second. The pulse width is minimum 1 μ s. The delay of the rising edge with respect to the wrap of the second is three clock periods of the 100 MHz syn1588[®] clock frequency, i.e. 30 ns. Right after initialization the 1PPS output will start to operate.

3.1.2 1PPS Input

The 1PPS input is available at the IO pin “event_i”. A signal transition from low-to-high (rising edge) of an external signal (e.g. a sensor value reaching a threshold) will be sampled with the 100 MHz syn1588[®] clock, a time stamp will be drawn and stored in a local buffer memory. For the correct sampling the minimum pulse width of the external signal has to be three clock periods of the 100 MHz syn1588[®] clock frequency, i.e. 30 ns.

3.1.3 Frequency Output

The frequency output signal is available at the IO pin “frequency_o”. The user may generate an arbitrary frequency derived from and phase locked to the synchronized, high accuracy clock with a resolution of 1 mHz (0.001 Hz) and below. Please keep in mind that frequencies generated by means of the syn1588[®]VIP period output will be phased locked on all nodes within a synchronized IEEE1588 network regardless of the value of the frequency.

The frequency output signal will be instantaneously available if the syn1588[®]VIP operates in master mode. In slave mode the frequency output is available if a master is present in the network and the offset of the node to the master is less than 10 us for the last 16 sync periods.

3.2 In-Sync LED

As soon as the IEEE1588 node is in sync with a master while it operates in slave mode the In-Sync LED is active.

3.3 Accuracy

The overall accuracy within an IEEE1588 network or in other words the maximum deviation between the 1 pps clock signals of any two given nodes is both dependent on several different configuration parameters and on the hardware of the nodes itself.

The latter has two major aspects to consider: On the one side the resolution of the high accuracy IEEE1588 clock located at the network interface defines the resolution of the time stamps gathered while scanning for IEEE1588 timing related packets. Furthermore, the stability of the oscillator driving the high accuracy clock is of equal importance when evaluating accuracy.

With respect to configuration parameters the rate of the sync and, to a certain extent, the rate of the delay request packets have considerable impact on the overall accuracy. For more details please refer to the white paper on highly accurate clock synchronization authored by Oregano Systems.

The local clock of the syn1588[®]VIP offers a resolution of less than 10 ns. If it is equipped with a 50 ppm 25 MHz oscillator accuracy in the range of ± 100 ns can be achieved if the message rate is selected in the range on 1 sec.

If the syn1588[®]VIP is equipped with an OCXO accuracies in the range of ± 10 ns may be achieved. However, it has to be kept in mind that this requires a careful analysis network structure and appropriate selection of all network components.

3.4 Remote Configuration

The syn1588®VIP may be configured using IEEE1588 Management Messages received via the Ethernet interface. Thus the syn1588®VIP unit can be configured remotely. The syn1588®VIP management interface is fully compliant to the IEEE1588 standard. Three vendor specific commands have been implemented to read/write from/to syn1588®VIP units (param, update, clkman).

The Oregano Systems' syn1588® PTP Management Tool (PTPMMM) is the tool of choice for configuring syn1588®VIP nodes. This tool can send IEEE1588 standard management messages as well as the Oregano specific IEEE1588 management messages. Please contact Oregano Systems support to receive a copy of the syn1588® PTP Management Tool free of charge (either via the web site <http://oregano.at> or via email contact@oregano.at).

3.4.1 Example 1: Identifying syn1588®VIP Nodes

The basic usage of the PTPMMM tool in combination with the syn1588®VIP is to read the value of a syn1588®Clock register. This is accomplished in the following way. First invoke the PTPMMM utility:

```
# ./ptpmmm
syn1588(R) PTP Management Tool - V 1.2.83 Rev 475 $ - IEEE1588-2008
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2012
Confidential unpublished data - All rights reserved
>
```

After invocation of PTPMMM you can enter commands that send IEEE1588 management messages to the syn1588®VIP nodes in the network. Note that PTPMMM has no command prompt or the like to facilitate batch operation and automated post processing of output data.

To discover all syn1588®VIP nodes in the network issue the “clock” command. You do this by typing “clock” followed by a carriage return. This should give a similar output like this:

```
# ./ptpmmm
syn1588(R) PTP Management Tool - V 1.2.83 Rev 475 $ - IEEE1588-2008
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2012
Confidential unpublished data - All rights reserved
>clock
0004A3FFFFF32A8B1 1 OC "IEEE 802.3" 0004A332A8B1 IPv4:C0A86776 FFFFFF "Oregano
Systems; syn1588(R) VIP; 00:04:A3:32:A8:B1" "HW build 526; syn1588(R) Clock M
2.1.2; SW 1.2.57" na 001B19000100
```

```
0004A3FFFF32CB96 1 OC "IEEE 802.3" 0004A332CB96 IPv4:C0A867F2 FFFFFFF "Oregano
Systems; syn1588(R) VIP; 00:04:A3:32:CB:96" "HW build 527; syn1588(R) Clock M
2.1.2; SW 1.2.86" na 001B19000100
0004A3FFFF3233BB 1 OC "IEEE 802.3" 0004A33233BB IPv4:C0A867F9 FFFFFFF "Oregano
Systems; syn1588(R) VIP; 00:04:A3:32:33:BB" "HW build 526; syn1588(R) Clock M
2.1.2; SW 1.2.161" "Napatech NTTSE unit" 001B19000100
0050C2FFFE2C2DFAE 1 OC "IEEE 802.3" 0050C2C2DFAE IPv4:C0A86702 000F0C "MBG;;"
";;" ";" 001B19000100
>
```

3.4.2 Example 2: Reading syn1588®VIP Registers

The syn1588®VIP supports a proprietary extension to the PTP management interface. This extension is made up of only one - very powerful – command: “clkman”. It allows to read and write to the hardware registers of the syn1588® VIP.

For example with this command one can read the version of the syn1588®Clock IP core that is embedded in the node. The version of the clock is located in register 0x0. So to get the version of the clock one issues a “clkman” command to read clock register 0x0.

```
# ./ptpmmm
syn1588(R) PTP Management Tool - V 1.2.83 Rev 475 $ - IEEE1588-2008
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2012
Confidential unpublished data - ClockID s reserved
> clock
0004A3FFFF4550CB 1 OC "IEEE 802.3" 0004A34550CB IPv4:C0A867FE FFFFFFF "Oregano
Systems; syn1588(R) VIP; 00:04:A3:45:50:CB" "HW build 527; syn1588(R) Clock M
2.1.2; SW 1.2.54" "Evaluation Version" 001B19000100
>clkman 0004A3FFFF32CB96 1 0 0x0
0004A3FFFF32CB96 1 0x4D323132
>
```

The result of the “clkman” command is always displayed in hexadecimal notation. Since the clock version is encoded as four ASCII characters the result of 0x4d323133 has to be converted in ASCII to get the clock version: 0x4d equals ‘M’, 0x32 equals ‘2’, 0x31 equals ‘1’, and finally 0x32 equals ‘2’. So the clock version is ‘M212’.

3.4.3 Setting and Storing Parameters

Starting with software version 1.2.53 the syn1588®VIP supports managing (read/get and write/set) and non-volatile storage of its parameters. The parameters are stored in the external SPI flash memory by using the management command “save”.

One uses the IEEE1588 management command CLOCK to determine the software revision.

```
clock
0004A3FFFF4550CB 1 OC "IEEE 802.3" 0004A34550CB IPv4:C0A867FE FFFFFFF "Oregano
Systems; syn1588(R) VIP; 00:04:A3:45:50:CB" "HW build 527; syn1588(R) Clock M
2.1.2; SW 1.2.87" "Evaluation Version" 001B19000100
>
```

Software version

Hardware build ID

There are the following group of parameters that may be modified and stored:

- network configuration
- hardware parameters
- syn1588® PTP Stack options
- clock servo parameters

The following sub chapters describe each set of parameters as well as the command used to read (get) and write (set) the parameters.

3.4.3.1 Network Parameters

syn1588®VIP network configuration are read and written using the Oregano Systems' specific IEEE1588 management command "param".

Name	Brief Description	Effective	Default Value
DHCP	Enable/Disable DHCP	Reboot	1
IPADR	Use the following IP if DHCP is disabled	Reboot	0.0.0.0
SubNet	Use this sub net mask if DHCP is disabled	Reboot	0.0.0.0
Gateway	Use this gateway if DHCP is disabled	Reboot	0.0.0.0
nwmode	Specifies if muticast, unicast or both is used M ... multicast U ... unicast B ... both	Reboot	M
nwproto	Selects the network protocol: layer2 ... Using PTP over IEEE802.3 IPv4 ... Using PTP over IPv4/UDP	Reboot	IPv4
dfs	Set the Differentiated Services Field of the IPv4 header (0x0..0xFF)	Reboot	0x0
grantor0	IP address of unicast master 0 (if available)	Reboot	192.168.103.130
grantor1	IP address of unicast master 1 (if available)	Reboot	0.0.0.0

Table 1 List of network parameters

By default, DHCP and multicast mode is enabled. Please make sure that the "save" command has been executed and the device is rebooted (power off/on or "init" management command) after setting a network parameter. If unicast is enabled, the grantor0 and grantor1 parameter offer the possibility to configure two different unicast masters. They are specified by using their IPv4 address. To delete a grantor, the IP address 0.0.0.0 is used. By sending this address, the grantor is deactivated.

Example

First read the IP address and set the IP address to 10.0.0.3 in a second step.

```
param 0004A3FFFF4550CB 1 0 ipadr
0004A3FFFF44FCCA 1 255.255.255.255
> param 0004A3FFFF4550CB 1 0 ipadr 10.0.0.3
0004A3FFFF4550CB 1 DONE
> save 0004A3FFFF4550CB 1 0
0004A3FFFF4550CB 1 DONE
>
```

3.4.3.2 Hardware Parameters

syn1588®VIP hardware parameters are read and written using the Oregano Systems' specific IEEE1588 management command "clkman". See chapter **Fehler! Verweisquelle konnte nicht gefunden werden.** for a detailed description of this command.

Example

Read the OSZPWM_CTR register; write the same register with the value 0xA6.

```
clkman 0004A3FFFF4550CB 1 0 0x1e0
0004A3FFFF44FCCA 1 0x0000007F
> clkman 0004A3FFFF4550CB 1 0 0x1e0 0xA6
0004A3FFFF44FCCA 1 DONE
>
```

Name	Brief Description	Effective	Default Value
OSCPWM_CTR	PWM Control register	instantly	0x00002E8B
SHDWSTEP_L	Step size lower 32 bit	instantly	0x015CED66
SHDWSTEP_H	Step size higher 32 bit (lower 16 bit used)	instantly	0x00000000
PERIODTIME0_L	Period of timer 0, lower 32 bit	instantly	0x00000000
PERIODTIME0_H	Period of timer 0, upper 32 bit	instantly	0x00000000
TRIGTIME1_L	Time to trigger event 1, lower 32 bit	instantly	0x00000000
TRIGTIME1_H	Time to trigger event 1, upper 32 bit	instantly	0x00000000

Table 2 List of hardware parameters

3.4.3.3 syn1588® PTP Stack Parameters

The following parameters are standard IEEE1588 parameters where dedicated IEEE1588 management messages are available. Therefore, they are not configured with the “param” command. The fourth column “Command” in Table 3 shows the respective management message and thus ptpmmm command required for set/get this parameter.

Name	Brief Description	Effective	Command	Default Value
Accuracy	set clock accuracy (range 0..255)	instantly	accuracy	39
Announce Interval	set announce interval (log2 range -4..4)	instantly	aival	1
Delay Mechanism	delay mechanism used: E .. end-to-end (0x01) P .. peer-to-peer (0x02) 0 .. no delay mechanism at all (0xFE)	instantly	dlymech	0x01
Domain	set Domain (range 0..255)	instantly	domain	0
pDelay Request Interval	set minimum path delay request interval (log2 range 0..5)	instantly	pival	0
Priority 1	sets Priority1 (range 0..255)	instantly	prio1	128
Sync Interval	set synchronization interval (log2 range -8..+8)	instantly	sival	0
User	Assigns a user description to the clock	instantly	user	syn1588_VIP

Table 3 List of IEEE1588 standard parameters

Example

Read the delay mechanism used; set the delay mechanism to peer-to-peer (0x2).

```
dlymech 0004A3FFFF4550CB 1 0
0004A3FFFF4550CB 1 E
> dlymech 0004A3FFFF4550CB 1 0 0x2
0004A3FFFF4550CB 1 DONE
>
```

3.4.3.4 Extended syn1588® PTP Stack Parameters

The extended parameters of the syn1588® PTP stack are read and written using the Oregano Systems' specific IEEE1588 management command "param". Table 16 shows all available parameters.

Example

Read the current log level of the selected clock; set the log level to verbose mode (0x2).

```
param 0004A3FFFF4550CB 1 0 loglevel
0004A3FFFF4550CB 1 0x1
>param 0004A3FFFF4550CB 1 0 loglevel 0x2
0004A3FFFF4550CB 1 DONE
>
```

Name	Brief Description	Effective	Default Value
adjval	Sets the clock adjust interval (log2 range 0..8)	instantly	0
twoStep	Use 2-step (1) or 1-step (0) mechanism	instantly	1
dlyReqIval	Sets the minimum delay request interval offset added to syncInt (log2 range 0..8)	instantly	4
Variance	set clock variance (range 0..0xFFFF)	instantly	0xFFFF
class	set clock class [248] M_EXT....Master on External Reference (6) M_HOLD...Master on External Reference (in Holdover) (7) M_NSUNC..Master on External Reference (not synchronized) (52) M_SLAVE..Master on External Reference (may be Slave) (187) S...Slave Only (default 255)	instantly	255
dlyAsym	delay asymmetry correction in scaled nanoseconds	instantly	0
boundary	Sets a boundary for offset to master in scaled nanoseconds	instantly	0
logLevel	change verbosity level (range 0..4) [default 0] (if available)	instantly	2
syncOut	Enable/Disable GPS-formatted output (NMEA) (if available)	instantly	true
syncIn	Enable/Disable external sync input (1PPS Event) (if available)	instantly	true

Table 4 List of syn1588® PTP Stack parameters

3.4.3.5 Clock Servo Parameters

The syn1588® clock servo parameters are read and written using the Oregano Systems' specific IEEE1588 management command "param".

Name	Brief Description	Effective	Default Value
PIK	PI Controller K (rel. to 65535) (range 0..0xFFFF)	instantly	16384
PIT	PI Controller T (rel. to 65535) (range 0..0xFFFF)	instantly	2048
IIRSMS	IIR Filter Stiffness M2S (rel. to 65536) (range 0..0xFFFF)	instantly	32768
IIRSPath	IIR Filter Stiffness Path (rel. to 65536) (range 0..0xFFFF)	instantly	32768
IIRAP	IIR Filter Adjustment Period (range 0..16)	instantly	4
IIRAG	IIR Filter Adjustment Gain (range 0..24)	instantly	16
TSplaus	change size of timestamp plausibility interval (range 0..31)	instantly	2

Table 5 List of Clock Servo parameters

3.5 Remote Firmware Update

Starting with software revision 366 (software version 1.2.0) and hardware build 522 the syn1588®VIP supports remote update of its firmware (i.e. FPGA bitstream and software). One can use the IEEE1588 management command “clock” to determine the hardware build revision.

```
clock
0004A3FFFF4550CB 1 OC "IEEE 802.3" 0004A34550CB IPv4:C0A867FE FFFFFFF "Oregano
Systems; syn1588(R) VIP; 00:04:A3:45:50:CB" "HW build 527; syn1588(R) Clock M
2.1.2; SW 1.2.54" "Evaluation Version" 001B19000100
>
```

Software version

Hardware build ID

The syn1588®VIP evaluation board supports dual-boot configurations as well as the remote update function. The “dual-boot” function allows the local storage of two independent FPGA bitstreams (including the required software) that are selected automatically during system power-up.

There is the “user configuration” and the “factory configuration”, latter one also referred to as the “golden configuration”. The syn1588®VIP will always try to boot the “user configuration”. If there is an error detected while loading the “user configuration” the “factory default configuration” will be loaded. Thus the “factory default configuration” acts as the known good configuration and ensures the proper operation of the syn1588®VIP under faulty conditions.

The remote update feature of the syn1588®VIP allows the user to update the “user configuration” remotely via the network. The “factory default configuration” cannot be altered remotely.

Caution!

If the remote update of a syn1588®VIP unit fails e.g. due to high network load immediately re-try the remote update procedure until it completes successfully. Never power down or reboot the unit in this state! This may invalidate the non-volatile memory and disable to operation of the unit!

3.5.1 Pre-Requisites

The following items are required for a successful remote firmware update of a syn1588®VIP.

- Oregano Systems’ ptpmmm software version 1.2.0 Rev 366 or later
- Optional Oregano Systems’ ptpmmm GUI software version 1.1 Build 482 or later

- New bitstream (the bit-file) for syn1588®VIP supplied by Oregano Systems' support
- The syn1588®VIP to be updated of course. Check that the syn1588®VIP is suited for remote update. Version has to be 510 or later. One can read the version of the syn1588®VIP using the ptpmmm software remotely.
- A computer running the ptpmmm software (Windows or Linux)

The syn1588®VIP may be connected point-to-point to the remote update computer or via a switched network.

3.5.2 Remote Firmware Update Procedure

The remote update is performed using the ptpmmm management software. The remote update may be performed either by running the ptpmmm on the command line or via the ptpmmm GUI. In the following we will describe in detail the command line flow since the GUI flow is self-explanatory.

- Invoke ptpmmm GUI
- Select the clock to be updated
- Open the syn1588 firmware update dialog (right click on clock)
- One is asked to select the bit file in the file system (file dialog box)
- One is asked for confirmation for start of the remote update
- A result window is displayed

Start the ptpmmm software from the command line as shown in the following example.

```
./ptpmmm
```

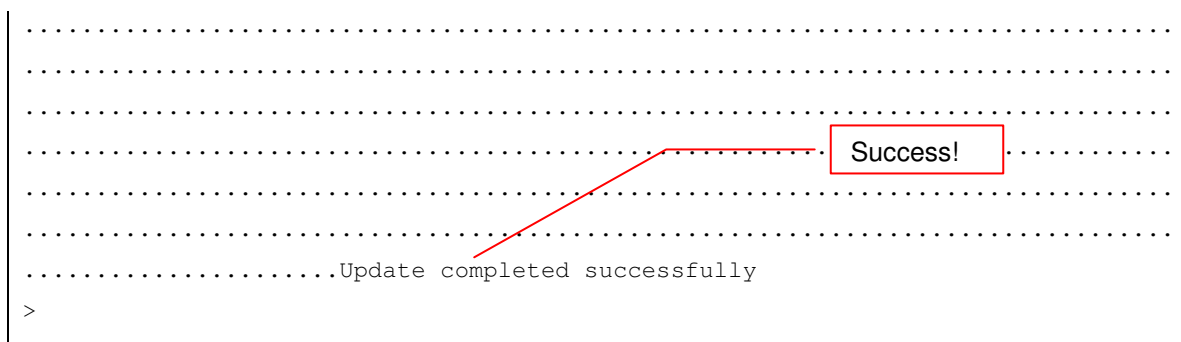
First identify the syn1588®VIP, which should be updated (e.g using the “clock” command). Determine the clock identifier, the port number and domain of the unit to be updated. See the following example for more details.

OC .. ordinary clock

```
update    <ClockId> <PortNumber> <Domain> <raw-bit-filename> <Startaddr(23:0)>
```

Programming

This image shows a full page of primary-ruled paper. It features a vertical margin line on the left side, creating a narrow left margin. The rest of the page is filled with horizontal dotted lines, which are evenly spaced and extend from the margin line to the right edge. There are no other markings, text, or illustrations on the page.



The start address has to be always 0x10000. The FPGA bit file can be addressed by absolute path or by relative path (recommended) to the location, where PTPMMM has been invoked. The “update” command will require approximately one minute for completion.

After performing the remote update, a power cycle is required to load the new configuration data from flash memory into the FPGA. After power-on the syn1588®VIP loads the user configuration (updated previously) from address 0x10000. If this process fails due to any reason, the syn1588®VIP loads the factory default configuration from address 0x0.

3.6 Revert to Factory Default

Starting with hardware build 531, the syn1588®VIP supports “Revert to Factory Default” of its firmware (i.e. FPGA bitstream and software) and of the user defined configuration parameters. One can use the IEEE1588 management command “clock” to determine the hardware build revision.

This can be achieved by connecting the SMA connectors of 1PPS input (X4) and 1PPS output (X6) with a SMA coax cable during power-on. The length of this SMA cable should be max. 1 m. Afterwards the SMA cable has to be removed again, and a second power cycle is necessary. The syn1588®VIP will then boot from the “Golden Image”.

Reverting to factory default is necessary, if the user defined configuration parameters have been altered in such a way, that the syn1588®VIP is not responding any more to the Ethernet or IP network (e.g. invalid fixed IP-address), or may be necessary before performing a major remote firmware update.

4 Electrical Characteristics

4.1 Supply Voltage Characteristics

The syn1588®VIP board's input supply ranges from 5 V to 12 V DC. The board has an option for a stable OCXO device.

DC Characteristics	
Minimum DC input voltage	5 V
Maximum DC input voltage	12 V
Maximum DC supply current @5 V	180 mA
Maximum DC supply current @12 V	400 mA

Table 6 Power supply DC characteristics (without OCXO)

The power jack is implemented as a standard coaxial power connector. It is 5.5 mm in outside diameter and 2.1 mm in inside diameter.

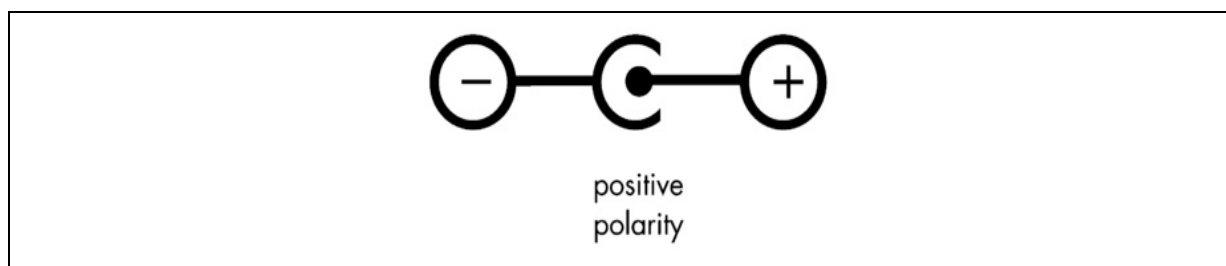


Figure 5 Power supply polarity of power jack

4.2 SMA Output Characteristics

Output coupling	DC
Output threshold: high	2.9 V min
Output threshold: low	0.4 V max
Absolute maximum applied voltage	-0 V to 3.465 V
Output to output skew, synchronous	< 1 ns, typical
Output current	±20 mA, max

Table 7 SMA output characteristics

All IO's are ESD protected according to the following standards

- IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)

4.3 SMA Input Characteristics

Input coupling	DC
Input threshold: high	2.0 V min
Input threshold: low	0.8 V max
Absolute maximum applied voltage	-0 V to 3.465 V

Table 8 SMA input characteristics

All IO's are ESD protected according to the following standards

- IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)

4.4 Serial Interface Configuration

Baudrate	115200
Databits	8
Parity	None
Stopbits	1
Hardware Flow Control	None

Table 9 UART configuration

5 Environmental

5.1 Temperature

Operating temperature range 0 – 50 °C

Storage temperature range -40 - +85 °C

5.2 Humidity

Operating humidity 5% to 80% RH, non-condensing

6 syn1588®VIP Handling Instructions

Caution

The syn1588® VIP is sensitive the electrostatic discharge that may damage the unit. Please observe the proper ESD protection rules. Do not directly touch the unmounted syn1588® VIP while not being properly grounded. Use the ESD bags provided by Oregano Systems for shipping and storage.

