R&D Gh

MVC-LVPS
Telemetry Specification
29D-DE00-801-ABC

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1 SCOPE

This specification defines the requirements for a telemetry interface between the Medium Voltage Converter (MVC), and Low Voltage – Communications module (LV).

2 REFERENCED DOCUMENTS

[1] Texas Instruments TLC2543-Q112 Bit A-D Converter with Serial Control Data Sheet

3 ABBREVIATIONS

MVC: **M**edium **V**oltage **C**onverter
LVPS: **L**ow **V**oltage **P**ower **S**ystem
LV: **L**ow **V**oltage communications module
SPI: **S**erial **P**eripheral **I**nterface
A-D: **A**nalogue to **D**igital **C**onverter

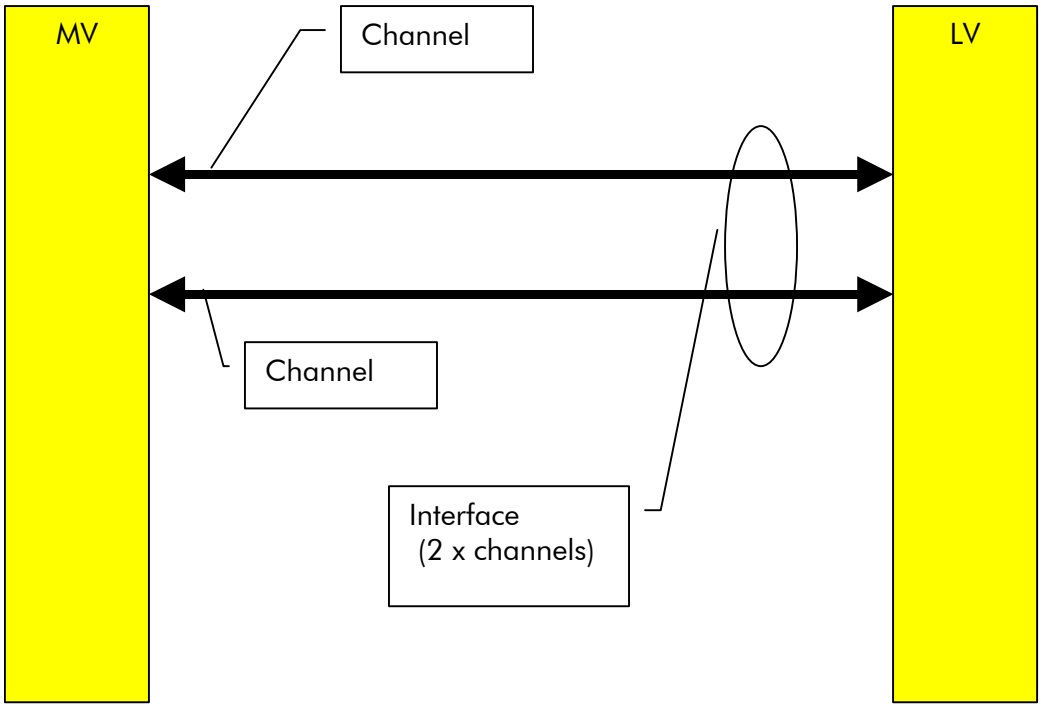
4 INTRODUCTION

This specification defines the requirements for a telemetry interface between the Medium Voltage Converter (MVC), and Low Voltage – Communications module (LV).
The interface permits 8 measurements taken at points within the MVC to be passed to the LV for further forwarding to the shore based monitoring equipment. The parameters to be monitored are recorded below:

- MV Converter Input Voltage
- MV Converter Input Current
- MV Converter Output Voltage
- MV Converter Output Current
- MV Converter Temp1 & 2
- MV Converter Pressure
- MV spare1

5 FUNCTIONAL REQUIREMENTS

The interface shall be fully redundant, providing two independent channels for enhanced reliability.



5.1 Data Transfer Protocol

The interface shall be based on the SPI protocol, each channel comprising 4 signals as shown below. The SPI protocol requires one end of the link to be the 'master' with the other end being the 'slave'. The master initiates all data transfers, and originates three signals. The 'slave' responds to the 'master', and originates 1 signal. The LV shall be the SPI 'master'.

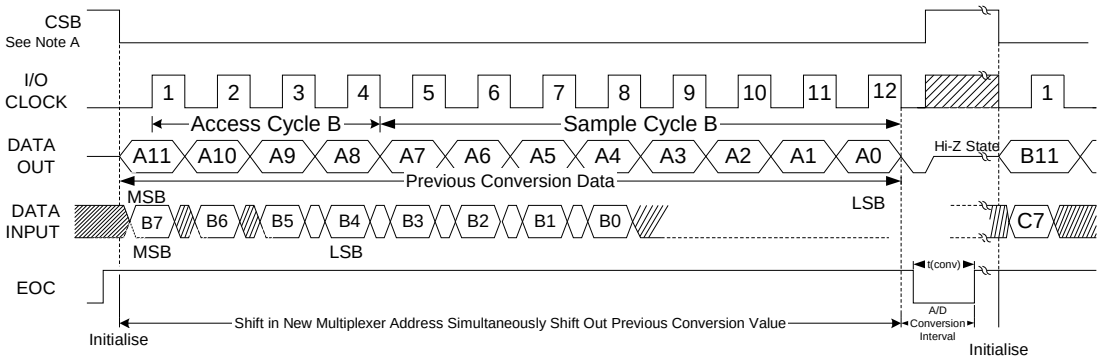
Table 1 SPI Signal Definitions

Signal name	Source	Destination	Brief description
Clip Select (CS)	Master (LV)	Slave (MV)	Asserted whilst a data transfer session is in progress.
Clock (CK)	Master (LV)	Slave (MV)	Timing reference for all data transfers.
Master Out Slave In (MOSI) DATA O/P	Master (LV)	Slave (MV)	Data from the 'master' (LV) to the 'slave' (MV).
Master In Slave Out (MISO) DATA I/P	Slave (MV)	Master (LV)	Data from the 'slave' (MV) to the 'master' (LV).

5.2 General definition of Signals and timing requirements

The general form of data to be presented at the A-D chip with SPI protocol is described below. The MV uses the Texas Instruments TLC2543-Q1 12 Bit A-D Converter with Serial Control. This section defines the behaviour at the A-D chip. Incoming and Outgoing signals from the MV may be subject to inversions passing through the opto-couplers. Where this occurs this shall be corrected for before connecting to the A-D IC.

Logic 1: 5 V max, Logic 0 : 0 V



NOTE A: To minimise errors caused by noise at CSB, the internal circuitry waits for a setup time after CSB going low before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum CSB setup time has elapsed.

Figure 1: Timing for 12-Clock Transfer Using CSB with MSB First

The I/O cycle shown in Figure 1 shall be implemented on the MVC Measurement Card. The selected mode of operation shall be the 12-bit resolution mode.
Initially, with CHIP SELECT at logic high, the I/O CLOCK and DATA INPUT shall be disabled and the DATA OUT shall be in the high-impedance state. CHIP SELECT going low shall begin the conversion sequence by enabling I/O CLOCK and DATA INPUT and removes DATA OUT from the high-impedance state.

An 8-bit data stream (DATA INPUT) initiates each measurement interrogation, consisting of a 4-bit analogue channel address (D7-D4), a 2-bit data length select (D3-D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0). The DATA OUT stream for a given interrogation is returned in the subsequent 12-bit message frame i.e. in Figure 1 above the data requested by message DATA INPUT B7-B0 appears in DATA OUT B11-B0 etc. Outgoing DATA from the device is clocked out on the falling edge of the I/O Clock, whereas Incoming DATA is sampled on the rising edge of the I/O Clock.

In order to achieve successful transmission the following timings need to be allowed for in a measurement cycle:
Setup time, CSB low before first clocking in first address bit, $\mathbf{tsu_{(CSB)} = 1.425\ \mu s}$
Delay time, last I/O Clock to EOC $\mathbf{td_{(I/O\text{-}EOC)} = 2.2\ \mu s}$

The transition time for I/O Clock (High-Low or Low-High) shall be better than 1µs

The transition time for DATA INPUT and CSB (High-Low or Low-High) shall be better than 10µs

The 8-bit data stream (DATA INPUT) for the MVC Measurement Card is defined in Table 2

N.B. The Manufacturers recommends that signaling to this device in the mode described above should be in continuous 12 clock cycles. If it is necessary to insert a gap in the measurement cycle, the preferred position would be between the 4th and 5th clock cycles for optimum measurement accuracy.

The DATA OUT 12-bit data, for each channel is decoded in the LVPS into a voltage between 0-5 Volts. These decoded values are subsequently referred to as AIN0, AIN1 etc. These are in turn translated into the Measurement Parameters required by the algorithms given in Paragraph 5.3.1

Table 2 Input Registers for the MVC A-D Converter

FUNCTION SELECT	DATA INPUT BYTE							
	ADDRESS BITS				L1	L0	LSBF	BIP
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
Select Input Channel AIN0	0	0	0	0	x	0	0	0
Select Input Channel AIN1	0	0	0	1	x	0	0	0
Select Input Channel AIN2	0	0	1	0	x	0	0	0
Select Input Channel AIN3	0	0	1	1	x	0	0	0
Select Input Channel AIN4	0	1	0	0	x	0	0	0
Select Input Channel AIN5	0	1	0	1	x	0	0	0
Select Input Channel AIN6	0	1	1	0	x	0	0	0
Select Input Channel AIN7	0	1	1	1	x	0	0	0
Select Input Channel AIN8	1	0	0	0	x	0	0	0
Select Input Channel AIN9	1	0	0	1	x	0	0	0
Select Input Channel AIN10	1	0	1	0	x	0	0	0
Select Test Voltage $(V_{ref+}-V_{ref-})/2$	1	0	1	1	x	0	0	0
Select Test Voltage $V_{ref\ -}$	1	1	0	0	x	0	0	0
Select Test Voltage $V_{ref\ +}$	1	1	0	1	x	0	0	0
Select Software Power Down	1	1	1	0	x	0	0	0

The particular Interface timing requirements are discussed in Para 6.2

Note the A-D IC provides 3 inbuilt test voltage inputs that are derived from the MVC supply rails. $Vref_+$ is connected to +5 V, $Vref_-$ is connected to 0 V, resulting in $(Vref_+ - Vref_-)/2 = +2.5$ Volts. Any of these 3 Test voltage selections can be used to validate the SPI data link between the MVC and LV Comms. Unit.

5.3 MVC Data Measurement for passing to LVPS

Table 3 below shows the required measurements for passing to the LV Comms. unit, with their associated ranges and measurement accuracies. The results are used to construct the 12 bit-serial data stream used for the DATA OUT signals as described in Paragraph 5.2

Table 3 MVC Monitoring Data

Analogue Measurement	Input Channel	Resolution	Accuracy	Min	Max
MV Converter Input Voltage	AIN0	10V	+/-1%	5000V	12000V
MV Converter Input Current	AIN1	10mA	+/-1%	10mA	3A
MV Converter Output Voltage	AIN2	1V	+/-1%	1V	500V
MV Converter Output Current	AIN3	100mA	+/-1%	100mA	35A
MV Converter Temp1	AIN4	1°C	+/-1%	0°C	100°C
MV Converter Pressure	AIN5	0.1 Bar	+/-1%	0 Bar	5 Bar
MV Converter Temp2	AIN6	1°C	+/-1%	0°C	100°C
MV spare1	AIN7				

5.3.1 MVC Transfer Coefficients

The transfer equations to be used by LV/ Data collecting Terminal for the returned counts from the MV are as follows:

MV Converter Input Voltage = -4000 x AIN0
MV Converter Input Current = 0.6 x AIN1
MV Converter Output Voltage = 160 x AIN2
MV Converter Output Current = 10 x AIN3
MV Converter Temp1= ((AIN4 – 1.375) /22.5 X 10E-3)
MV Converter Pressure = 1 x AIN5
MV Converter Temp1= ((AIN6 – 1.375) /22.5 X 10E-3)

6 PHYSICAL INTERFACE REQUIREMENTS

In order to minimize the transfer of noise from the MV to the LV, all of the signals shall be opto-isolated at each end. Each signal comprises 2 wires, the '+' terminal is a current limited voltage source, the '-' terminal is the switching terminal able to sink current from the source.

For all signals at the interface, logic 1 level corresponds to the low current condition, and logic 0 level corresponds to the high current state.

The LVPS interface shall provide three output switches for the CSB, I/O Clock and DATA I/P functions, one input sensor and the voltage source for all the opto-isolator diodes as shown in Figure 6. The LVPS positive supply connections (+) for CSB, I/O Clock and DATA I/P will be used to provide DC bias to the integral PIN diode of the MV opto coupler associated with the DATA O/P (MISO). The current drain expected as a result will be of the order of 60 μA. The MV must supply filtering required. No impairment of the LV signals shall occur as a result of this.

The MV provides three input sensors, and one output switch as shown in Figure 6.

6.1 Signal levels

6.1.1 LVPS to MVC interface (CSB select, I/O clock, DATA IN)

Logic 1: < 10μA , Vmax = 12 +/-0.5 Volts

Logic 0: 2mA < Io < 20mA with up to maximum load of 2.4 kΩ distributed between MVC/LVPS. The total impedance across the shared electrical path must be adjustable to achieve the optimal current drive conditions for the opto-coupler components. In order to achieve this part of the load must be supplied by each unit.

6.1.2 MVC to LVPS interface (DATA O/P)

Logic 1: < 10μA, Vmax = 12V +/-0.5 Volts

Logic 0: 5 mA < Io < 20mA with up to maximum load of 2.4 kΩ distributed across MVC/LVPS. The total impedance across the shared electrical path must be adjustable to achieve the optimal current drive conditions for the opto-coupler components. In order to achieve this part of the load must be supplied by each unit.

6.2 Timing Requirements

6.2.1 Frequency Range

The Maximum Operating Frequency of the Interface shall be 2 kHz

6.2.2 Rise and Fall Times

The rise time shall be better than 90µs (10% to 90%)

The fall time shall be better than 90µs (90% to 10%)

6.2.3 Interface Waveforms

The following defines the signals at the interface point between the LVPS and MV. Refer to Figure 6. The test frequency to be used is 2 kHz, with a bus length of 5m between the units. For the purposes of the following limits the average worst-case delay through the MV and LV interface opto-couplers is assumed to be 60µs

For the purposes of this definition, the signals should be measured with the receiver diode replaced by the diode network shown in the inset diagram in Figure 7 and measured across the 2kΩ load resistor

6.2.3.1 Data O/P From LVPS

See Figure 2 below. For the purposes of testing the LVPS waveforms an arrangement similar to Figure 7 should be used. At the LVPS output the MOSI data (DATA INPUT) shall change on the falling clock edge. The waveforms for CSB, I/O Clock, and MOSI data should be compared for relative timing differences. The delay between the falling edge of the Clock (Tc) and the MOSI data (Tmo) shall be: - -60µs < Tc-Tmo< 60µs. The delay between the falling edge of CSB and the rising edge of I/O Clock shall be $\mathbf{tsu_{(CSB)}}$ **+Ttol , where** $\mathbf{tsu_{(CSB)}}$ **=** 1.425 μs and **Ttol=** 60µs, being the total worst case differential delay between the CSB and I/O CLOCK signals through the MV opto-couplers

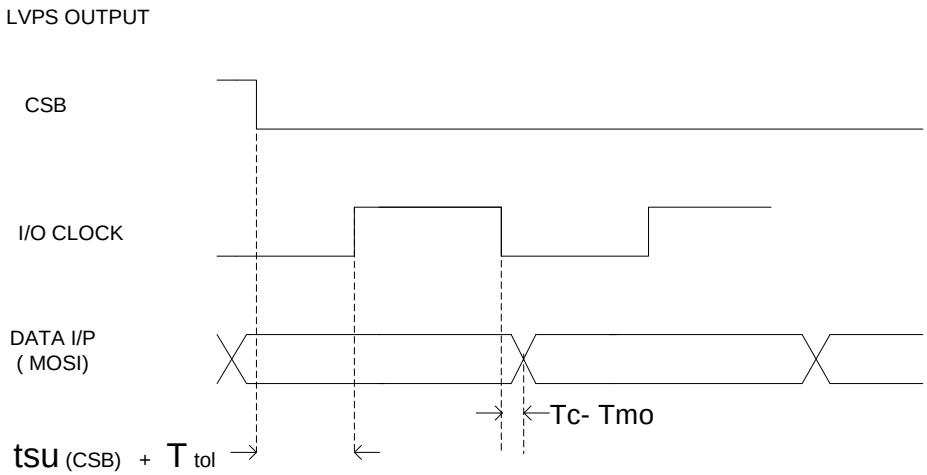


Figure 2 LVPS Output DATA I/P to I/O Clock phasing at Interface

6.2.3.2 Data I/P To MV

See Figure 3 below.

At the MV input, MOSI shall be sampled on the rising clock edge. The MOSI data shall be set Ts-Tmo before the clock rising edge, and remain valid until Th-Tmo after the clock edge. Data that meets this constraint shall be correctly accepted by the MV. The limits should be determined by adjusting the DATA I/P or I/O CLOCK phase by introducing suitable delays in either path. Alternatively, the minimum of the two timings can be found by increasing the clock frequency until the onset of decoding errors.

Ts-Tmo = 110µs.
Th-Tmo = 110µs.

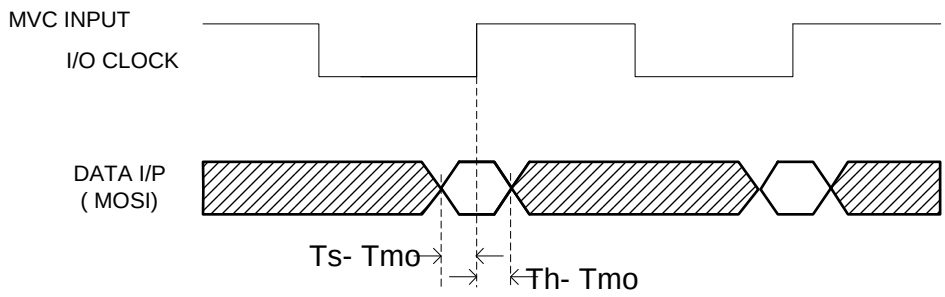


Figure 3 MVC DATA I/P to I/O Clock phasing at Interface

6.2.3.3 Data O/P From MV

See Figure 4 below.

For the purposes of testing the MV waveforms an arrangement similar to Figure 8 should be used. At the MV output the MISO data shall change on the falling clock edge. At the MV, the delay between the falling edge of the clock input and the MISO data shall be:-
0µs < Tc-Tmi < 120µs

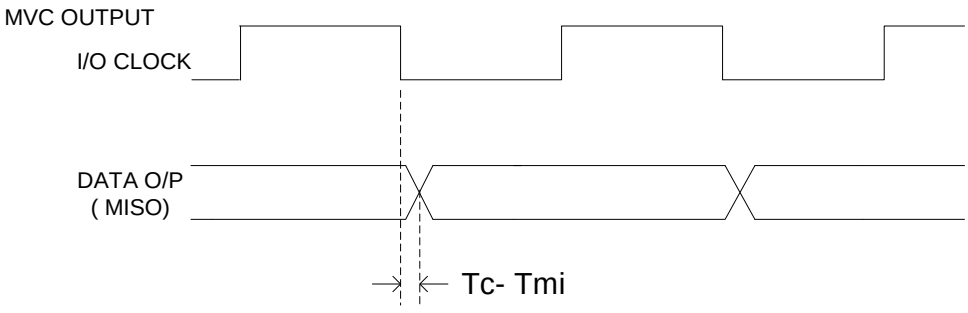


Figure 4 MVC DATA O/P to I/O Clock phasing at Interface

6.2.3.4 Data O/P to LVPS

See Figure 5 below.

At the LVPS input, MISO shall be sampled on the rising clock edge. The MISO data shall be set Ts-Tmi before the clock rising edge, and remain valid until Th-Tmi after the clock edge. Data that meets this constraint shall be correctly accepted by the LVPS. The limits should be determined by adjusting the DATA O/P or I/O CLOCK phase by introducing suitable delays in either path. Alternatively, the minimum of the two timings can be found by increasing the clock frequency until the onset of decoding errors.

Ts-Tmi = 70µs
Th-Tmi = 1µs

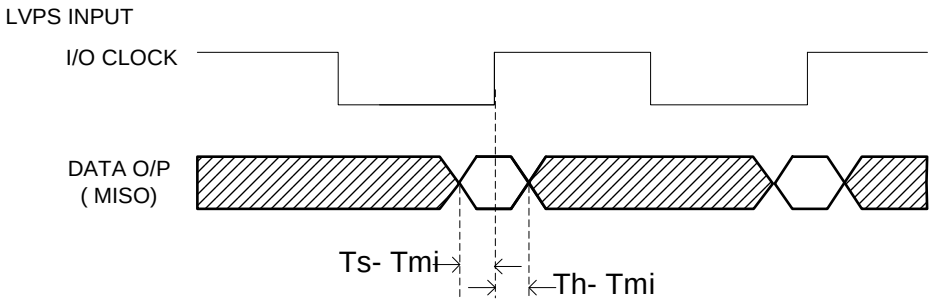


Figure 5 LVPS INPUT DATA O/P to I/O Clock phasing at Interface

APPENDIX A MV & LVPS Circuit Diagrams

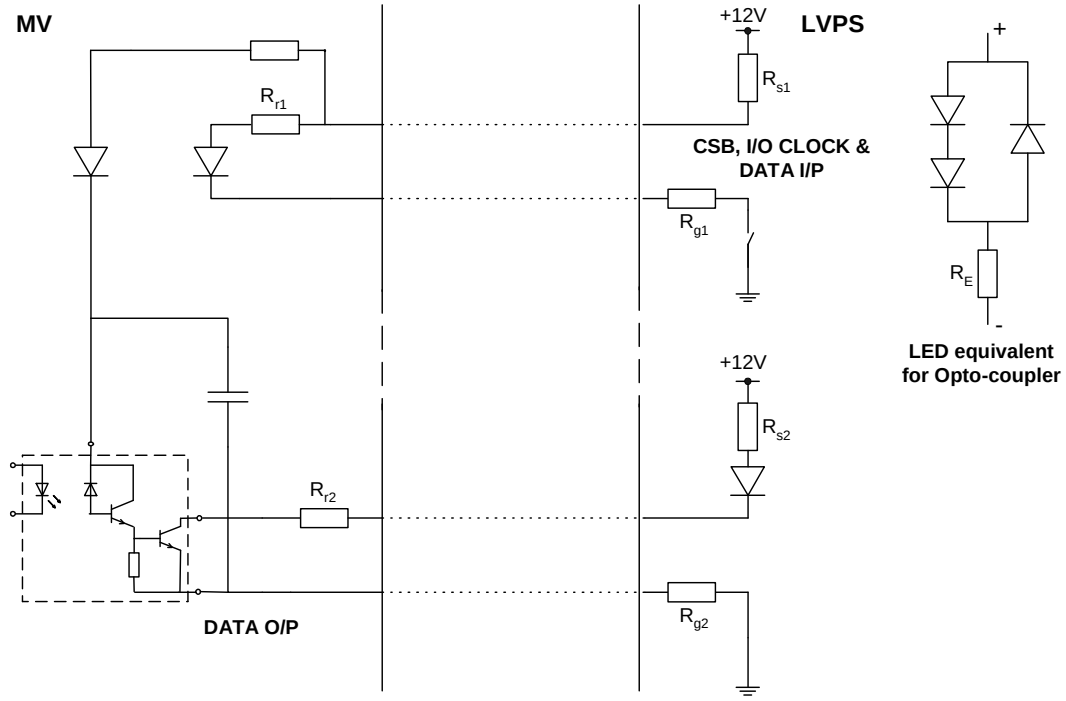


Figure 6 Equivalent circuits for Interface circuitry

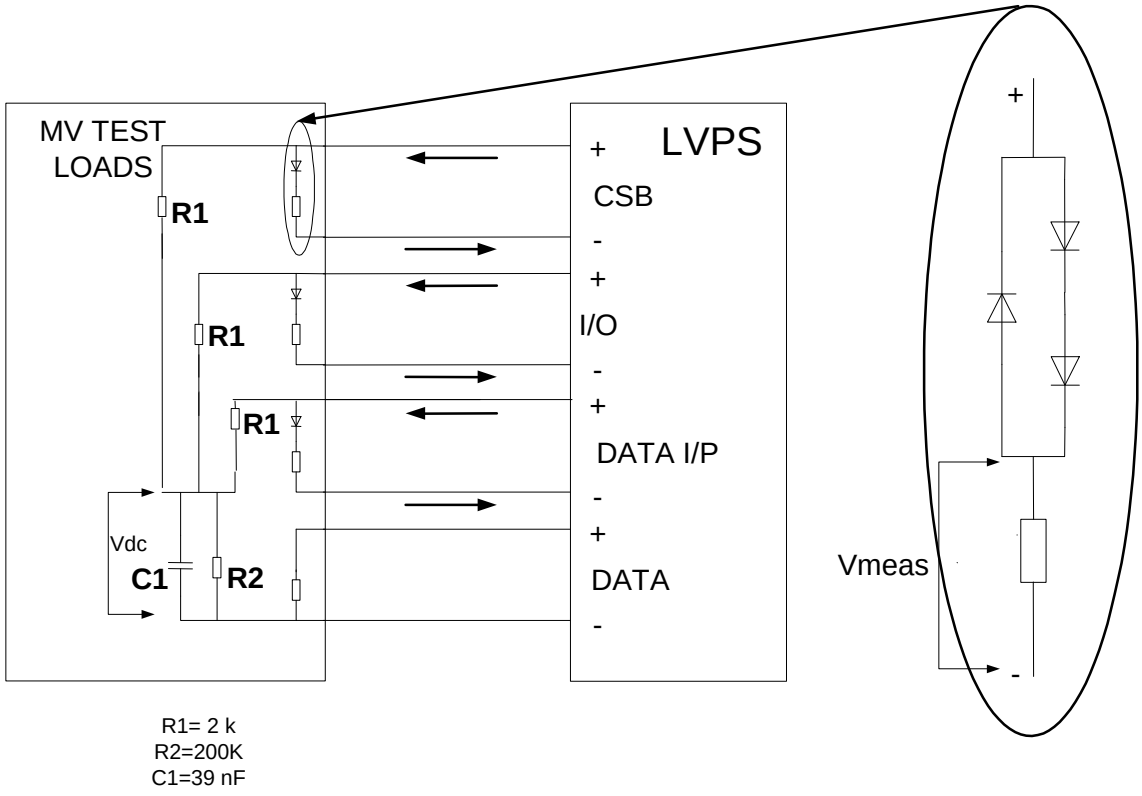


Figure 7 Test loading for LVPS for monitoring CSB, I/O CLOCK & DATA 1/P

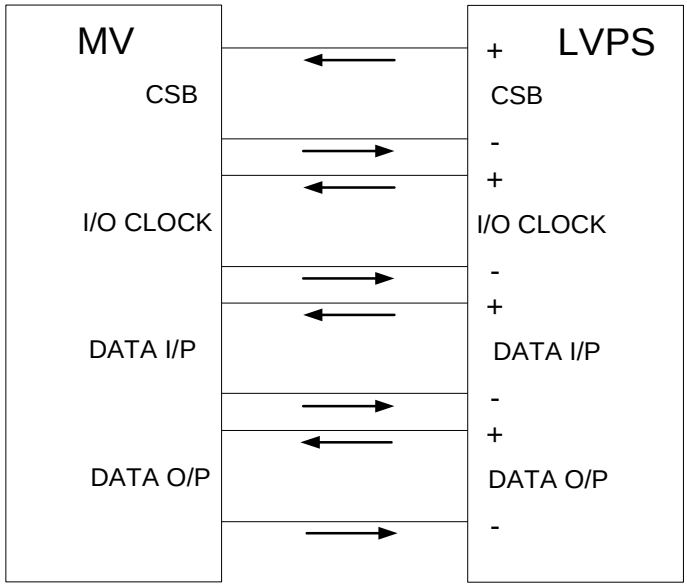


Figure 8 Test arrangement for MV/LVPS for monitoring I/O CLOCK & DATA O/P

I/O Pin annotations and MVC/LVPS connectivity

Table 4 I/O Pins and Connectivity

Function	MVC Pinouts	LVPS Pinouts	
I/O CLOCK	CLK1N	ISO_SPI_a_I/O_CLK	Y4
	CLK1P		Y3
CSB	CS1N	ISO_SPI_a_I/O_CS	Y2
	CS1P		Y1
DATA INPUT	DATAIN1N	ISO_SPI_a_I/O_DI	Y6
	DATAIN1P		Y5
DATA OUT	DATAOUT1N		Y8
	DATAOUT1P	ISO_SPI_a_I/O_DO	Y7
I/O CLOCK	CLK2N	ISO_SPI_b_I/O_CLK	Y12
	CLK2P		Y11
CSB	CS2N	ISO_SPI_b_I/O_CS	Y10
	CS2P		Y9
DATA INPUT	DATAIN2N	ISO_SPI_b_I/O_DI	Y14
	DATAIN2P		Y13
DATA OUT	DATAOUT2N		Y16
	DATAOUT2P	ISO_SPI_b_I/O_DO	Y15

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