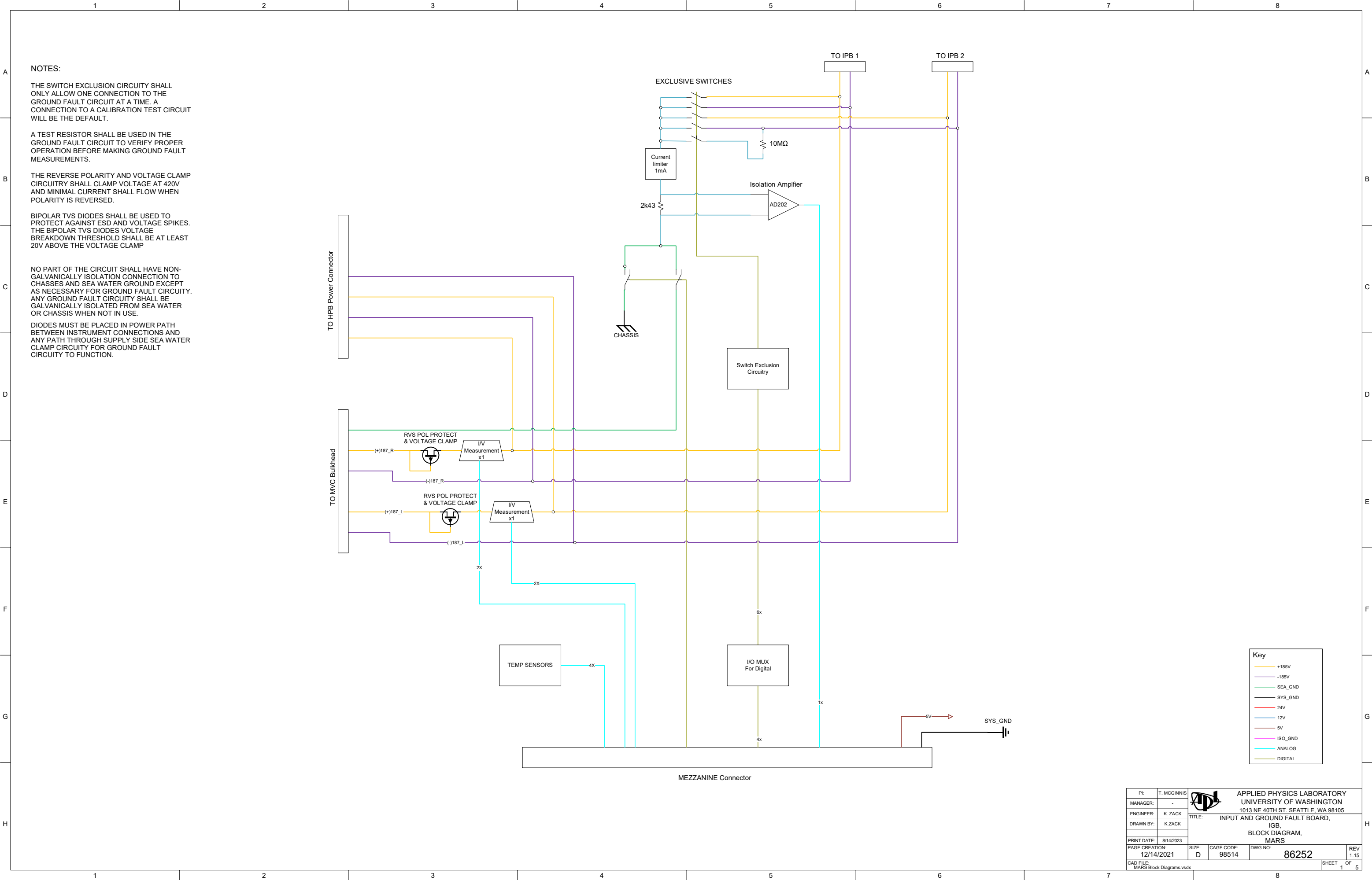
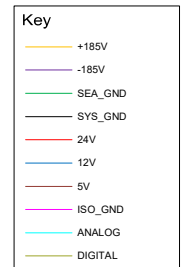




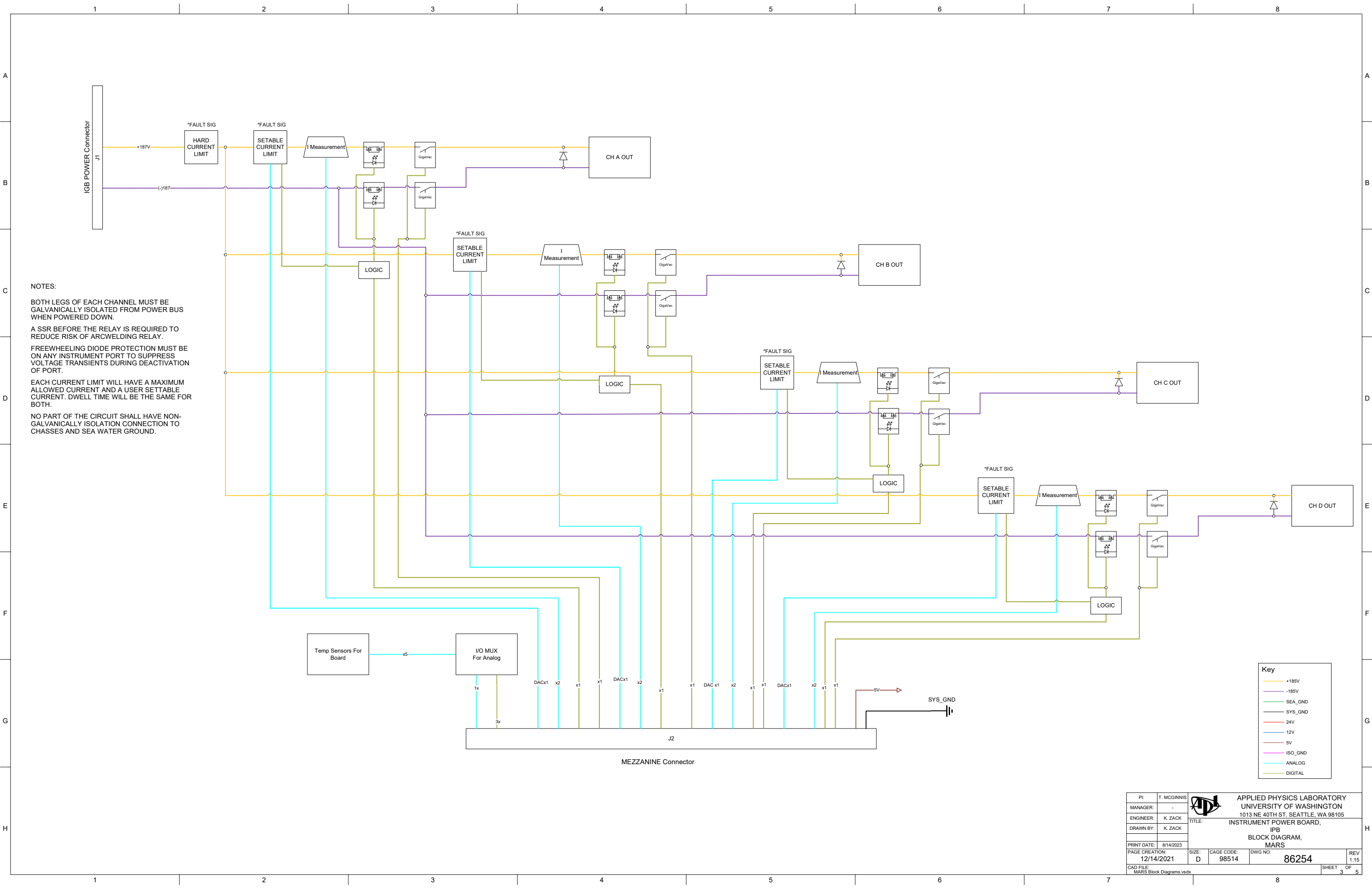
DIODES MUST BE PLACED IN POWER PATH BETWEEN INSTRUMENT CONNECTIONS AND ANY PATH THROUGH SUPPLY SIDE SEA WATER CLAMP CIRCUITRY FOR GROUND FAULT CIRCUITRY TO FUNCTION.

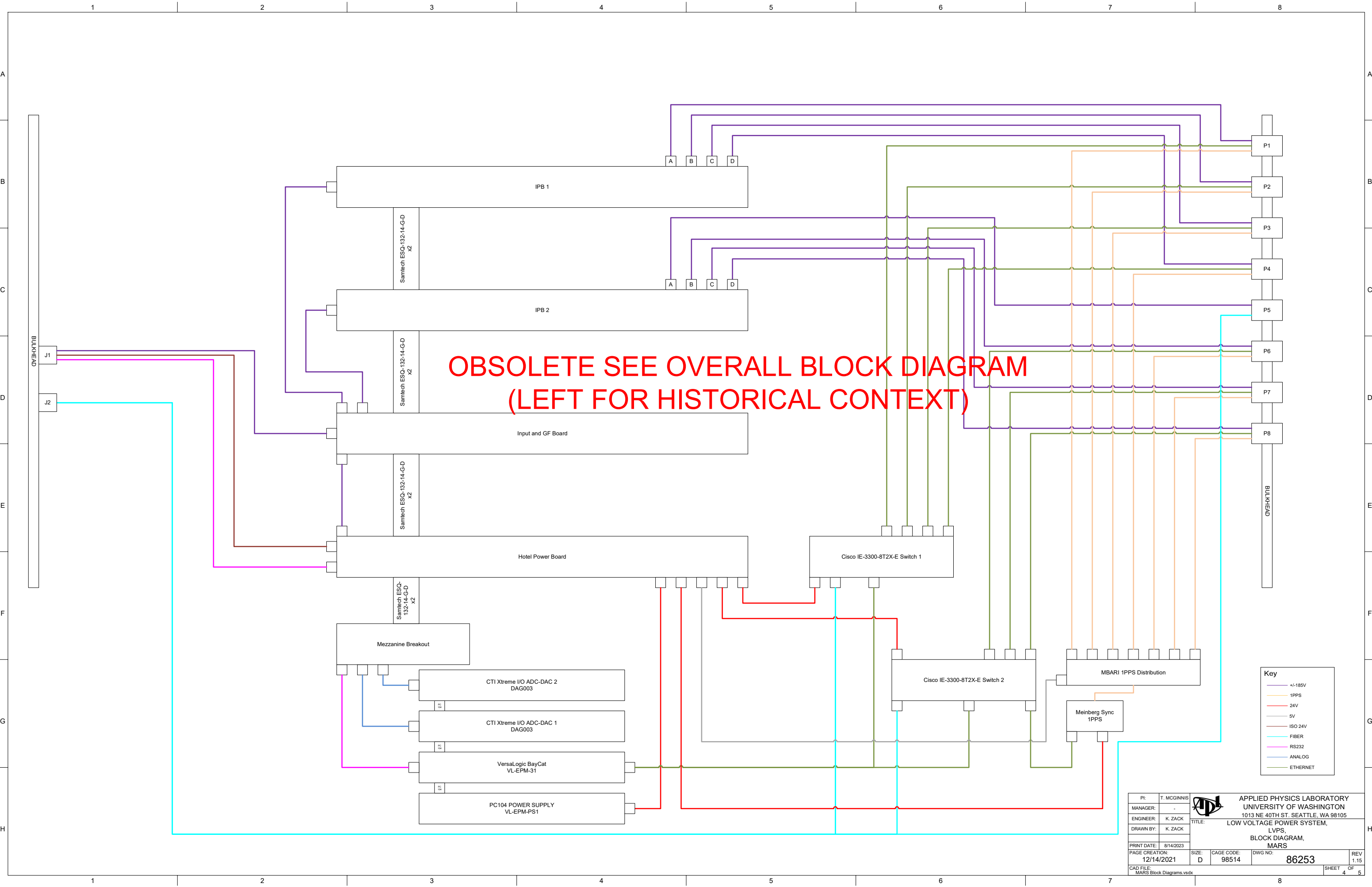
SWITCHED CIRCUITS SHALL HAVE CURRENT MEASUREMENTS. NON-SWITCHED CIRCUITS WILL BE PART OF THE BUS MEASUREMENTS

NO PART OF THE CIRCUIT SHALL HAVE NON-GALVANICALLY ISOLATION CONNECTION TO CHASSES AND SEA WATER GROUND.



PL:	T. MCGINNIS		APPLIED PHYSICS LABORATORY		
MANAGER:	-		UNIVERSITY OF WASHINGTON		
ENGINEER:	K. ZACK		1013 NE 40TH ST. SEATTLE, WA 98105		
DRAWN BY:	K. ZACK		TITLE: HOTEL POWER BOARD, HPB BLOCK DIAGRAM, MARS		
PRINT DATE:	8/14/2023				
PAGE CREATION:		SIZE:	CAGE CODE:	DWG NO:	REV
12/14/2021		D	98514	86253	1.15
CAD FILE:					SHEET
MARS Block Diagrams.vsdw					2 OF 5



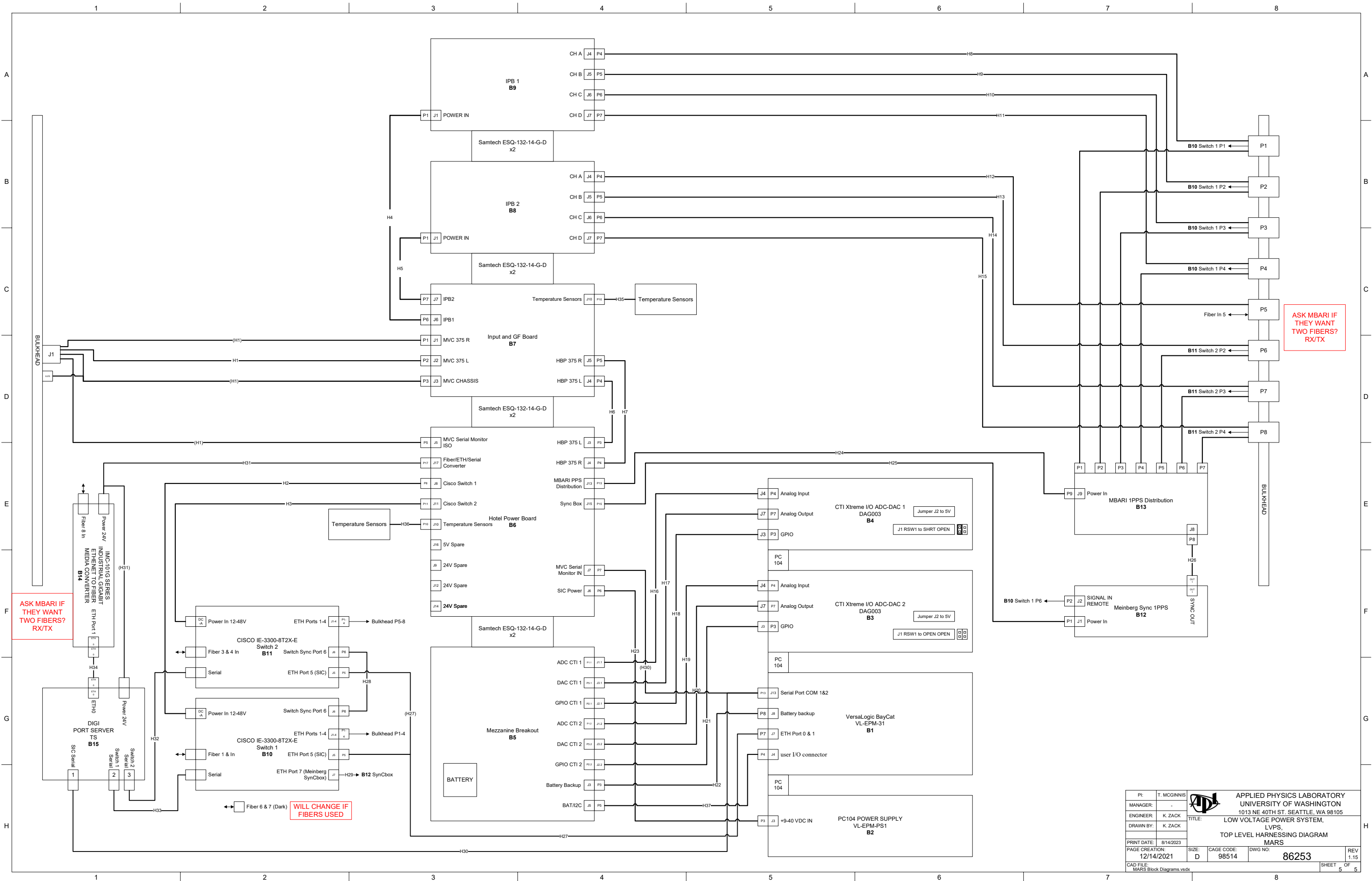


OBSOLETE SEE OVERALL BLOCK DIAGRAM
(LEFT FOR HISTORICAL CONTEXT)

Key

—	+/-185V
—	1PPS
—	24V
—	5V
—	ISO 24V
—	FIBER
—	RS232
—	ANALOG
—	ETHERNET

PI:	T. MCGINNIS		APPLIED PHYSICS LABORATORY		
MANAGER:	-		UNIVERSITY OF WASHINGTON		
ENGINEER:	K. ZACK		1013 NE 40TH ST. SEATTLE, WA 98105		
DRAWN BY:	K. ZACK		LOW VOLTAGE POWER SYSTEM,		
PRINT DATE:	8/14/2023			LVPs,	
PAGE CREATION:	12/14/2021			BLOCK DIAGRAM,	
CAD FILE:	MARS Block Diagrams.vsd			MARS	
SIZE:	D	CAGE CODE:	98514	DWG NO:	86253
REV:	1.15			SHEET	4 OF 5



PI:	T. MCGINNIS		APPLIED PHYSICS LABORATORY		
MANAGER:	-		UNIVERSITY OF WASHINGTON		
ENGINEER:	K. ZACK		1013 NE 40TH ST. SEATTLE, WA 98105		
DRAWN BY:	K. ZACK		TITLE: LOW VOLTAGE POWER SYSTEM, LVPS, TOP LEVEL HARNESSING DIAGRAM MARS		
PRINT DATE:	8/14/2023	SIZE:	D	CAGE CODE:	98514
PAGE CREATION:	12/14/2021	SIZE:	D	CAGE CODE:	98514
CAD FILE:	MARS Block Diagrams.vsd	DWG NO:	86253	REV	1.15
				SHEET	5 OF 5