

## ADS1271EVM & ADS1271EVM-PDK

This user's guide describes the characteristics, operation, and use of the ADS1271EVM, both by itself and as part of the ADS1271EVM-PDK. This EVM is a 24-bit analog-to-digital converter evaluation module. A complete circuit description, schematic diagram, and bill of materials are also included.

The following related documents are available through the Texas Instruments web site at [www.ti.com](http://www.ti.com).

### EVM-Compatible Device Data Sheets

| Device       | Literature Number        |
|--------------|--------------------------|
| ADS1271      | <a href="#">SBAS306</a>  |
| OPA350       | <a href="#">SBOS099B</a> |
| OPA1632      | <a href="#">SBOS286</a>  |
| REF1004      | <a href="#">SBVS002</a>  |
| REF3125      | <a href="#">SBVS046A</a> |
| SN74AVC1T45  | <a href="#">SCES530C</a> |
| SN74AVC2T45  | <a href="#">SCES531D</a> |
| SN74LVC1G125 | <a href="#">SCES223L</a> |
| SN74LVC2G66  | <a href="#">SCES325G</a> |
| SN74LVC2G157 | <a href="#">SCES207I</a> |
| TPS71550     | <a href="#">SLVS338H</a> |

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## 1 EVM Overview

### 1.1 Features

- Full-featured evaluation board for the ADS1271 24-bit Analog-to-Digital Converter
- Two ADS1271 converters on board illustrate use of daisy-chain mode
- On-board reference and oscillator circuits
- Modular design for use with a variety of DSP and microcontroller interface boards.
- ADS1271EVM-PDK is a complete evaluation kit, which includes a USB-based motherboard and evaluation software for use with a personal computer running Microsoft Windows™ operating systems.

### 1.2 Introduction

The ADS1271EVM is built in Texas Instruments' modular EVM form factor, which allows direct evaluation of the ADS1271 performance and operating characteristics, and eases software development and system prototyping. This EVM is compatible with the 5-6K Interface Board (SLAU104) from Texas Instruments and additional third-party boards such as the HPA449 demonstration board from SoftBaugh, Inc. ([www.softbaugh.com](http://www.softbaugh.com)) and the Speedy33™ from Hyperception, Inc. ([www.hyperception.com](http://www.hyperception.com)).

The ADS1271EVM-PDK is a complete evaluation/demonstration kit, which includes a USB-enabled DSP-based motherboard (the MMB0) and evaluation software for use with a PC.

## 2 Analog Interface

The ADS1271EVM features several analog input options. Signals can be routed directly to the converters or can pass through the on-board buffer amplifiers (U5, U6). Signals can be applied to the board through the standard modular EVM analog connector (J1) or brought in through the auxiliary input connectors (J4, J5). A set of switches selects which analog connector source is used and whether the buffer amplifiers are in the signal path. These switches enable several configurations for evaluation. Switch operation and analog path configuration are described in [Section 5.1](#).

For maximum flexibility, the ADS1271EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J1. This header/socket provides access to the analog input pins of the ADS1271. Consult Samtec at [www.samtec.com](http://www.samtec.com) or call 1-800-SAMTEC-9 for a variety of mating connector options. [Table 1](#) through [Table 3](#) summarize the standard and auxiliary analog pinout configurations.

**Table 1. Analog Interface Pinout (J1)**

| Pin Number         | Signal | Description                                |
|--------------------|--------|--------------------------------------------|
| J1.1               | AIN0N  | ADS1271 (U7) AINN                          |
| J1.2               | AIN0P  | ADS1271 (U7) AINP                          |
| J1.3               | AIN1N  | ADS1271 (U8) AINN                          |
| J1.4               | AIN1P  | ADS1271 (U8) AINP                          |
| J1.5               | Unused |                                            |
| J1.6               | Unused |                                            |
| J1.7               | Unused |                                            |
| J1.8               | Unused |                                            |
| J1.15              | Unused |                                            |
| J1.18              | REF(-) | External reference source low side         |
| J1.20              | REF(+) | External reference source input (2.5V NOM) |
| J1.9-J1.19 (odd)   | GND    | Analog ground connections (except J1.15)   |
| J1.10-J1.16 (even) | Unused |                                            |

**Table 2. Auxiliary Analog Input 1 Pinout (J4)**

| Pin Number | Signal   | Description                                     |
|------------|----------|-------------------------------------------------|
| J4.1       | AUX1P    | Auxiliary Signal Input 1 - Positive terminal    |
| J4.2       | AUX1N    | Auxiliary Signal Input 1 - Negative terminal    |
| J4.3       | AUXREF1P | Auxiliary Reference Input 1 - Positive terminal |
| J4.4       | AUXREF1N | Auxiliary Reference Input 1 - Negative terminal |
| J4.5       | GND      | Ground                                          |

**Table 3. Auxiliary Analog Input 2 Pinout (J5)**

| Pin Number | Signal   | Description                                     |
|------------|----------|-------------------------------------------------|
| J5.1       | AUX2P    | Auxiliary Signal Input 2 - Positive terminal    |
| J5.2       | AUX2N    | Auxiliary Signal Input 2 - Negative terminal    |
| J5.3       | AUXREF2P | Auxiliary Reference Input 2 - Positive terminal |
| J5.4       | AUXREF2N | Auxiliary Reference Input 2 - Negative terminal |
| J5.5       | GND      | Ground                                          |

### 3 Digital Interface

The ADS1271EVM is designed to easily interface with multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the ADS1271. Consult Samtec at [www.samtec.com](http://www.samtec.com) or call 1-800-SAMTEC-9 for a variety of mating connector options.

Because the ADS1271 devices are capable of daisy-chaining, this EVM has been designed to permit stacking; up to 4 EVMs can be stacked, allowing for 8 devices to be placed in a signal chain. To accommodate stacking of EVMs, J2 has some different connections on the top and the bottom side of the board. Differences between top and bottom connectors are highlighted in [Table 4](#).

**Table 4. Digital Interface Pinout (J2)**

| Pin Number | Signal                    | Description                                                                                                                             |
|------------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| J2.1       | SYNC                      | Synchronization Control                                                                                                                 |
| J2.2       | MODE0                     | 0 = High-Speed Mode<br>1 = Low-Power Mode<br>(In either case, only if Mode1=1)                                                          |
| J2.3       | CLKX                      | CLKXMODE = 1: master clock output<br>CLKXMODE = 0: no connection                                                                        |
| J2.4       | DGND                      | Digital ground                                                                                                                          |
| J2.5       | SCLK                      | Serial Clock                                                                                                                            |
| J2.6       | MODE1                     | 0 = High-Resolution Mode<br>1 = Mode determined by MODE0                                                                                |
| J2.7       | Unused.                   |                                                                                                                                         |
| J2.8       | FSDIR                     | Indicates FSR direction:<br>0 = Output (DRDY in SPI mode)<br>1 = Input (FSYNC mode)                                                     |
| J2.9       | Top: FSOUT<br>Bottom: FSR | FSOUT: in FSYNC mode, copy of FSR; in SPI mode, not connected<br>FSR: in FSYNC mode, frame-sync input; in SPI mode, DRDY output from U8 |
| J2.10      | DGND                      | Digital ground                                                                                                                          |
| J2.11      | Unused                    |                                                                                                                                         |
| J2.12      | CLKRMODE                  | 0 = Use CLKR for SPI Clock<br>1 = Use ADC Clock for SPI clock                                                                           |
| J2.13      | Top: DIN<br>Bottom: DOUT  | Top: Serial data input<br>Bottom: Serial data output                                                                                    |
| J2.14      | CLKXMODE                  | 0 = CLKX is High Z<br>1 = CLKX outputs ADC master clock                                                                                 |
| J2.15      | Unused                    |                                                                                                                                         |
| J2.16      | SCL                       | I <sup>2</sup> C bus serial clock                                                                                                       |
| J2.17      | EXTCLK                    | External ADC clock input                                                                                                                |
| J2.18      | DGND                      | Digital ground                                                                                                                          |
| J2.19      | OBCLKSEL                  | Onboard Clock Select:<br>High to select onboard clock instead of external clock.                                                        |
| J2.20      | SDA                       | I <sup>2</sup> C bus data line                                                                                                          |

## 4 Power Supplies

J3 provides connection to the common power bus for the ADS1271EVM. Power is supplied on the pins listed in [Table 5](#).

**Table 5. Power Supply Pinout**

| Signal                                        | Pin Number |    | Signal                                        |
|-----------------------------------------------|------------|----|-----------------------------------------------|
| +AVDD: +15V to power buffer amplifier section | 1          | 2  | –AVDD: –15V to power buffer amplifier section |
| +5VA                                          | 3          | 4  | Unused                                        |
| DGND                                          | 5          | 6  | AGND                                          |
| +1.8VD                                        | 7          | 8  | Unused                                        |
| +3.3VD                                        | 9          | 10 | +5VD                                          |

When power is supplied to J3, J6 allows for either 3.3V or 1.8V to be applied to the digital sections of the ADS1271. J6 also provides for a method of measuring AVDD and DVDD supply currents if the shunts on J6.1-2, J6.3-4, J6.5-6, and J6.7-8 are removed and a current meter is connected between the appropriate pins. See the schematic and printed circuit board silkscreen for details.

#### 4.1 ADC Power

Power for the ADS1271 analog supply voltage (AVDD) comes from +5V<sub>A</sub>, which is supplied through J3.3. The shunt from J6 pins 1 to 2 applies this supply to the U7 ADS1271 device, while the shunt from J6 pins 5 to 6 applies this supply to the U8 ADS1271.

The ADS1271 digital supply voltage (DVDD) is selected using J6. When a shunt is applied from J6 pins 9 to 10, +1.8V<sub>D</sub> is selected, and this power comes from J3.7. If a shunt is placed from J6 pins 11 to 12 (the default factory setting), +3.3V<sub>D</sub> is selected, which is provided from J3.9. J6 pins 13 and 15 provide a means of connecting analog and digital grounds to the EVM; these grounds come from J3.6 and J3.5, respectively. These grounds are always connected together at the EVM.

##### CAUTION

Verify that all power supplies are within the safe operating limits shown on the ADS1271 data sheet before applying power to the EVM. Note that a shunt should only be connected between J6 pins 9 and 10 **OR** pins 11 and 12, but never both; doing so would short the +3.3V supply to the +1.8V digital supply.

#### 4.2 Stand-Alone Operation

When used as a stand-alone EVM, the analog power can be applied to J6.2 and J6.6, referenced to J6.13. DVDD can be applied to J6.4 and J6.8, referenced to J6.15. Note that this EVM uses only a single ground plane.

#### 4.3 Reference Voltage

The ADS1271 requires an external voltage reference. Two switches, S3 and S5, select the source of the reference for the two ADS1271s on the EVM. An external reference may be supplied through J1 pin 20 on the ADS1271EVM, or through J4 and J5, the auxiliary analog input connectors. A 2.5V reference is provided on the EVM for convenience. These different reference sources can be selected using S3 and S5, as shown in [Table 6](#).

##### CAUTION

Verify that the external reference voltage is within the safe operating limits shown on the ADS1271 data sheet before applying power to the EVM.

**Table 6. Reference Selection Options - S3 and S5**

| S3/S5 Position | Reference Inputs                                                                     |
|----------------|--------------------------------------------------------------------------------------|
| Left           | Onboard 2.5V reference                                                               |
| Middle         | External Reference from J1.20 (REFP) referenced to J1.18 (REFN)                      |
| Right          | S3: AUXREF1 from J4.3 referenced to J4.4<br>S5: AUXREF2 from J5.3 referenced to J5.4 |

## 5 EVM Operation

The following section provides information on the analog input, digital control, and general operating conditions of the ADS1271EVM. Refer to [Figure 1](#) for switch and jumper locations, and the meanings of *left*, *middle* and *right* for switch settings in the following discussion.

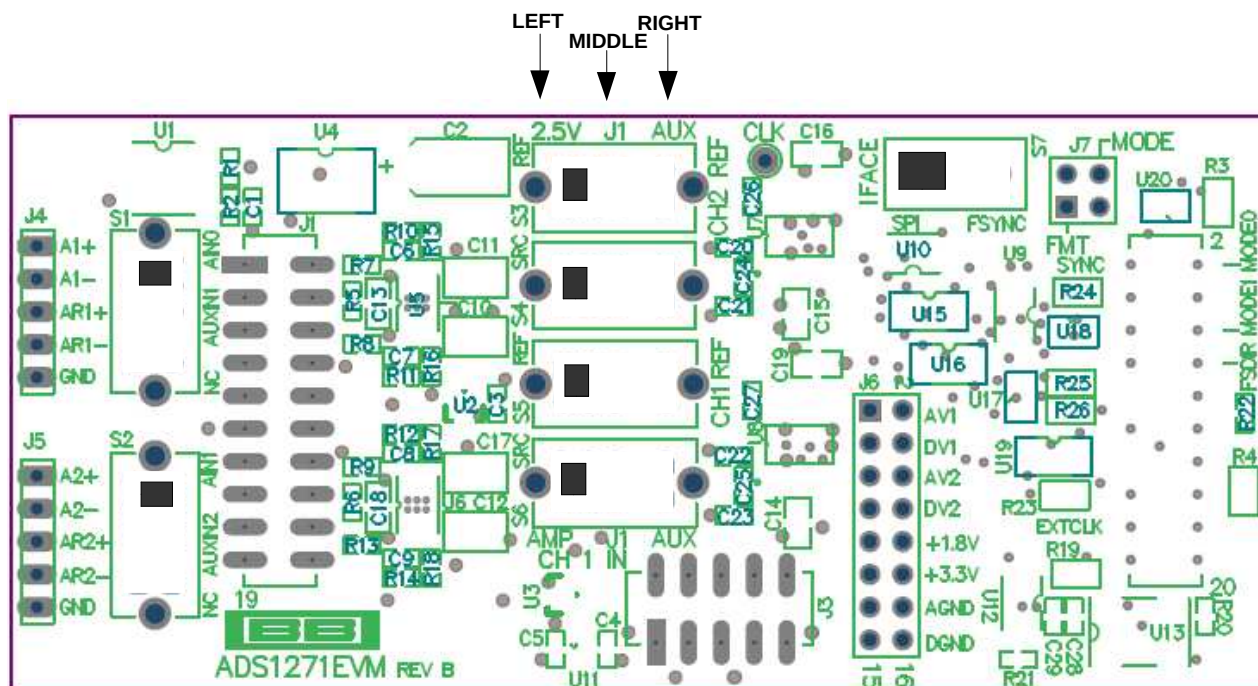


Figure 1. ADS1271EVM Switch and Jumper Locations

### 5.1 Analog Input

The analog input sources can be applied directly to J1 (top or bottom side) or through the auxiliary connectors J4 and J5. The analog input signals can be routed directly to the two ADS1271s on the EVM, or they can be routed through an optional buffer amplifier stage built around U5 or U6. Consult the ADS1271 data sheet to determine the maximum analog input range. [Table 7](#) summarizes the position of switches S1 and S2. S4 and S6 can be used to select the routing of the ADS1271 analog inputs as shown in [Table 8](#).

Table 7. Buffer Amplifier Options - S1 and S2

| S1/S2 Position | Analog Inputs                     |
|----------------|-----------------------------------|
| Top            | Input from J1                     |
| Middle         | Input from J4/J5 auxiliary inputs |
| Bottom         | No connection                     |

Table 8. ADC Analog Input Options - S4 and S6

| S4/S6 Position | Analog Inputs                     |
|----------------|-----------------------------------|
| Left           | Input from Buffer Amplifier       |
| Middle         | Input from J1                     |
| Right          | Input from J4/J5 auxiliary inputs |

### 5.1.1 Buffer Amplifiers

The buffer amplifiers on this EVM are OPA1632s (U5, U6). These amplifiers are optimized for AC performance and are configured as fully-differential unity gain buffers. They require  $\pm 15V$  supplies, which are provided from J3 pins 1 and 2.

The OPA1632 requires a common mode voltage, which is provided on this EVM by U2 and U3. Some users may not wish to use the buffer amplifier section and provide the  $\pm 15V$  supplies. If the  $\pm 15V$  supplies are not connected, then having a voltage on the  $V_{OCM}$  pins of the amplifiers would exceed their maximum ratings. Thus, U2 and U3 provide a separate 2.5V reference for the buffer amplifier section rather than using the same reference as the ADS1271, which would always be powered. For this reason, U2 and U3 power is provided through a separate regulator, U11.

## 5.2 Digital Control

The digital control signals can be applied directly to J2. The modular ADS1271EVM can also be connected directly to a DSP or microcontroller interface board, such as the HPA449. For a current list of compatible interface and/or accessory boards for the EVM or the ADS1271, see the relevant product folder on the TI web site.

## 5.3 Communication Modes

The ADS1271EVM has a digital routing network which can help simulate several possible system connections. The routing network also provides level-shifting, which allows the ADS1271 to be operated at any supported logic level regardless of the logic level used on J2. Note that you are not required to include this circuitry in your own designs; typically no glue logic is required to connect one or more ADS1271s to a processor.

### 5.3.1 Routing control

Routing is controlled by pins CLKRMODE, CLKXMODE, and OBCLKSEL on J2. CLKRMODE controls the direction and connection of CLKR. When CLKRMODE is low, CLKR is an input connected only to SCLK. When CLKRMODE is high, CLKR becomes an output connected to SCLK, and SCLK is tied to CLK. This connection can be useful in both FSYNC and SPI modes. A pulldown on CLKRMODE makes FSYNC mode the default setting.

When CLKXMODE is high, CLKX is an output connected to CLK. This setting is primarily useful for certain configurations using TI's McBSP, where CLKX can be used as a reference clock input for the serial port. When CLKXMODE is low, CLKX on J2 is unconnected. A pulldown on CLKXMODE makes this configuration the default.

OBCLKSEL selects between one of two master clock sources. When OBCLKSEL is high, the on-board clock is active and used for the master clock. When OBCLKSEL is low, the master clock is taken from EXTCLK on J2, and the on-board oscillator is disabled. A pulldown on OBCLKSEL makes this setting the default.

### 5.3.2 Using the ADS1271 communication modes

You can use either of the two ADS1271 interface modes with the ADS1271EVM. The interface modes are chosen manually using switch S7, and cannot be selected electrically.

The FSR and FSOUT pins on J2 operate differently depending on the communication mode. In SPI mode, FSR, which is on the socket on the bottom side of the board, carries the DRDY output signal from the first ADC (U8), the second ADC (U7) DRDY line is not connected, and the FSOUT pin on the header on the top side of the board is not connected. In FSYNC mode, the FSYNC pins of both ADCs are tied together, and the signal on FSR is copied to the top connector on pin FSOUT.

This arrangement allows the ADS1271EVM to be stacked with other ADS1271EVMs in either mode, as long as all boards in the stack are in the same mode.

A motherboard can sense which state the switch is in and configure itself appropriately by monitoring the FSDIR pin on J2. This pin is high when FSOUT is active and FSR is an input, and low when FSOUT is disconnected and FSR is an output (that is, it carries the DRDY signal).

## **5.4 Clock Source**

### **5.4.1 Onboard Oscillator**

The ADS1271 requires a clock. A 25MHz clock oscillator is provided on the EVM, and is selected as the clock source for the device when OBCLKSEL (J2.19) is high.

### **5.4.2 External Oscillator**

When OBCLKSEL (J2.19) is low, the clock source for the ADS1271 is provided from J2.17, and the on-board clock oscillator is shut down.

## **6 Kit Operation**

The following section provides information on using the ADS1271EVM-PDK, including setup, program installation, and program usage.

## 6.1 ADS1271EVM-PDK Block Diagram

A block diagram of the ADS1271EVM-PDK is shown in Figure 2. The evaluation kit consists of two printed circuit boards connected together. The motherboard is designated as the MMB0, while the daughtercard is the ADS1271EVM described previously in this manual.

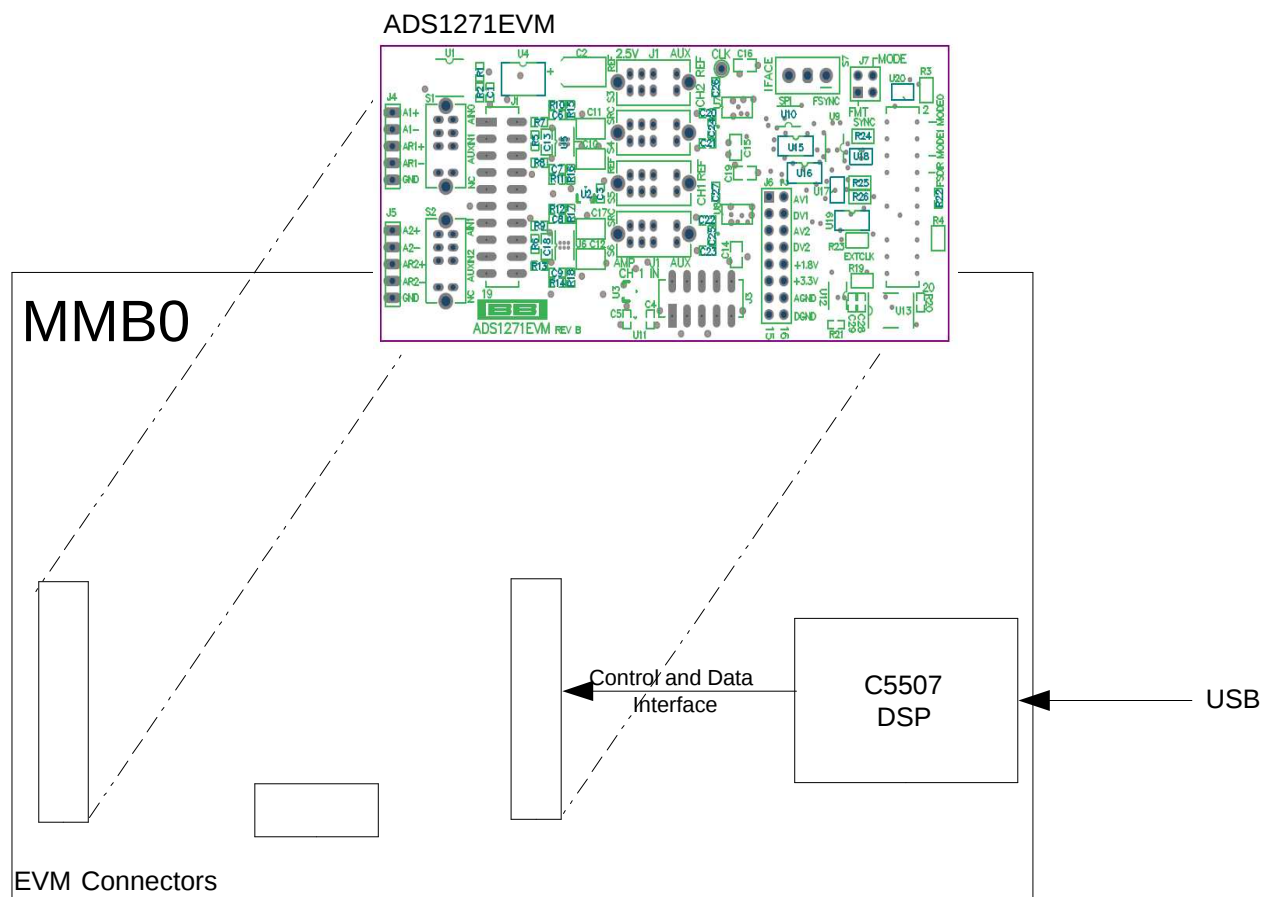


Figure 2. ADS1271EVM-PDK Block Diagram

## 6.2 Quick Start

Ensure that the ADS1271EVM is installed on the MMB0. Place the CD-ROM into your PC CD-ROM drive. Locate the Setup program on the disk and execute it. The Setup program installs the ADS1271 evaluation software on your PC. Follow the instructions and prompts given.

After the main program is installed, a dialog box appears with instructions for installing NI-VISA 3.1 Runtime, a self-extracting archive. Click OK to proceed. A WinZip™ dialog appears. Click *Unzip*, and the archive extracts itself and automatically runs the NI-VISA 3.1 Runtime installer.

Follow the instructions in the NI-VISA 3.1 Runtime Installer. When prompted for which features to install, do the following:

1. Click on the disk icon next to NI-VISA 3.1
2. Select, **Do not install this feature.**
3. Click on the disk icon next to USB.
4. Select the option which installs this feature.
5. Click *Next*.

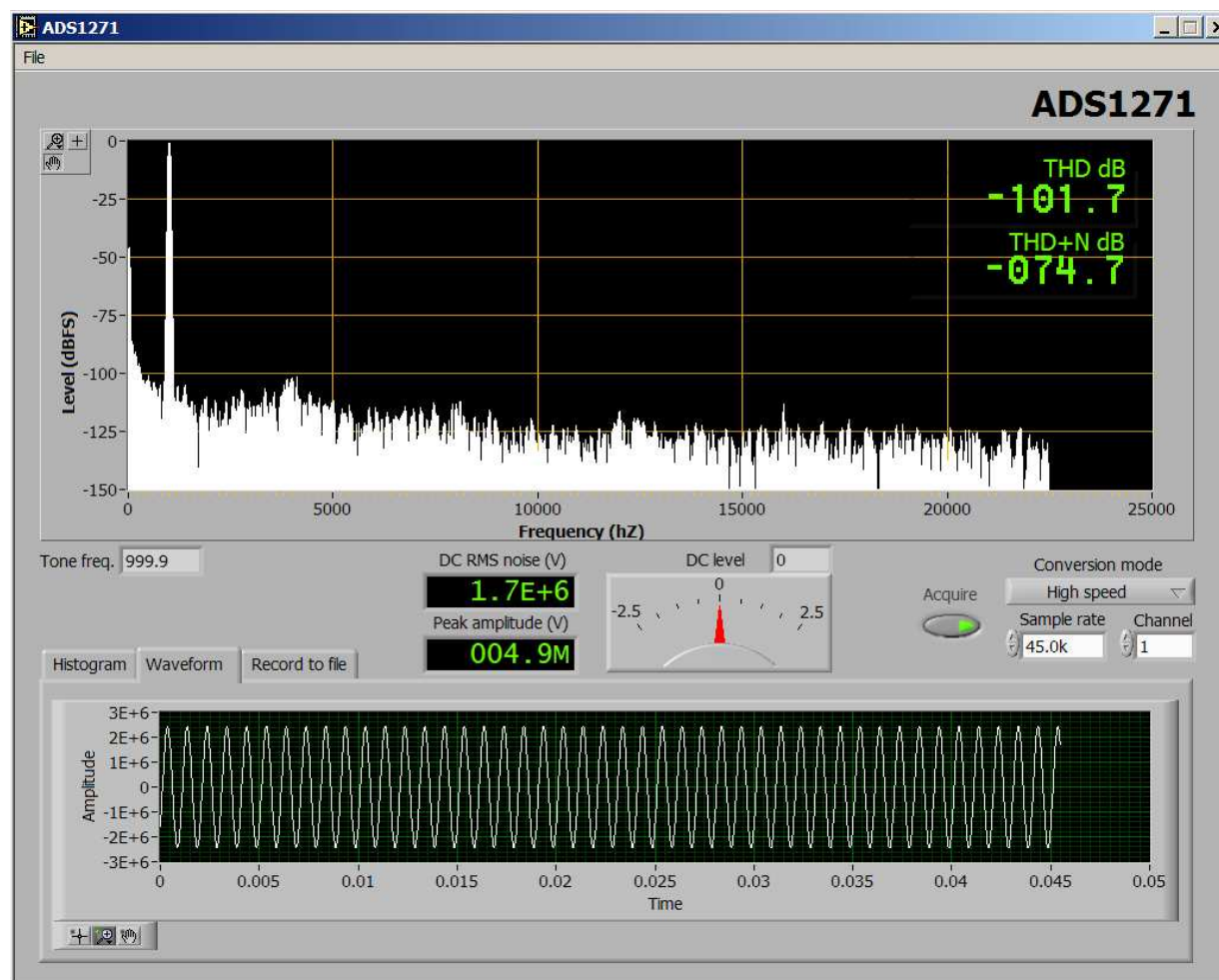
Accept the license agreement, and continue the installation.

## Kit Operation

When the installation completes, click *Finish* on the ADS1271EVM installer window. You may be prompted to restart your computer.

When installation is complete, attach a USB cable from your PC to the MMB0. Supply power to J14 on the MMB0, following the silkscreen markings or schematic; this will supply the ADS1271EVM power through the J3 connector on the ADS1271EVM.

The software should automatically find the ADS1271EVM, and a screen similar to the one in [Figure 3](#) should appear.



**Figure 3. Default Software Screen**

## 6.3 Program Description

Once the ADS1271EVM-PDK software (described in [Section 6.2](#)) is installed, evaluation and development with the ADS1271 can begin.

### 6.3.1 Basic Usage

When the program runs, it checks to see whether an MMB0 is connected. If it is, the program downloads the firmware to it, and runs; otherwise, it shows a dialog box telling you that it cannot find an MMB0. If you see this, make sure the MMB0 is connected and powered on, correct this if necessary, and click *Retry*. If you cannot fix the problem, click *Cancel* to quit.

After the program loads the MMB0 successfully, you will see a screen similar to that shown in [Figure 3](#). The top display shows an FFT of the ADC output up to the Nyquist frequency (half the sampling rate), and certain AC analysis numbers. Below this are a number of controls and meters, and at the bottom is a set of tabs, which show either a histogram, a picture of the incoming waveform, or the data recording controls.

To exit the program, select **File -> Exit** from the menu bar.

When the program starts, it is idle. You can put it in either Acquire mode or Record mode.

### 6.3.1.1 Acquire Mode

To put the program into Acquire mode, click the *Acquire* button. In Acquire mode, the ADS1271EVM software collects data as quickly as possible from the board in 2,048-sample blocks and analyzes it. Both AC and DC analyses are performed.

In Acquire mode, you can only view the data from one channel at a time. To choose channels, use the Channel box.

AC analysis consists of the FFT display and THD analysis. For THD analysis to work, the input must be a sine wave below half the Nyquist frequency, since the THD analyzer needs at least one harmonic to work from. The THD analyzer uses an automatic tone-detection algorithm, which searches for the highest harmonic and uses that for THD analysis. The frequency it detects is shown in the indicator marked *Tone Freq*. This frequency may not be exactly what your oscillator is set for, but it should generally be very close.

For DC analysis, the program provides DC RMS noise (standard deviation), peak amplitude, and a DC level meter. A histogram is also provided; this is visible in the left tab. Basic DC measurements work best when the ADC is driven by an amplifier or stable voltage source; shorting the inputs also works.

### 6.3.1.2 Record Mode

To record data, go to the Record To File tab and do the following:

1. If Acquire is on, turn it off. You cannot start recording when Acquire is on.
2. Set the Conversion Mode and Sample Rate fields to the settings you want to record with. The channel selector has no effect for data recording.
3. Enter a path in the *Destination File* field. You can use the folder icon to browse for the file with a standard file dialog. If the file you enter cannot be opened or created, the record button will be disabled. If the path points to an existing file, the file will be overwritten when you activate recording.
4. Enter a number of samples to convert. You can enter this in time or number of samples; the other box will update automatically. The number of samples is limited by available memory on the MMB0.
5. Click the record button. You will see the *Samples Retrieved* bar graph increase. When it reaches the number of samples you selected, recording will stop and the record button will go dark.

After this, the file you selected will contain comma-separated decimal numbers collected from the ADCs. The samples are written two to a line, with the sample from Channel 1 first, followed by a comma, followed by the sample from Channel 2. This kind of file can easily be imported into a spreadsheet, among other applications.

### 6.3.1.3 Configuration

You can set the sample rate and conversion mode. Sample rate and conversion mode are always the same for each ADS1271 being evaluated; you cannot set one channel to a different parameter.

The ADS1271's three conversion modes are selected from the flip-menu labelled *Conversion Mode*.

The ADS1271 clock is normally generated by a PLL synthesizer on the MMB0. The synthesizer cannot synthesize all frequencies precisely; the software will come as close as it can, but in some cases the sample rate will be slightly off.

When you change the sample rate, you may find the value clamped or altered. The limits are different for high-speed mode: in that mode, the maximum sampling rate is approximately 105ksps, but in the other modes, it is approximately 52.5ksps. If you have the sampling rate set too high when you switch to another mode, the program will automatically reduce the rate to the maximum rate allowed for that mode.

Note that the block size does not change. When you reduce the sampling rate, waveforms will appear to go up in frequency.

## 7 EVM Bill of Materials and Schematic

The following table contains a complete bill of materials for the modular ADS1271EVM.

**Table 9. ADS1271EVM Bill of Materials**

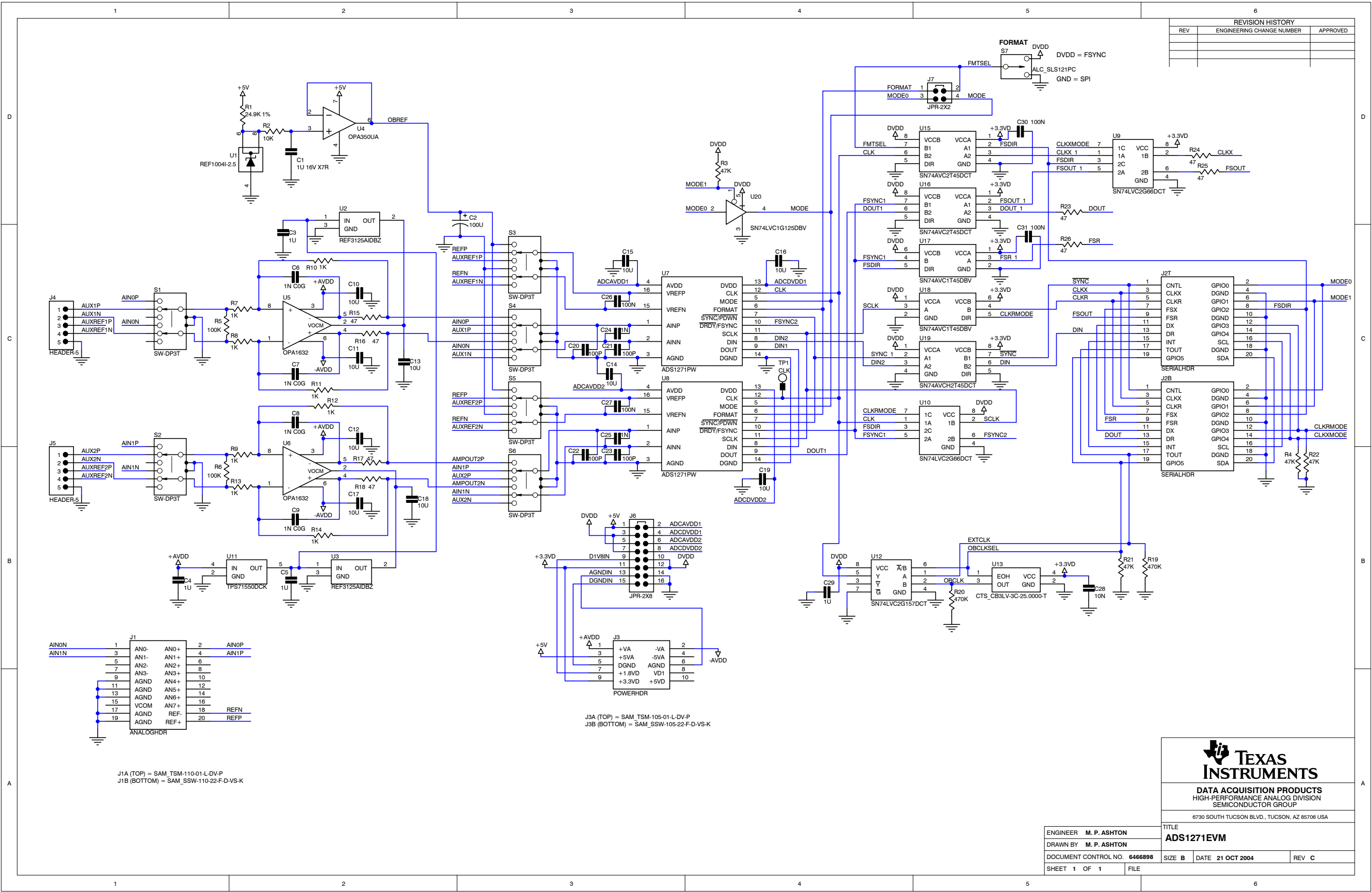
| Designators                            | Description                                   | Manufacturer      | Mfg. Part Number   |
|----------------------------------------|-----------------------------------------------|-------------------|--------------------|
| R15, R16, R17, R18, R23, R24, R25, R26 | 47Ω 1/8W 5% Chip Resistor                     | Panasonic         | ERJ-3GEYJ470V      |
| R7, R8, R9, R10, R11, R12, R13, R14    | 1KΩ 1/16W 1% Chip Resistor                    | Panasonic         | ERJ-3EKF1001V      |
| R2                                     | 10KΩ 1/10W 5% Chip Resistor                   | Panasonic         | ERJ-3GEYJ103V      |
| R1                                     | 24.9KΩ 1/16W 1% Chip Resistor                 | Panasonic         | ERJ-3EKF2492V      |
| R3, R4, R21, R22                       | 47KΩ 1/10W 5% Chip Resistor                   | Panasonic         | ERJ-3GEYJ473V      |
| R5, R6                                 | 100KΩ 1/10W 5% Chip Resistor                  | Panasonic         | ERJ-3GEYJ104V      |
| R19, R20                               | 470KΩ 1/10W 5% Chip Resistor                  | Panasonic         | ERJ-3GEYJ474V      |
| C20, C21, C22, C23                     | 100pF 50V Ceramic Chip Capacitor, ±5%, C0G    | TDK               | C1608C0G1H101JT    |
| C6, C7, C8, C9, C24, C25               | 1nF 50V Ceramic Chip Capacitor, ±5%, C0G      | TDK               | C1608C0G1H102JT    |
| C28                                    | 0.01μF 50V Ceramic Chip Capacitor, ±5%, X7R   | TDK               | C1608X7R1H103KT    |
| C26, C27, C30, C31                     | 0.1μF 50V Ceramic Chip Capacitor, ±10%, X7R   | TDK               | C1608X7R1H104KT    |
| C1, C3, C4, C5, C29                    | 1μF 16V Ceramic Chip Capacitor, ±10%, X7R     | TDK               | C1608X7R1C105KT    |
| C13, C14, C15, C16, C18, C19           | 10μF 6.3V Ceramic Chip Capacitor, ±20%, X5R   | TDK               | C2012X5R0J106MT    |
| C10, C11, C12, C17                     | 10μF 25V Ceramic Chip Capacitor, ±20%, X5R    | TDK               | C3225X7R1E106MT    |
| C2                                     | 100μF 10V Low ESR Tantalum Capacitor, ±20%    | Kemet             | T520D107M010ASE055 |
| U1                                     | Precision Voltage Reference                   | Texas Instruments | REF1004I-2.5       |
| U2, U3                                 | Precision Voltage Reference                   | Texas Instruments | REF3125AIDBZ       |
| U4                                     | Precision Operational Amplifier               | Texas Instruments | OPA350UA           |
| U5, U6                                 | Fully Differential Amplifier                  | Texas Instruments | OPA1632DGN         |
| U7, U8                                 | Precision Delta-Sigma ADC                     | Texas Instruments | ADS1271IPW         |
| U9, U10                                | Dual Analog Switch                            | Texas Instruments | SN74LVC2G66DCT     |
| U11                                    | LDO Voltage Regulator, High Input Voltage     | Texas Instruments | TPS1550DCK         |
| U12                                    | Single, 2-Line to 1 Data Selector/Multiplexer | Texas Instruments | SN74LVC2G157DCT    |
| U13                                    | 3.3V Oscillator                               | CTS               | CB3LV-5I-27-M0000  |
| U15, U16                               | Dual Split Rail Level Shifter Transceiver     | Texas Instruments | SN74AVC2T45DCT     |
| U17, U18                               | Split Rail Level Shifter Transceiver          | Texas Instruments | SN74AVC1T45DBV     |

**Table 9. ADS1271EVM Bill of Materials (continued)**

| Designators            | Description                               | Manufacturer         | Mfg. Part Number    |
|------------------------|-------------------------------------------|----------------------|---------------------|
| U19                    | Dual Split Rail Level Shifter Transceiver | Texas Instruments    | SN74AVCH2T45DCT     |
| U20                    | Tri-State Buffer                          | Texas Instruments    | SN74LVC1G125DBV     |
|                        | ADS1271EVM PCB                            | Texas Instruments    | 6466987             |
| J1A, J2T               | 20-pin SMT Plug                           | Samtec               | TSM-110-01-L-DV-P   |
| J1B, J2B               | 20-pin SMT Socket                         | Samtec               | SSW-110-22-F-D-VS-K |
| J3A                    | 10-pin SMT Plug                           | Samtec               | TSM-105-01-L-DV-P   |
| J3B                    | 10-pin SMT Socket                         | Samtec               | SSW-105-22-F-D-VS-K |
| J4, J5                 | Terminal Strip, 5 pin (5x1), Right Angle  | Samtec               | TSW-105-08-L-S-RA   |
| J6                     | Terminal Strip, 16-pin (8x2)              | Samtec               | TSW-108-07-L-D      |
| J7                     | Terminal Strip, 4-pin (2x2)               | Samtec               | TSW-102-07-L-D      |
| S1, S2, S3, S4, S5, S6 | Dual Pole 3 Position Switch               | E-Switch             | EG2305A             |
| S7                     | SPDT Switch                               | Tyco-Alcoswitch      | SLS121PC            |
| TP1                    | Miniature Test Point Terminal             | Keystone Electronics | 5000                |
|                        | Header Shorting Block                     | Samtec               | SNT-100-BK-T        |

## 7.1 ADS1271EVM Schematic

The schematic diagram is provided as a reference.



| REVISION HISTORY |                           |          |
|------------------|---------------------------|----------|
| REV              | ENGINEERING CHANGE NUMBER | APPROVED |
|                  |                           |          |
|                  |                           |          |
|                  |                           |          |

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|                      |              |       |             |
|----------------------|--------------|-------|-------------|
| ENGINEER             | M. P. ASHTON | TITLE | ADS1271EVM  |
| DRAWN BY             | M. P. ASHTON | SIZE  | B           |
| DOCUMENT CONTROL NO. | 6466898      | DATE  | 21 OCT 2004 |
| SHEET                | 1 OF 1       | FILE  | REV C       |

## FCC Warnings

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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During normal operation, some circuit components may have case temperatures greater than 30 °C. The EVM is designed to operate properly with certain components above 85 °C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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