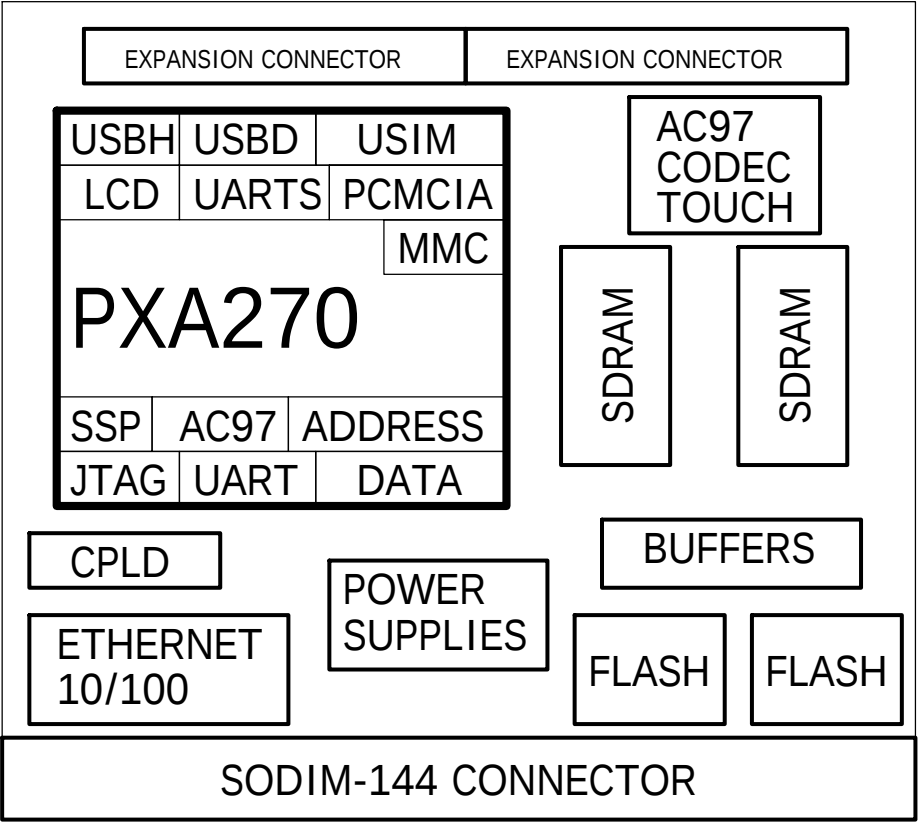


PROJECT:	PXA270-10
PART NUMBER:	1000076
ASSEMBLY NAME:	PXA270-10 CARD ENGINE
SCHEMATICS:	KTL
TABLE OF CONTENTS	
PAGE	DESCRIPTION
1	TITLE PAGE AND BLOCK DIAGRAM
2	CONNECTORS
3	BUFFERS
4	SDRAM
5	FLASH
6	WIRED LAN
7	CPLD
8	PERIPHERAL CIRCUITS
9	CODEC
10	PROCESSOR
11	TEST POINTS

COLOR LEGEND
NOTE: NOTES IN GREEN TEXT ARE GENERAL DESIGN OR SCHEMATIC NOTES
LAYOUT NOTE: NOTES IN RED TEXT ARE PCB LAYOUT RECOMMENDATIONS OR GUIDLINES
NET NAMES NET NAMES IN GREEN TEXT ARE NETS THAT ARE NOT DIRECTLY CONNECTED WITH A VISIBLE WIRE ON SINGLE SCHEMATIC PAGE, BUT USE THIS CONVENTION TO MAKE THE SCHEMATIC EASIER TO READ
NET NOTE NET NOTES IN BLACK TEXT INDICATE A PARTICULAR FUNCTIONALITY OF A SPECIFIC NET, IT IS NOT A NET NAME MERELY TEXT AND HAS NO AFFECT ON THE DRC.



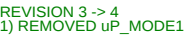
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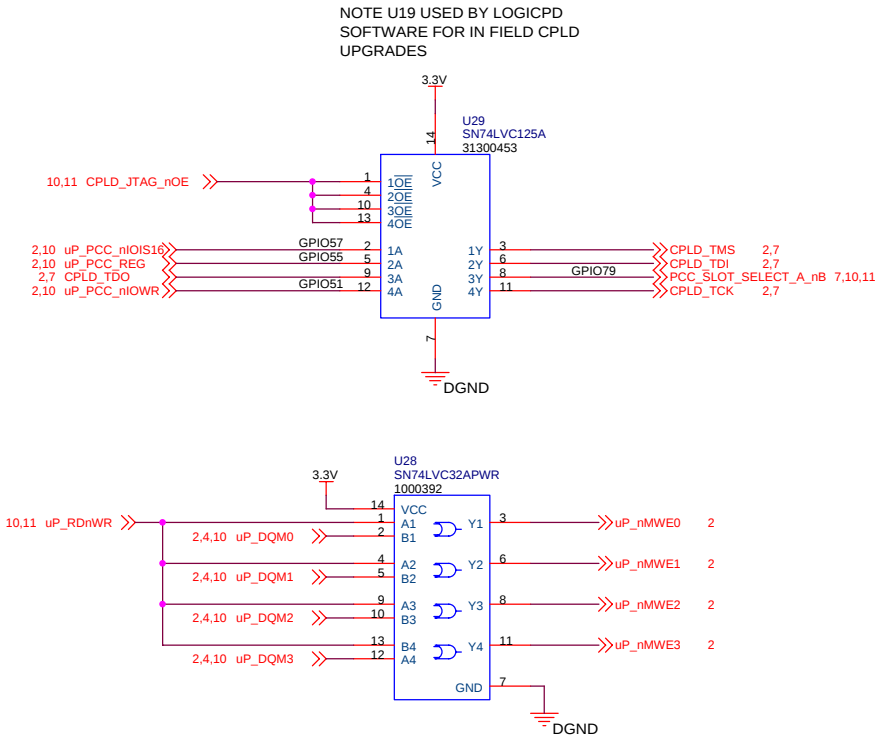
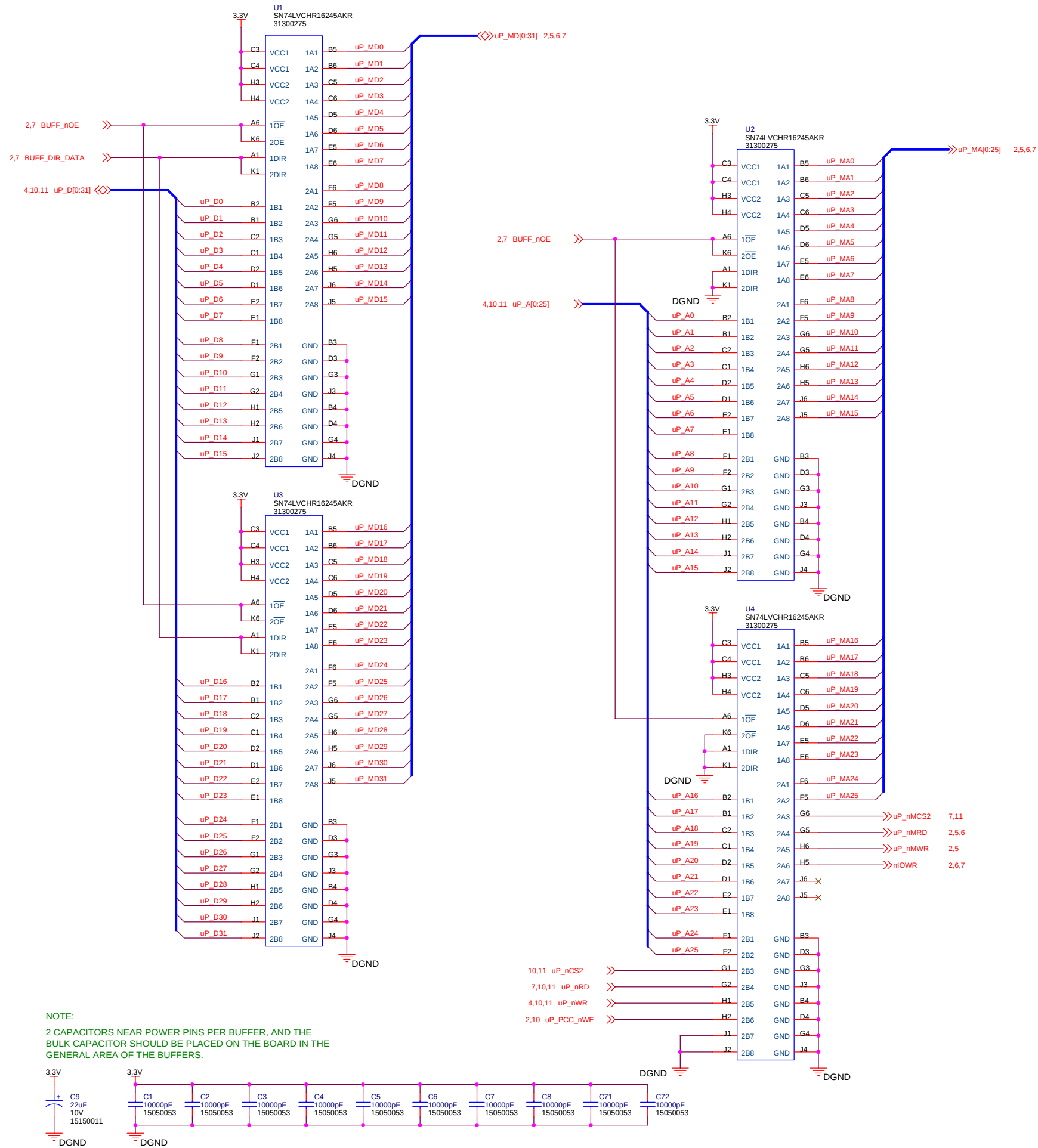
		LOGIC PRODUCT DEVELOPMENT	411 WASHINGTON AVE. N MINNEAPOLIS, MN 55401 PHONE: (612) 672-9495 FAX: (612) 672-9489
Title PXA270-10 CARD ENGINE			
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03 - BUFFERS



REVISION 4 -> A
1) U29 JAM PLAYER CHANGED CONTROL SIGNALS FROM LCD TO PCMCIA MUXED SIGNALS

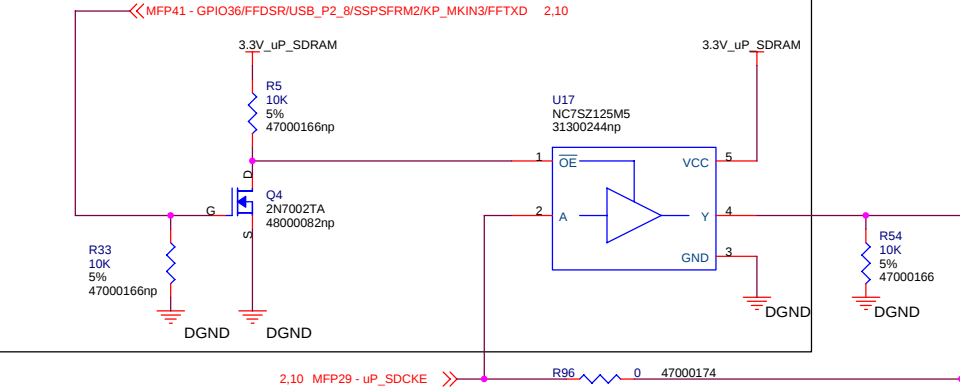
2) TIED U4 PIN K4 TO GND

REVISION 2 -> 3
1) MOVED LCD SIGNALS ON U19 TO MATCH CHANGES MADE ON PAGE 10
2) ADDED U28 AND MOVED FOR nWE OUTPUTS
3) MOVED uP_nCS2, uP_nRD, uP_nWR, uP_PCC_nWE FROM U19 TO U4
4) REMOVED U19, ADDED U29

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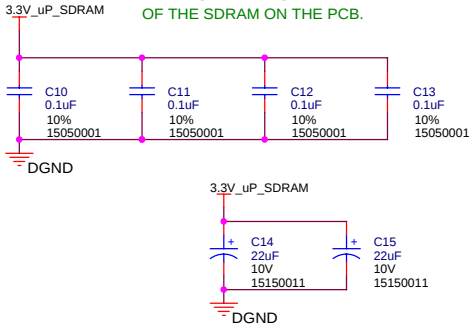
04 - SDRAM

NOTE: DEFAULT IS NOT POPULATED

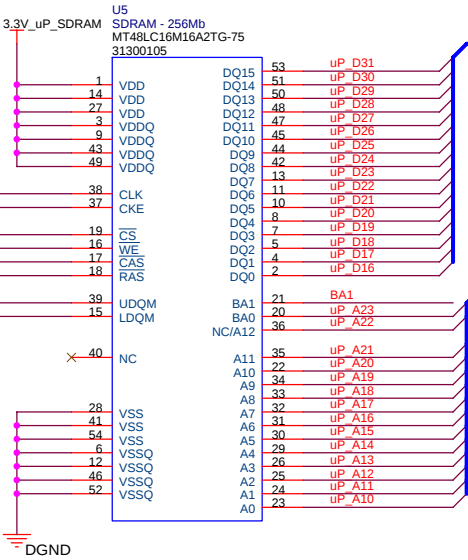


ENGINE DENSITY	CONFIG	RESISTOR	PART #
16 MByte		R93	MT48LC4M16A2TG-75
32 MByte		R93	MT48LC8M16A2TG-75
64 MByte	STANDARD	R7	MT48LC16M16A2TG-75
128 MByte		R7	MT48LC32M16A2TG-75

NOTE:
TWO .1uF DECOUPLING CAPS
PER CHIP, TWO BULK CAPS TO
BE PLACE IN THE GENERAL AREA
OF THE SDRAM ON THE PCB.



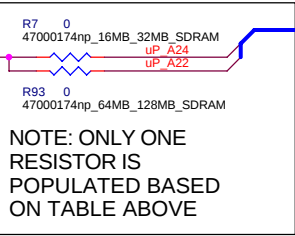
10 uP_SD_CLK
7.10.11 uP_nSDCS0
3.10.11 uP_nWR
2.5.10 uP_nCAS
2.10 uP_nRAS
2.3.10 uP_DQM3
2.3.10 uP_DQM2



uP_D[0:31] 3.10.11

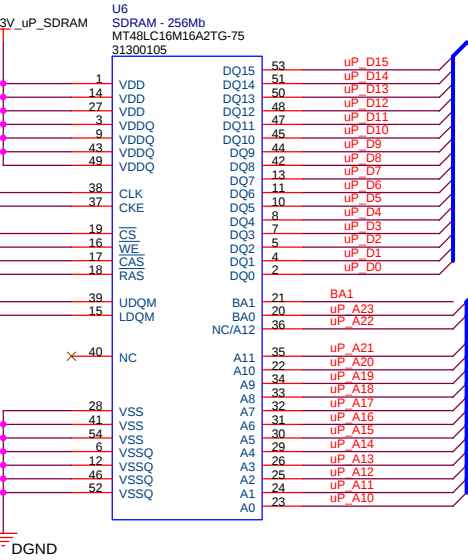
uP_A[0:25] 3.10.11

11



NOTE: ONLY ONE
RESISTOR IS
POPULATED BASED
ON TABLE ABOVE

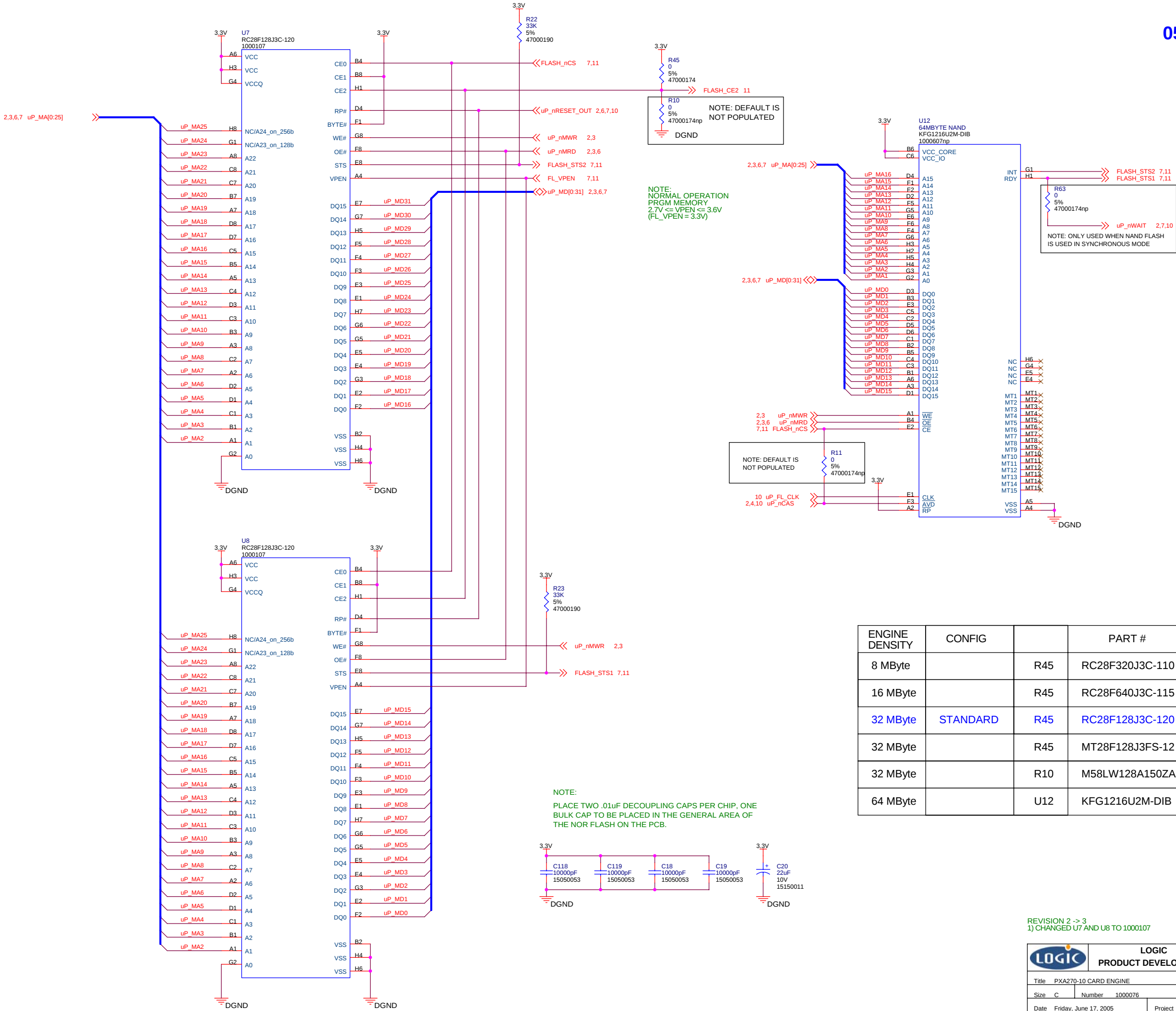
2.3.10 uP_DQM1
2.3.10 uP_DQM0



uP_D[0:31] 3.10.11

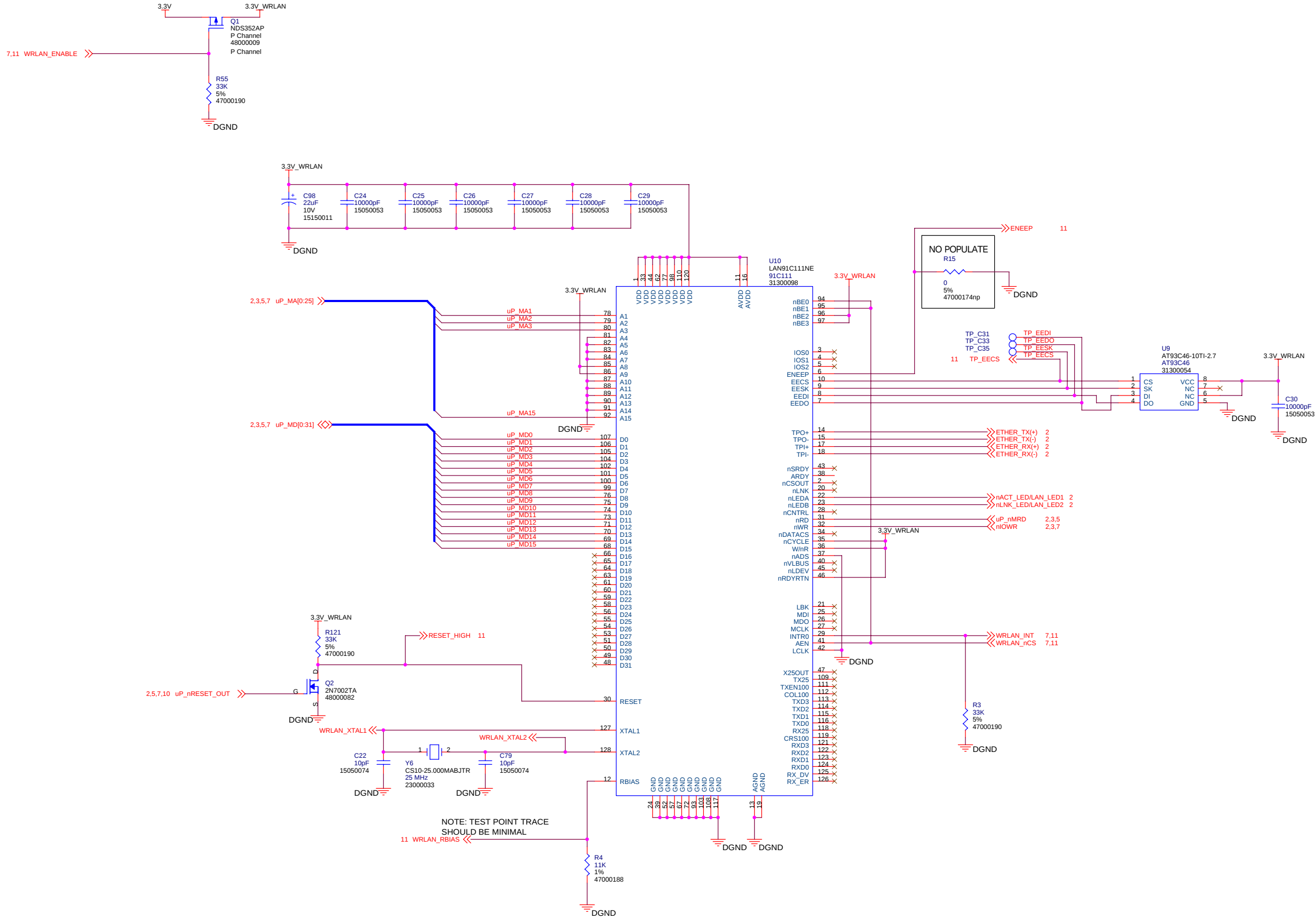
uP_A[0:25] 3.10.11

05 - FLASH



ENGINE DENSITY	CONFIG		PART #
8 MByte		R45	RC28F320J3C-110
16 MByte		R45	RC28F640J3C-115
32 MByte	STANDARD	R45	RC28F128J3C-120
32 MByte		R45	MT28F128J3FS-12
32 MByte		R10	M58LW128A150ZA1
64 MByte		U12	KFG1216U2M-DIB

06 - WIRED LAN



07 - CPLD

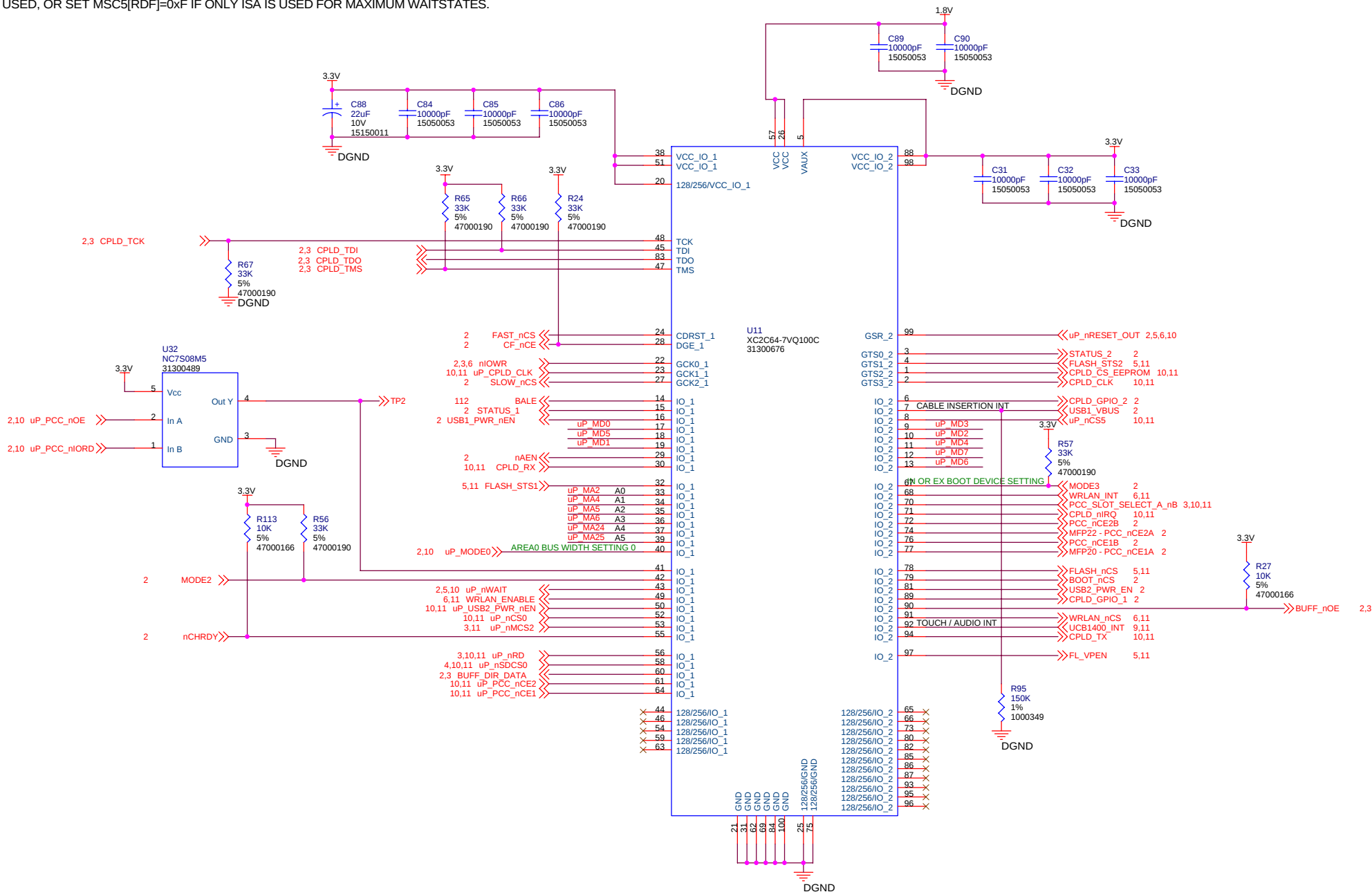
uP_nCS2 IS MAIN CHIP SELECT, 32 BIT AREA IN MAINSTONE BSP
uP_nCS5 USED FOR CF AND ISA INTERFACES

USE VLIO INTERFACE TO CREATE CF AND ISA TIMINGS -> ONLY NEED TO EXTEND THE CF_nCS AND nAEN SIGNAL BY 1 CLOCK CYCLE.

CF: MSC5[RDN]=0x3, MSC5[RRR]=0x1, MSC5[RDF]=0xC

ISA: MSC5[RDN]=0x3, MSC5[RRR]=0x1, MSC5[RDF]=0xF

LOGIC BSP SETS MSC5[RDF]=0xC FOR CF SUPPORT. ISA USERS MUST ASSERT uP_nWAIT TO EXTEND CYCLE TO MEET DESIRED ISA TIMING IF BOTH INTERFACES ARE USED, OR SET MSC5[RDF]=0xF IF ONLY ISA IS USED FOR MAXIMUM WAITSTATES.

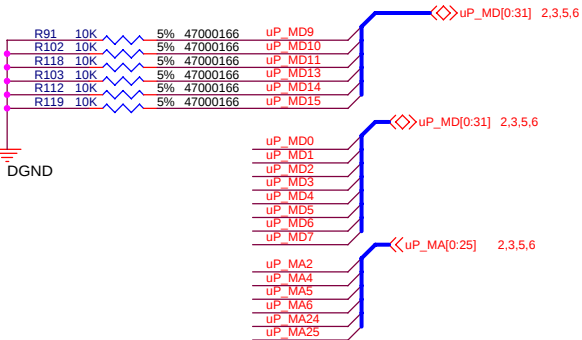


```

pcmcia1_src 0800_00E4 -> 0800_00E7
pcmcia0_src 0800_00E0 -> 0800_00E3
INT_SET CLR 0800_00D0 -> 0800_00D3 (0=clear, 1=set)
INT_MASK EN 0800_00C0 -> 0800_00C3 (0=mask, 1=enable)
MISC_RD 0800_0090 -> 0800_0093
MISC_WR2 0800_0084 -> 0800_0087

```

NOTE: THESE ARE REQUIRED TO MASK OFF MAINSTONE INTERRUPT SOURCES THAT ARE NOT IMPLEMENTED IN THE CPLD WHEN READS ARE DONE TO THE INT_SET_CLR REGISTER.



REVISION 2 -> 3
1) ADDED BUFF DIR DATA TO CPLD
2) CHANGED uP_nMWR TO nIOWR
3) ADDED nCHRDY AND uP_nWAIT TO CPLD
4) ADDED R113

REVISION 3 -> 4
1) ADDED U23, REMOVED R64 AND uP_MODE1

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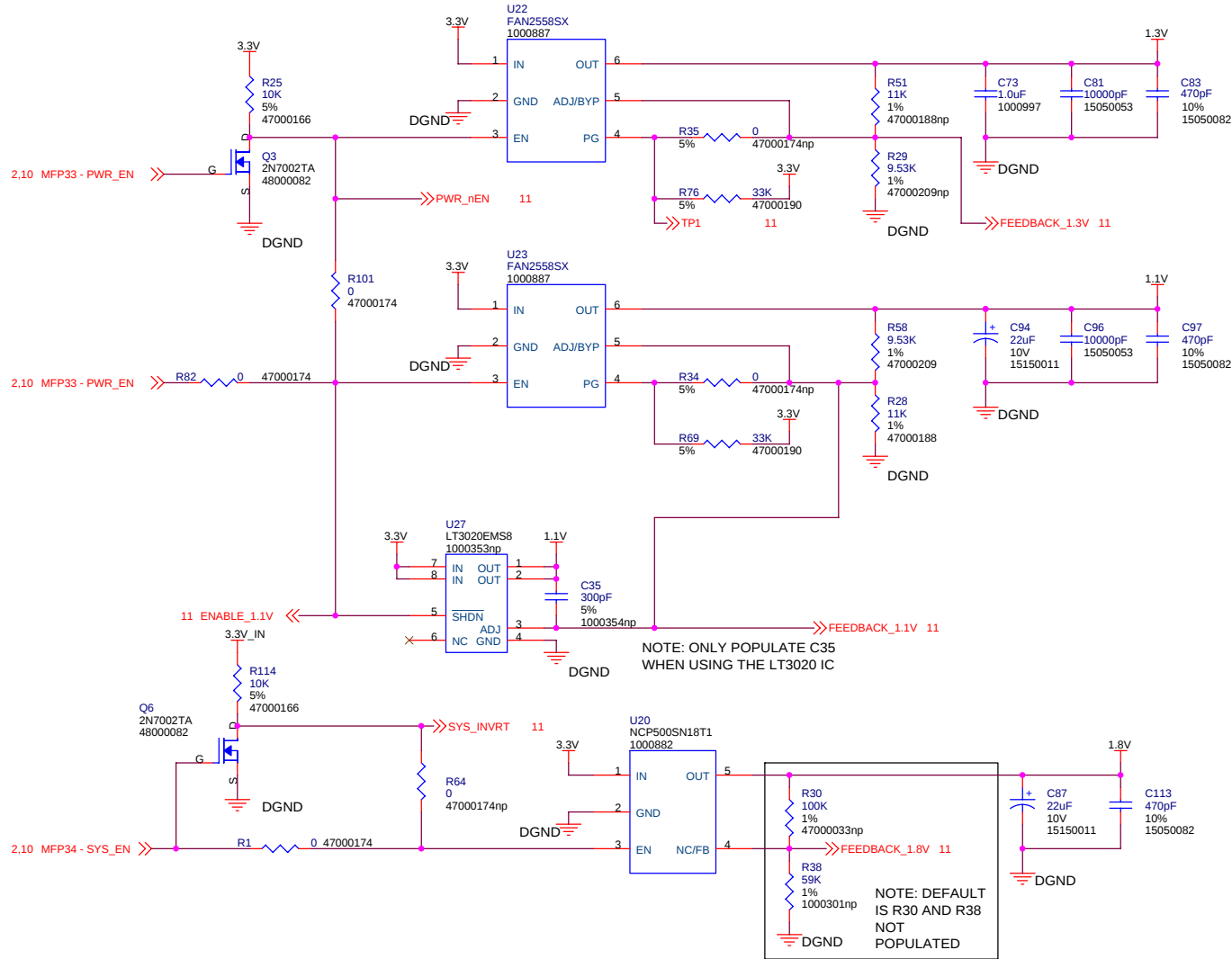
PLL, SRAM, AND CPLD CORE POWER

NOTE: MULTIPLE POWER SUPPLY OPTIONS ARE AVAILABLE FOR PRICE VS. AVAILABILITY VS. POWER REQUIREMENTS

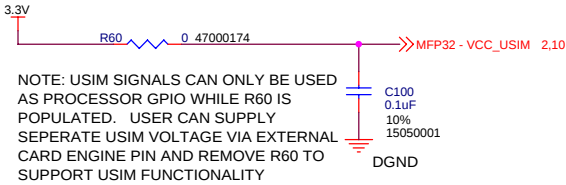
1.3V	MFR PN	LPD NUMBER	PRIORITY	R51	LPD NUMBER	R29	LPD NUMBER	R82	R101	Q3	R35	R76
U22	FAN2558S13X	1000888	STANDARD	NO		NO		YES	YES	NO	NO	YES
U22	FAN2558SX	1000887	2ND	11K	47000188	9.53K	47000209	YES	YES	NO	NO	YES
U22	TPS76901DBVT	1000351	3RD	10K	47000166	150K	1000349	X	X	YES	YES	NO
U22	TPS76201DBVR	1000295	4TH	59K	1000301	62K	1000302	X	X	YES	YES	NO
U22	LT1761ES5-SD	31300501	5TH	10K	47000166	150K	1000349	YES	YES	NO	YES	NO

1.1V	MFR PN	LPD NUMBER	PRIORITY	R58	LPD NUMBER	R28	LPD NUMBER	R82	R101	Q3	R34	R69
U23	FAN2558SX	1000887	STANDARD	9.53K	47000209	11K	47000188	YES	X	NO	NO	YES
U23	TPS76201DBVR	1000295	2ND	40.2K	1000303	62K	1000302	NO	YES	YES	YES	NO
U27	LT3020EMS8	1000353	3RD	59K	1000301	13K	1000355	YES	X	X	NO	NO

1.8V	MFR PN	LPD NUMBER	PRIORITY	R1	x	Q6	R30	R38
U20	NCP500SN18T1	1000882	STANDARD	YES	x	YES	NO	NO
U20	TPS76318DBVT	31300585	2ND	YES	x	YES	NO	NO
U20	TPS76918DBVT	31300404	3RD	NO	x	YES	NO	NO
U20	TPS76201DBVR	1000295	4TH	NO	x	YES	YES	YES

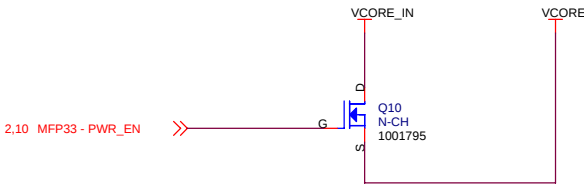
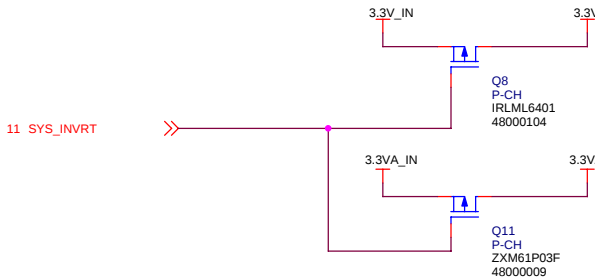
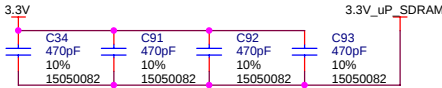


USIM



LAYOUT NOTE:

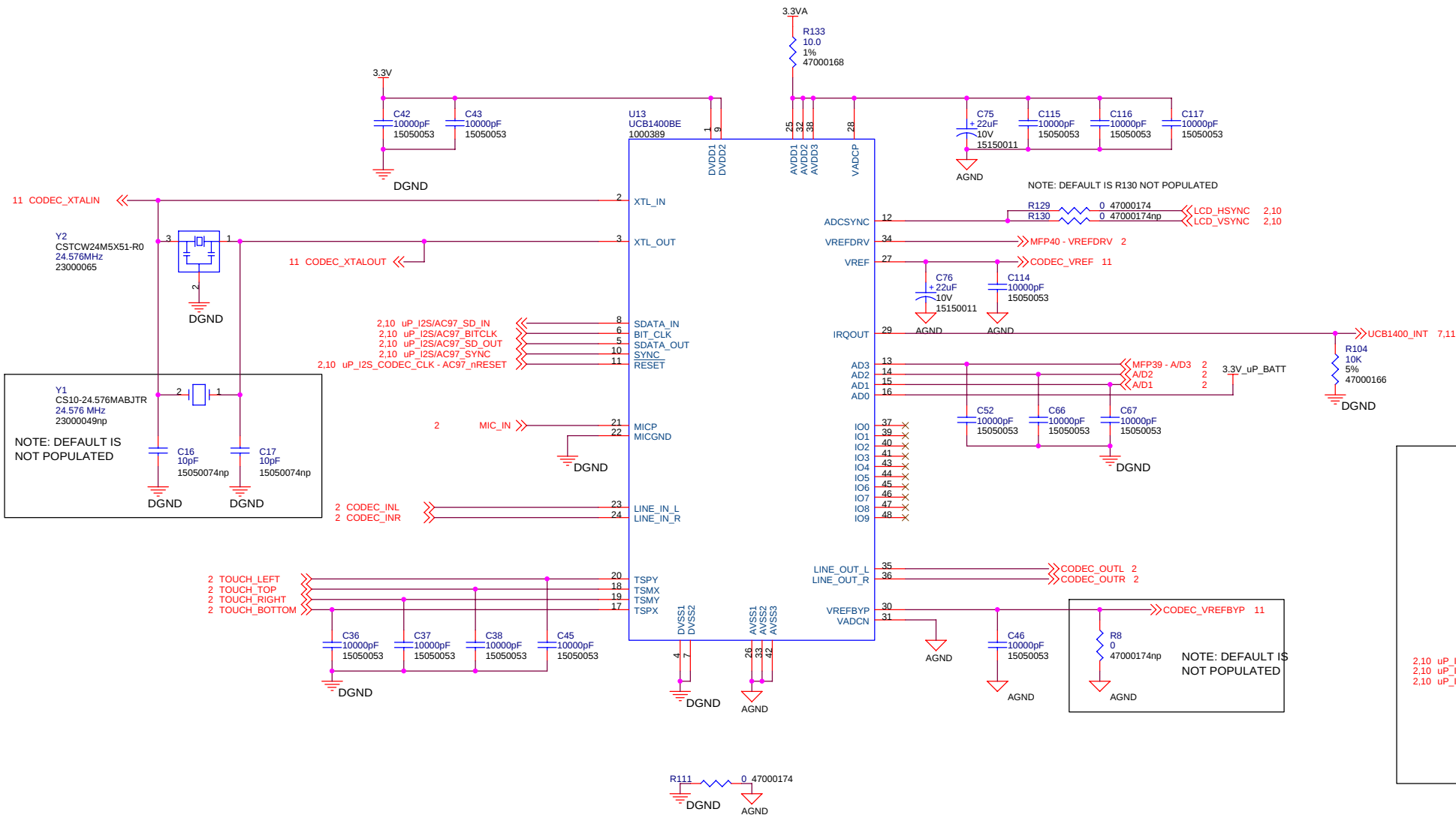
THESE CAPACITORS ARE USED FOR DECOUPLING ACROSS POWER PLANES ON THE CARD ENGINE AND ARE STRATEGICALLY PLACED TO MINIMIZE EMISSIONS.



REVISION 3 -> 4
1) CHANGED C73 TO 1000997

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09 - CODEC



AUDIO CODEC ID REGISTER TABLE

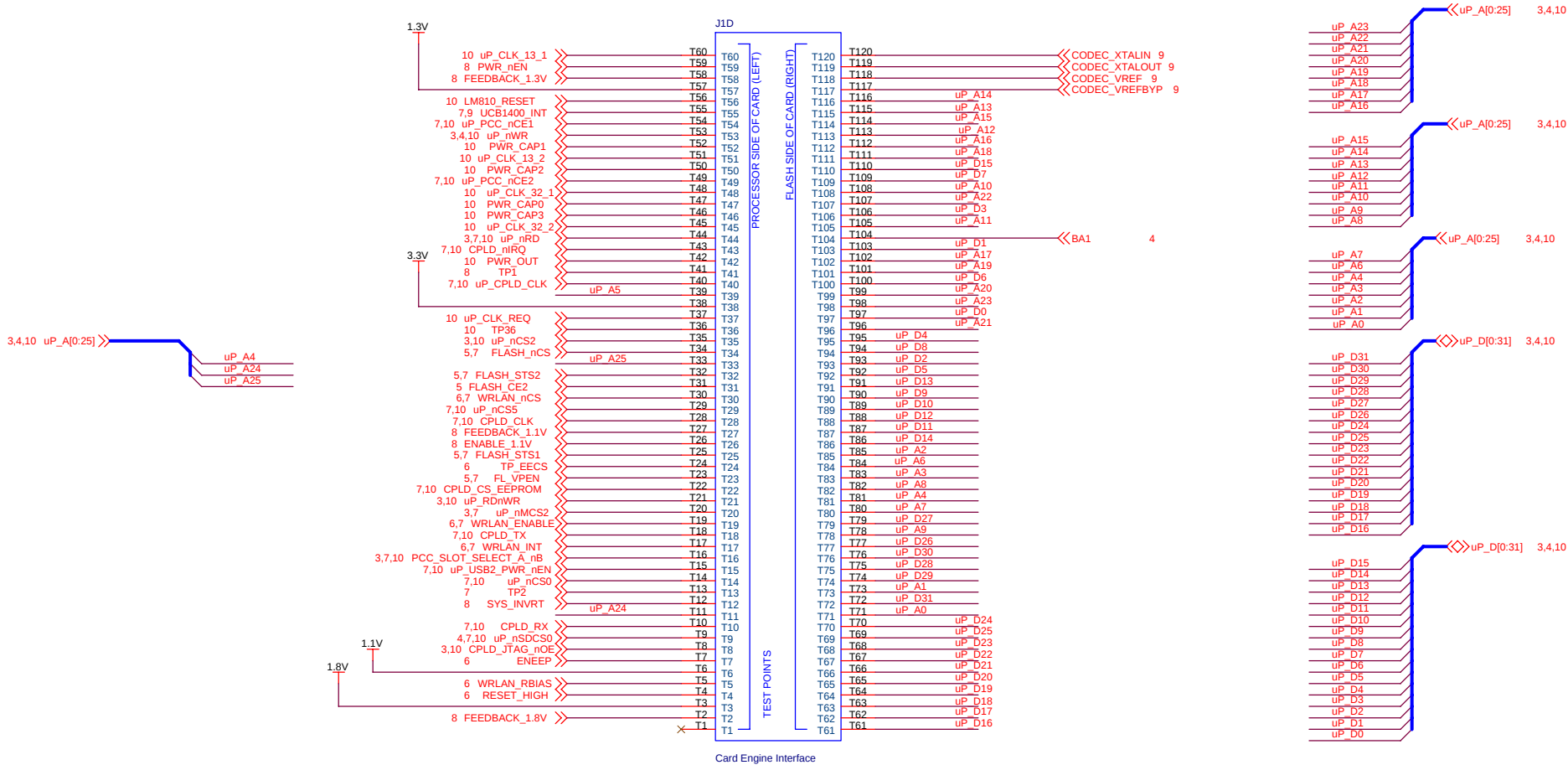
SIGNAL	BIT NAME
uP_I2S_CODEC_CLK - AC97_nRESET	AUDIOID[2]
uP_I2S/AC97_SYNC	AUDIOID[1]
uP_I2S/AC97_SD_OUT	AUDIOID[0]

NOTE: DEFAULT IS R105, R106, R108 NOT POPULATED

2,10 uP_I2S/AC97_SD_OUT
2,10 uP_I2S/AC97_SYNC
2,10 uP_I2S_CODEC_CLK - AC97_nRESET

REVISION 4 -> A
1) CHANGED R129 TO BE STANDARD
AND R130 REMOVED
2) ADDED R133
REVISION 2 -> 3
1) ADDED LCD_VSYNC/HSYNC OPTION TO
ADCSYNC ON UCB1400
2) ADDED R129, R130

11 - TEST POINTS



REVISION 2 -> 3
1) REMOVED uP_nTRST_INTERNAL
2) ADDED uP_RdWr

REVISION 3 -> 4
1) ADDED TP2

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12 - ECO LIST

Revision Control			
ECO Number	Rev	Description of Change	Date
	1	Draft	10/08/2004
	2	Incorporated design review feedback	10/13/2004
C00795	3		03/18/2005
C01124	4	Pilot run	04/06/2005
C01340	A	Production	06/17/2005