PXA270-10 LoCE User's Guide Addendum

BSP Documentation

Logic Product Development
Published: December 2006

Abstract

This document provides information specific to the PXA270-10 Card Engine to supplement the *LoCE Windows Embedded CE BSP User's Guide*.

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	LoCE Kernel Ver	APPROVAL	DATE
A	Michael Aanenson	Initial Release	2.1.8.0	JCA	12/28/06

Table of Contents

1 Synopsis

1.1 Feature Support Summary

Feature	Supported (Y/N)	Details
RAM Image	Y	Default
Flash Image	Y	Environment Variable - **IMGFLASH** set to **1** NOR flash – supported NAND flash – not supported (Use RAM image and YAFFS partition in LogicLoader)
Relocation Image	Y	Environment Variable - **LOCE_RELOCATE_FROM_FLASH** set to 1 NOR flash – supported NAND flash – not supported (Use RAM image and YAFFS partition in LogicLoader)
SDRAM Support	Y	64 MB, 128 MB (auto detect)
RTC	Y	On-chip RTC, boot parameter 'rtc' used
Debug Serial	Y	UARTA (UART1), boot parameter 'debug_serial' used
Debug Ethernet	Y	Onboard SMSC 91C111, boot parameter 'debug_enet'
Power Management:		
- Idle	Y	PXA270 idle mode
- Suspend	Y	PXA270 standby mode
- Standby	N	
- Soft Reset	N	
- Hard Reset	N	
System Timer	Y	Operating system timer 0
Profiling Timer	Y	Operating system timer 5
Installable ISRs	Y	

2 Memory Configuration

2.1 General Memory Map

Image Type	Supported (Y/N)	Description
RAM	Y	The image boot and runs out of RAM
Flash (XIP)	Y	The image boots and runs out of flash
Relocation	Y	The image boots from flash, copies itself to RAM, and runs out of RAM

2.1.1 RAM Image Memory Structure

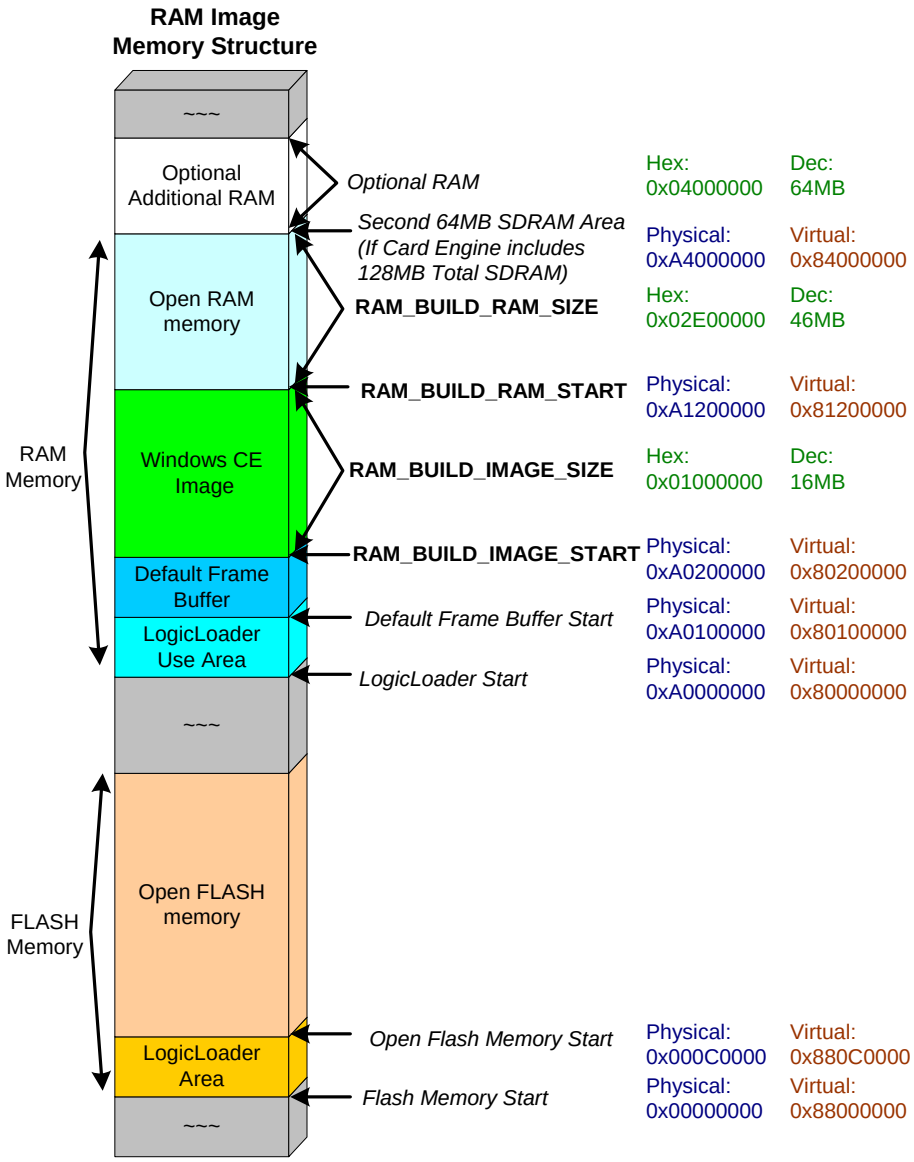

Figure 2.1 – RAM Image Memory Structure

2.1.2 Flash Image Memory Structure

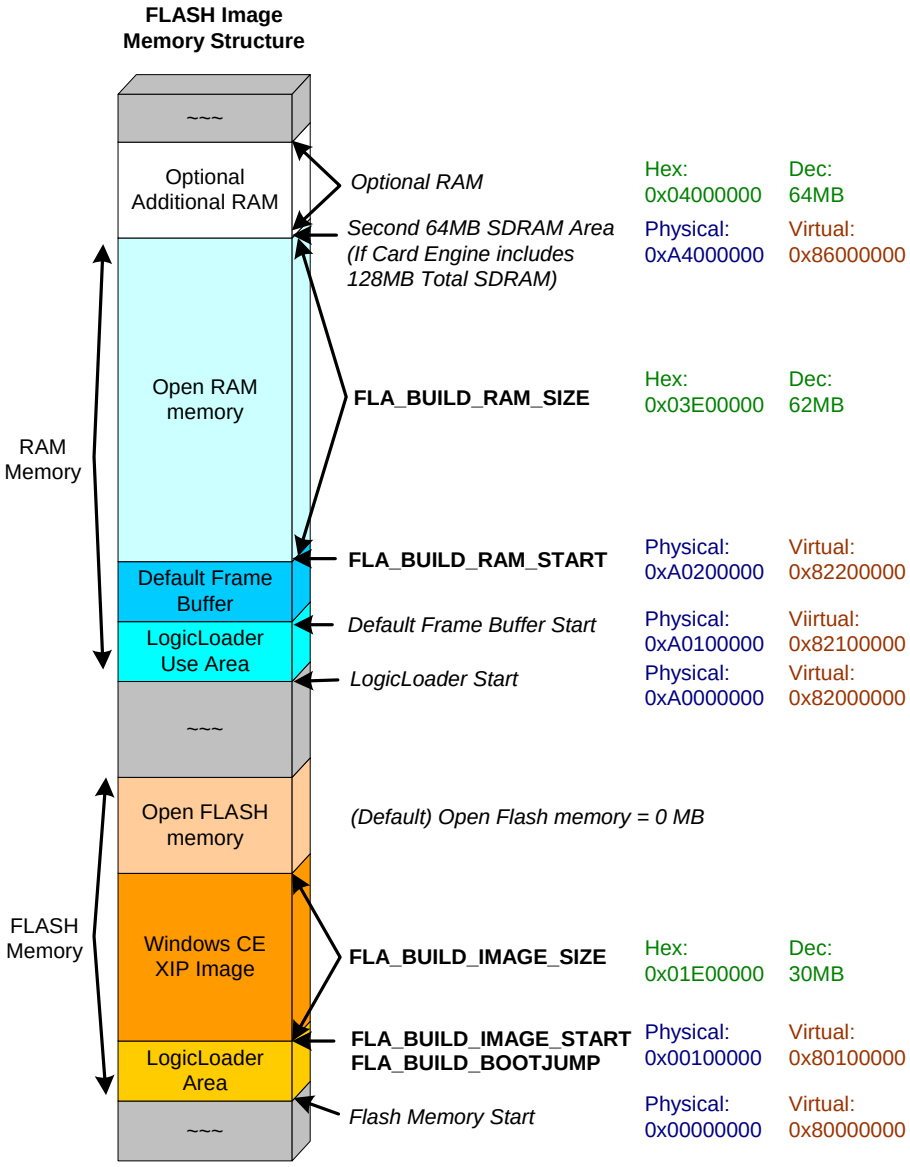

Figure 2.2 – Flash Image Memory Structure

2.1.3 Relocation Image Memory Structure

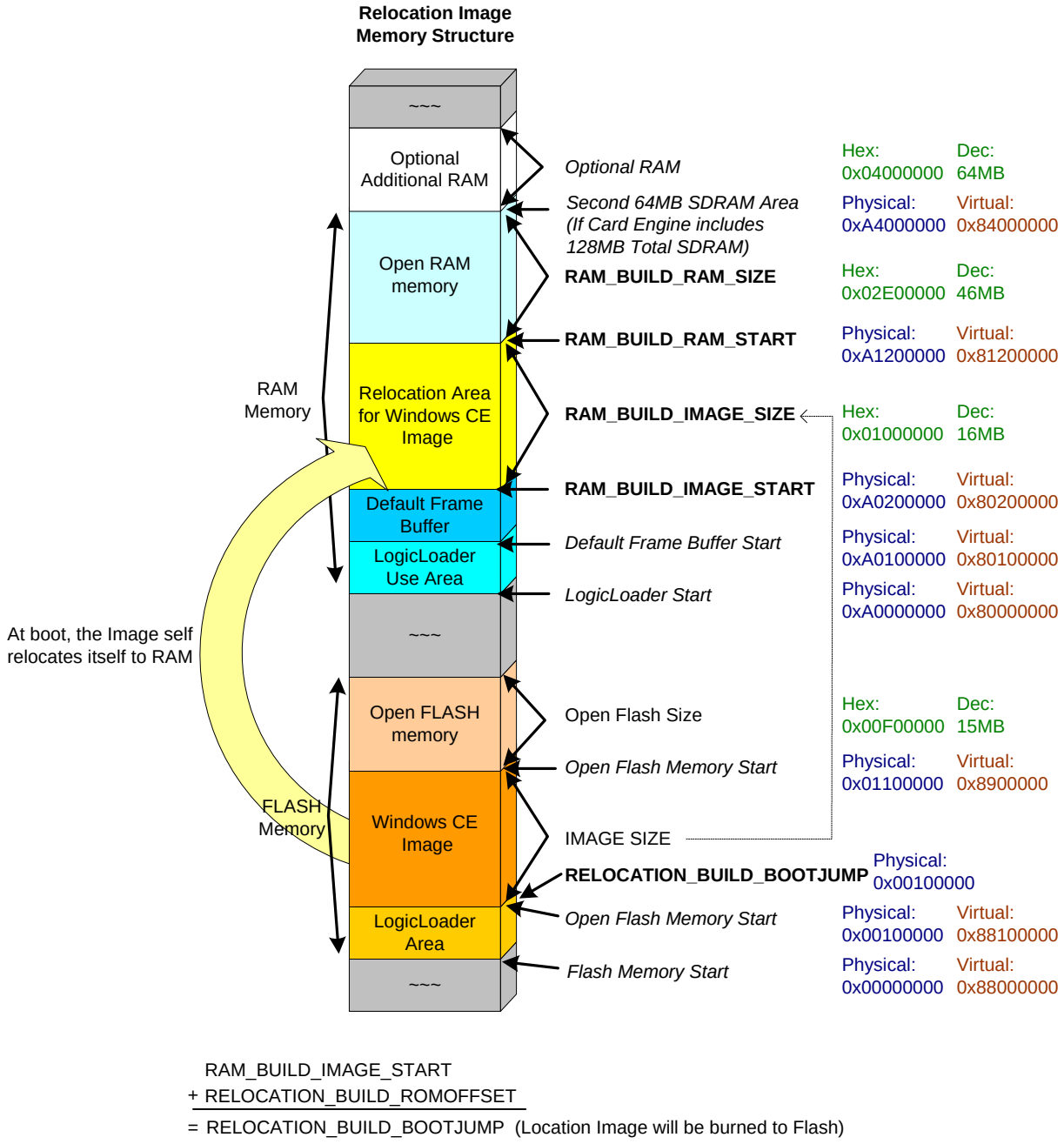

Figure 2.3 – Relocation Image Memory Structure

2.2 SDRAM Configuration

The PXA270 Card Engine supports two SDRAM configurations: 64 MB and 128 MB.

The default settings in the *config.bib* and *pxa270_10_config_bib.h* files are set for 64 MB of SDRAM. If a PXA270 Card Engine has 128 MB of SDRAM onboard, this will be detected in the **OEMInit()** function and added to the total amount of RAM for the system. It is assumed that the SDRAM has been initialized by LogicLoader and the PXA270 Register bit **MDCNFG[MDENX])** has been set to **1**.

When using a PXA270 Card Engine with 64 MB of SDRAM onboard, two SDRAM chips totaling 64 MB can be used externally to the board using the SDRAM Partition 1 area. In this situation, the external 64 MB will be detected automatically.

Please see the *Intel® PXA27x Processor Family Developer's Manual* from Intel for more information regarding the SDRAM interface and set up.

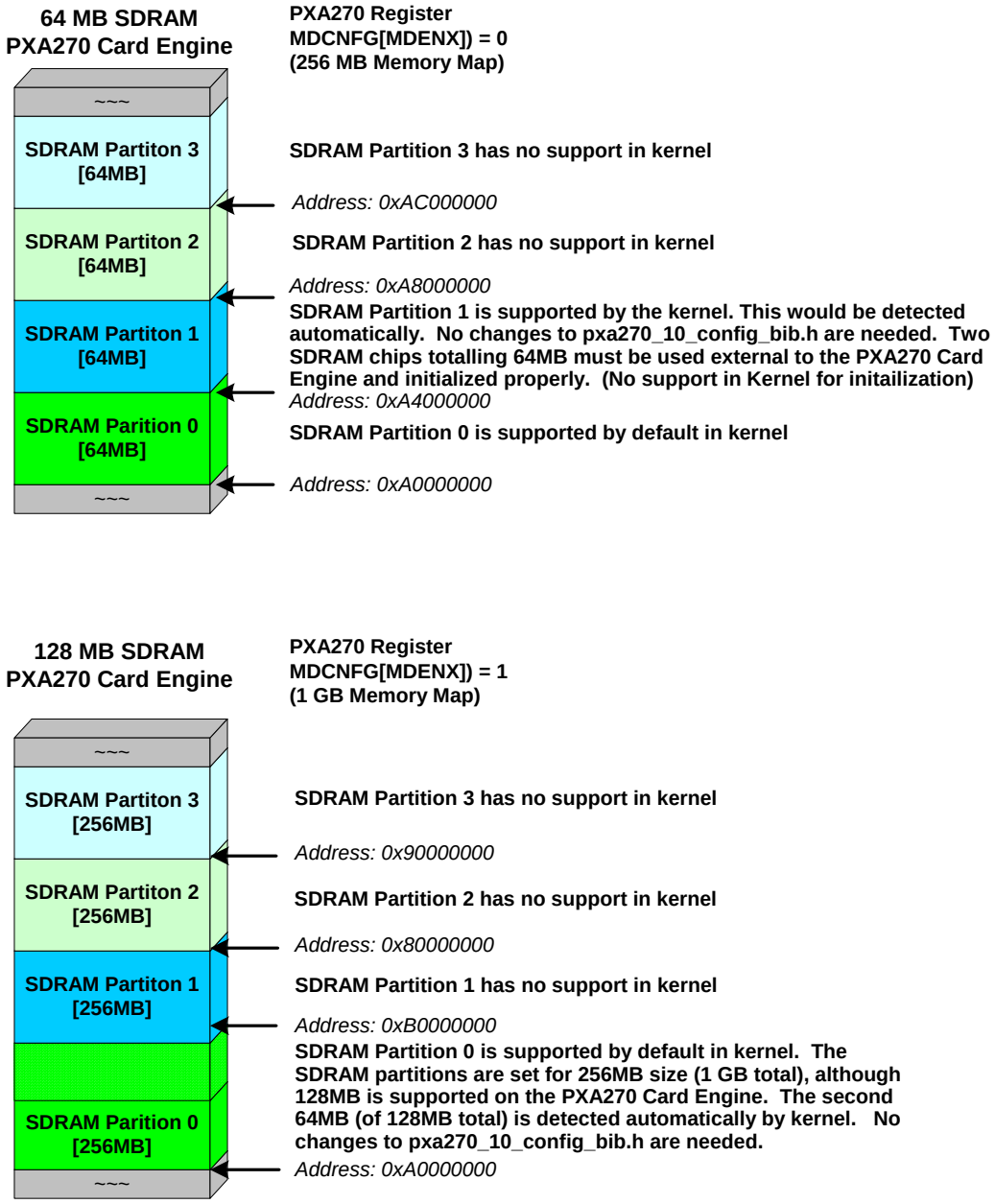

Figure 2.4 – SDRAM Configuration Structures

2.3 OEMAddressTable Entries

Physical	Virtual (RAM Image)	Virtual (Flash Image)	Size	Description
0xA0000000	0x82000000	0x80000000	64	SDRAM Partition 0
0xA4000000	0x86000000	0x84000000	64	SDRAM Partition 1 (or second 64 MB of Partition 0)
0x00000000	0x88000000	0x80000000	32	CS0 - flash CS (boot)
0x5C000000	0x9BD00000	0x9BD00000	1	Internal SRAM memory (256kB)
0x40000000	0x9C000000	0x9C000000	32	Internal peripheral registers
0x44000000	0x9B900000	0x9B900000	1	LCDC registers
0x08000000	0x8E000000	0x8E000000	1	CS2 - fast area, CPLD registers
0x09000000	0x8E100000	0x8E100000	1	CS2 - fast area, WLAN
0x0A000000	0x8E200000	0x8E200000	32	CS2 - fast area, Fast_nCS
0x0B000000	0x8F200000	0x8F200000	16	CS2 - fast area, Flash/Boot_nCS
0x04000000	0x8A000000	0x8A000000	64	CS1
0x0C000000	0x91200000	0x91200000	64	CS3
0x10000000	0x95200000	0x95200000	64	CS4
0x14000000	0x99200000	0x99200000	1	CS5 - slow area, memory CompactFlash
0x15000000	0x99300000	0x99300000	16	CS5 - slow area, ISA
0x17000000	0x9A300000	0x9A300000	16	CS5 - slow area, Slow_nCS
0x20000000	0x9B300000	0x9B300000	1	PC card slot 0 I/O space
0x28000000	0x9B400000	0x9B400000	1	PC card slot 0 attribute memory
0x2C000000	0x9B500000	0x9B500000	1	PC card slot 0 common memory
0x30000000	0x9B600000	0x9B600000	1	PC card slot 1 I/O space
0x38000000	0x9B700000	0x9B700000	1	PC card slot 1 attribute memory
0x3C000000	0x9B800000	0x9B800000	1	PC card slot 1 common memory
0x48000000	0x9BA00000	0x9BA00000	1	Memory controller registers
0x4C000000	0x9BB00000	0x9BB00000	1	USBH registers
0x50000000	0x9BC00000	0x9BC00000	1	Capture interface registers
0x00000000	0x00000000	0x00000000	0	EOT

3 OAL Processor & Peripheral Utilization

3.1 OAL Hardware Initialization

The OAL (OEM Adaptation Layer) makes the assumption that the hardware has been initialized properly by a bootloader, like LogicLoader. No changes from LogicLoader, with the exception of:

- PXA270 PSSR register, **RDH** bit set to **0**. (GPIO pins are configured according to their GPIO configuration.)

3.2 OAL Resource Use

The following peripherals are supported by the OAL. Any peripherals listed below will have software associated that modifies the peripheral's registers during system initialization and may continue to access and modify registers during system runtime. Any peripherals not listed are left in the state that they were when Windows Embedded CE was started

3.2.1 Scheduler Timer / System Time

The OAL uses the PXA270's internal timer 0 to implement the kernel's scheduler and system time.

Optional: *No*

3.2.2 Real Time Clock

The OAL uses the PXA270's internal real-time clock (RTC). The PXA270 Card Engine's 3.3V_uP_BATT pin must be powered to keep the RTC's contents. If the 3.3V_uP_BATT pin is not powered, the RTC will be set to a default time and date. This clock can be updated with the following Windows Embedded CE APIs:

- `GetSystemTime()`
- `SetSystemTime()`

Optional: *Yes → Boot Parameter*

Boot Parameter: *rtc:rtc_pxa270*:

3.2.3 Debug Serial

The OAL uses the PXA270's UART1 port (UARTA on the Card Engine) for debug serial messages.

Optional: *Yes → Boot Parameter*

Boot Parameter: *dbg_serial:FFUART:*

3.2.4 Debug Ethernet (KITL)

The OAL uses the SMSC 91C111 Ethernet connection for debugging. The OAL implements VMINI Ethernet sharing, allowing download, debug, KITL, and product Ethernet over one port.

Optional: *Yes → Boot Parameter*

Boot Parameter:
dbg_enet:91C111:dbg_enet_base:0x09000000:dbg_enet_irq:0x00000008:kitl:true:

dbg_enet:91C111:dbg_enet_base:0x09000000:dbg_enet_irq:0x00000008:kitl:true:share_eth:1:

3.2.5 Kernel Profiler

The OAL uses the PXA270's internal OS timer 5 for the Kernel Profiler.

Optional: *Yes → Enable/Disable Kernel profiling*

3.2.6 Interrupt Handler

The OAL's **OEMInterruptHandler()** implementation is shown in the following diagram:

Optional: *No*

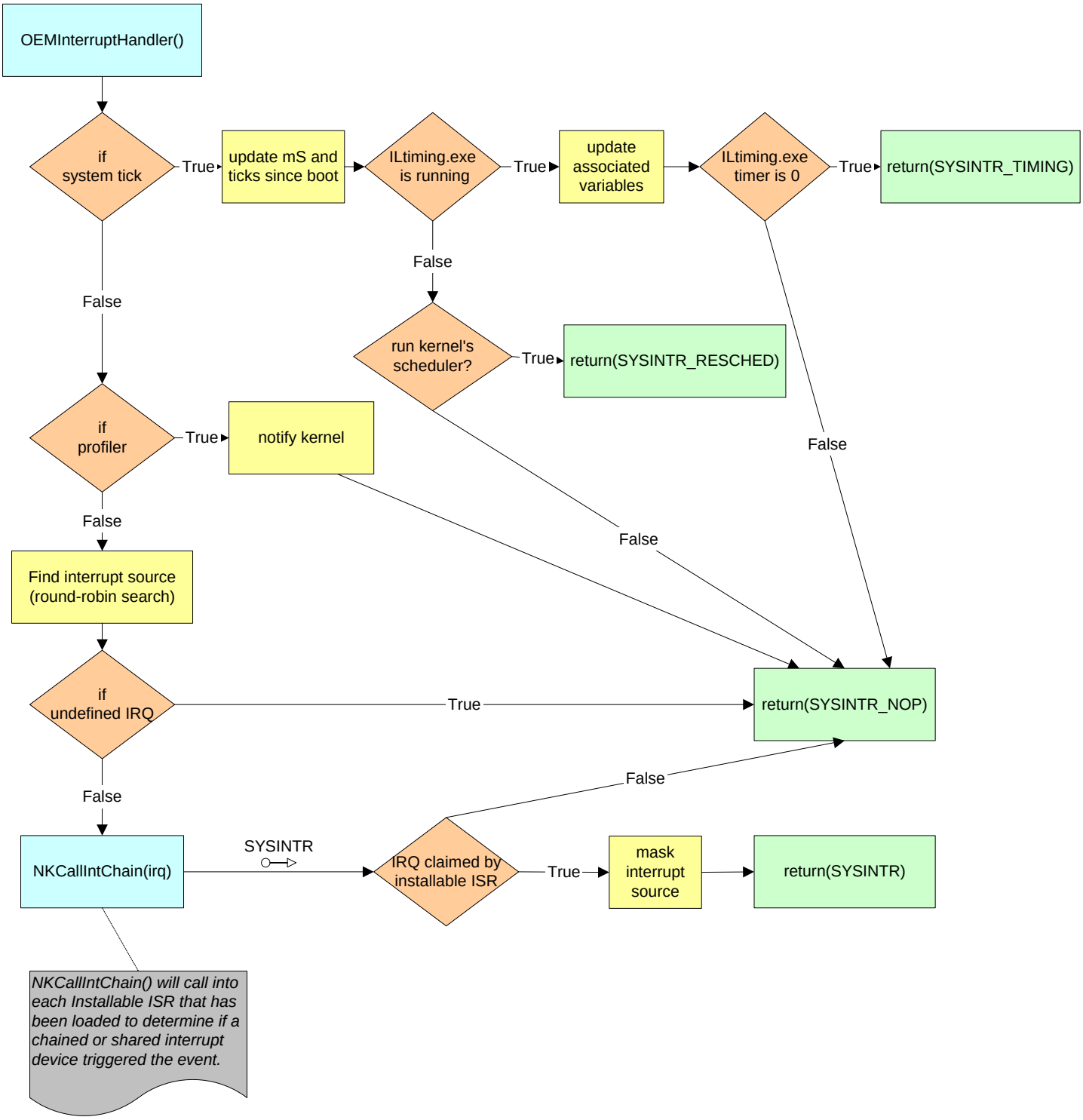

Figure 3.1 – OEMInterruptHandler() Implementation Diagram

3.3 Interrupts

The following table lists the PXA270 hardware interrupt with a number that can be used with **IOCTL_HAL_REQUEST_SYSINTR**.

IRQ	Description	IRQ	Description	IRQ	Description
0	SSP 3	16	SSP 2	32	reserved
1	MSL	17	LCD	33	Quick Capture Interface
2	USB Host 2	18	I2C	34	reserved
3	USB Host 1	19	Infrared Port	35	reserved
4	Keypad Controller	20	STUART	36	reserved
5	Memory Stick	21	BTUART	37	reserved
6	Power I2C	22	FFUART	38	reserved
7	OS System Timers 4-11	23	MMC	39	reserved
8	GPIO 0	24	SSP 1		
9	GPIO 1	25	DMAC		
10	GPIO 2-120	26	OS System Timer 0		
11	USB Client (Function)	27	OS System Timer 1		
12	PMU	28	OS System Timer 2		
13	I2S	29	OS System Timer 3		
14	AC97	30	RTC Hz Clock		
15	USIM	31	RTC Alarm		

4 Boot Parameters

The following boot parameters are supported by the OAL.

Parameter	Settings	PXA270 Example	Summary
share_eth	1 / 0 / [not set]	*share_eth:1:*	Enable bridged VMINI with KITL
kitl	true / false / [not set]	*kitl:true:*	Enable KITL Ethernet debugger
ip_addr	xxx.yyy.xxx.yyy / [not set]	*ip_addr:192.168.0.154:*	Manual IP address for Ethernet debugger
clean_syshive	1 / [not set]	*clean_syshive:1:*	Force clean system hive on boot
clean_usrhive	1 / [not set]	*clean_usrhive:1:*	Force clean user hive on boot
dbg_serial	PXA270_FFUART / null / [not set]	*dbg_serial:PXA270_FFUART:*	Debug serial port enable
dbg_enet	91C111 / null / [not set]	*dbg_enet:91C111:*	Debug Ethernet controller enable
dbg_enet_base	0x09000000 / [not set]	*dbg_enet_base:0x09000000:*	Debug Ethernet controller physical address
dbg_enet_irq	0x00000008 / [not set]	*dbg_enet_irq:0x00000008:*	Debug Ethernet controller interrupt
rtc	rtc_pxa270 / rtc_null / [not set]	*rtc:rtc_pxa270:*	RTC interface enable
quantum	0xXXXXYYYY / [not set]	*quantum:0x60*	Sets **dwDefaultThreadQuantum** in Kernel

Example boot scripts:

RAM Image:
exec rtc:rtc_pxa270:

Flash or Relocation Image:
exec 0x00100000 - rtc:rtc_pxa270

RAM Image with debug serial and debug Ethernet enabled:
exec
rtc:rtc_pxa270:dbg_serial:PXA270_FFUART:dbg_enet:91C111:dbg_enet_base:0x09000000:dbg_enet_irq:0x00000008:share_eth:1:kitl:true:

RAM Image with display mode specified:
exec rtc:rtc_pxa270:disp_num:8

5 Kernel IOCTLs

The following Kernel IOCTLs are either not supported or differ from the documented implementation as detailed.

5.1 IOCTL_HAL_REBOOT

- Hard Reset: not supported
- Soft Reset: not supported

6 Disclaimer

Logic strives to provide the most up-to-date information. However, the list of supported features in this document is partial and subject to change.

If you need software support on demand, please contact Logic Product Development sales at: product.sales@logicpd.com.

