

PROJECT:	LCE-APP-10
PART NUMBER:	80000116
ASSEMBLY NAME:	Zoom SDK Application Kit
SCHEMATICS:	ECR

TABLE OF CONTENTS	
PAGE	DESCRIPTION
1	TITLE PAGE
2	EXPANSION BUS
3	ENGINE ETHERNET
4	AUDIO
5	CF
6	RS232
7	VIDEO
8	POWER
9	SH AND ARM JTAGS
10	EXPANSION HEADERS
11	USB HOST/FUNCTION
12	ECO LIST

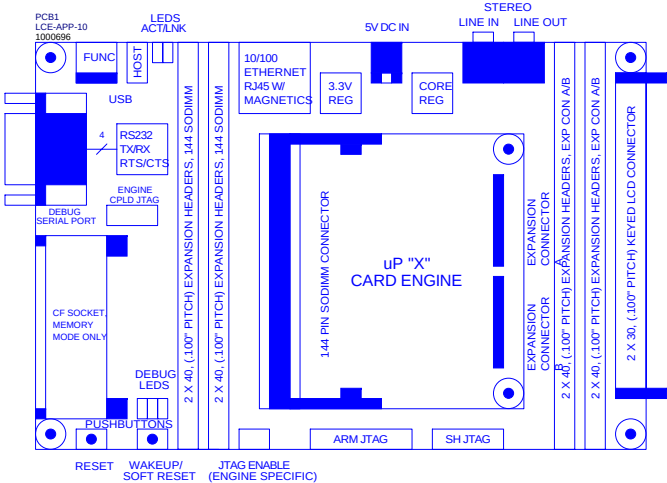
COLOR LEGEND

NOTE:
NOTES IN GREEN TEXT ARE GENERAL
DESIGN OR SCHEMATIC NOTES

LAYOUT NOTE:
NOTES IN RED TEXT ARE PCB LAYOUT
RECOMMENDATIONS OR GUIDLINES

NET NAMES
NET NAMES IN GREEN TEXT ARE
NETS THAT ARE NOT DIRECTLY
CONNECTED WITH A VISIBLE WIRE ON
SINGLE SCHEMATIC PAGE, BUT USE
THIS CONVENTION TO MAKE THE
SCHEMATIC EASIER TO READ

NET NOTE
NET NOTES IN BLACK TEXT INDICATE
A PARTICULAR FUNCTIONALITY OF A
SPECIFIC NET, IT IS NOT A NET NAME
MERELY TEXT AND HAS NO AFFECT
ON THE DRC.



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REVISIONS A->F:
1. SUBMITTED PART FOR LCE-APP-10 AND UPDATED BLOCK DIAGRAM AND TITLE PAGE

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TitleZoom SDK Application Board

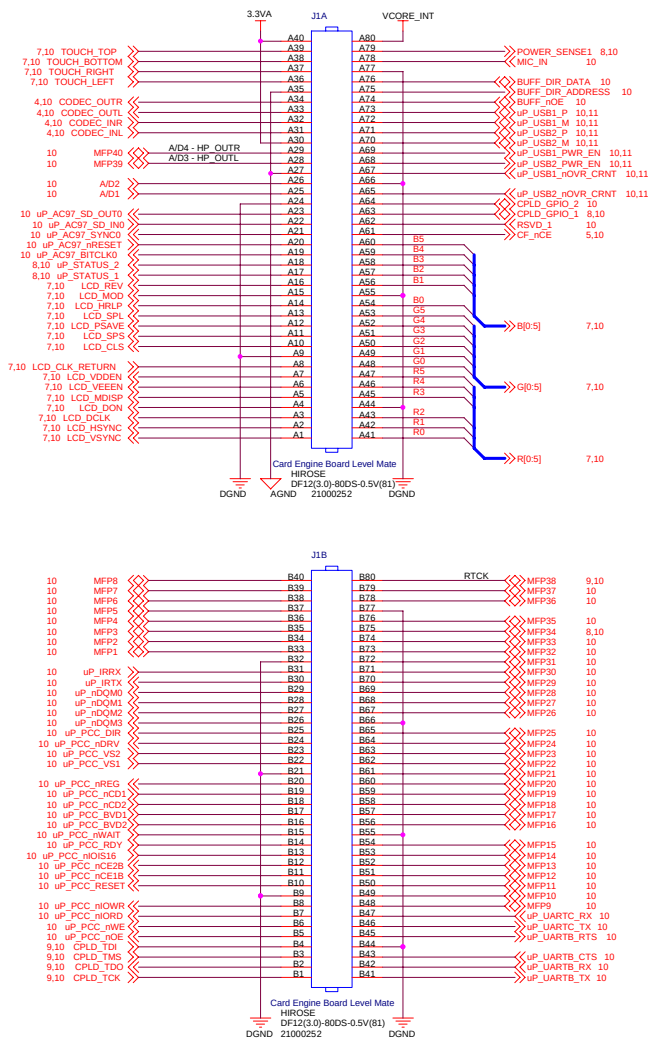
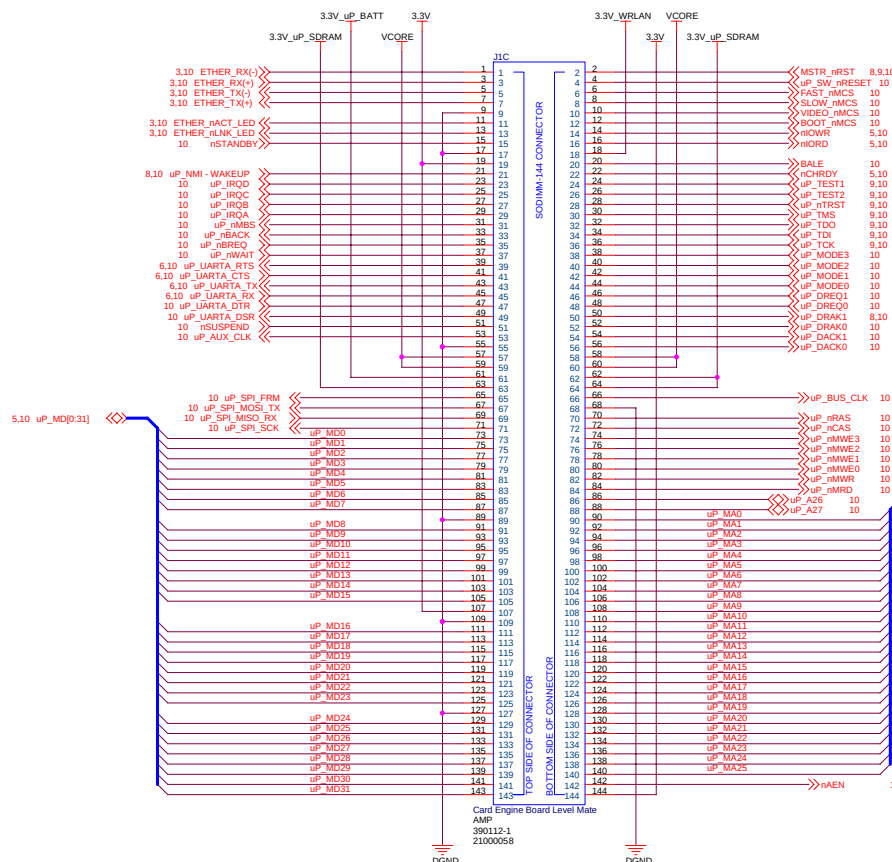
SizeCNumber80000116RevL

Design Create Date = Monday, July 01, 2002ProjectLCE-APP-10Sheet1Of12

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02 - EXPANSION BUS

NOTE:
NOT ALL CARD ENGINES WILL
HAVE ALL THESE SIGNALS,
PLEASE SEE SPECIFIC CARD
ENGINE HARDWARE SPEC FOR
DETAILED PINOUT AND SIGNAL
INFORMATION.



NOTE:
REFER TO THE PROCESSOR
CARD ENGINE PINOUT PAGES (7,
10) FOR LCD DATA SIGNALS.
THE DATA SIGNALS ARE SETUP
FOR AN 18 BIT TFT INTERFACE.
FOR SUPPORT OF OTHER
DISPLAY TYPES, REFER TO THE
LCD PINOUT TABLE IN THE CARD
ENGINE HARDWARE
SPECIFICATION MANUAL.

REVISIONS C->D:

- ```

1. CHANGED NETS
A39 - TOUCH_TOP (was TOUCHX2)
A38 - TOUCH_BOTTOM (was TOUCHX)
A37 - TOUCH_RIGHT (was TOUCHY2)
A36 - TOUCH_LEFT (was TOUCHY)

2. REMOVED THE NET CF_RDYnBSY AND RENAMED
THE NET RSVD 1

```

REVISIONS D-&gt;E:

1. CHANGED NET NAME OF uP\_NMI (J1C.21) TO uP\_NMI - WAKEUP TO ACCOMMODATE THE a400 AND A404

REVISIONS I-&gt;J:

1. Changed pin 61 of SODIMM from 3.3V to 3.3V\_uP\_BATT.

REVISIONS B-&gt;C

1. SEPARATED THE 3.3V AND 3.3V\_U<sub>P</sub>\_SDRAM ON PINS 61-64 OF THE SODIMM CON.
2. ADDED 3.3V\_VRLN TO THE DIMM CONNECTOR J1C.19
3. CHANGED NET NAMES TO FOLLOW NEW NAMING CONVENTION SHOWING ACTIVE LEVEL I.E. MSTR\_RST -> MSTR\_!RST.
4. ADDED SIGNAL\_U<sub>P</sub>\_RTCK TO MFG38 FROM THE 20PIN JTAG HEADER
5. SWITCHED THE PINS ON J1C THAT NETS LCD\_PSAVE AND LCE\_REV GO TO
6. RENAMED NET LCD\_CLKIN -> LCD\_CLK\_RETURN AND NET LCD\_CLKOUT -> LCD\_DCLK
7. REMOVED R22

REVISIONS A-&gt;E

1. CHANGED DIRECTION OF NETS LCD\_CLKIN AND LCD\_CLKOUT
2. CHANGED THE NAMES OF THE LCD DATA LINES
3. CHANGED THE NET NAMES OF EVB1 AND EVB2 TO CF\_nCE AND CF\_BSYnRDY RESPECTIVELY

REVISIONS J-&gt;L

1. Changed Net uP\_UARTB\_DSR to uP\_UARTB\_RTS

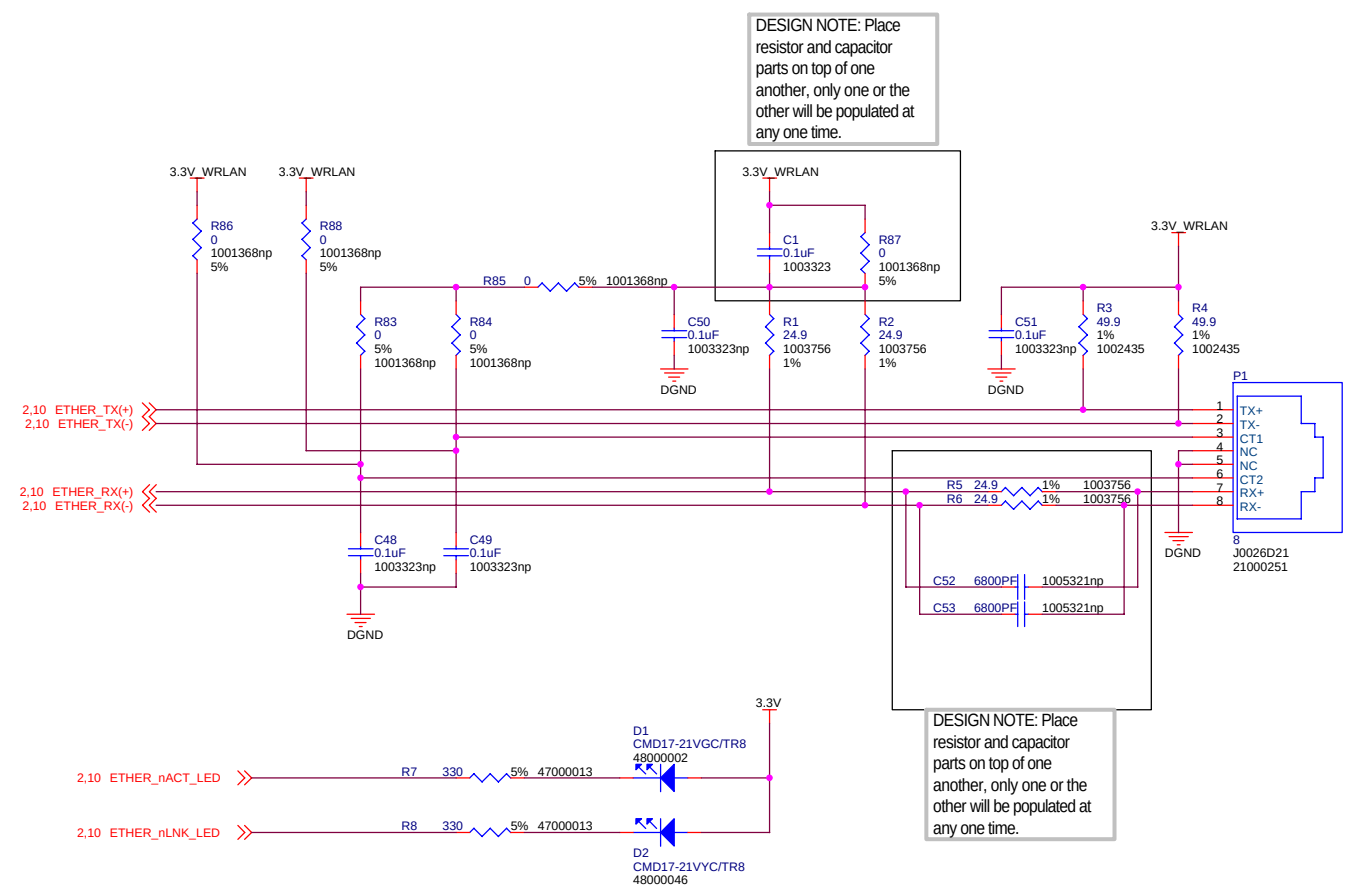
Schematic Modify Date = Friday, October 12, 2001


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|-------|----------------------------|
| Title | Zoom SDK Application Board |
|-------|----------------------------|

|                                            |                    |               |
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ETHERNET CONFIGURATION

|                  |          |          |        |        |        |        |        |        |        |        |
|------------------|----------|----------|--------|--------|--------|--------|--------|--------|--------|--------|
|                  | R1       | R2       | R3     | R4     | R5     | R6     | R83    | R84    | R85    | R86    |
| AC101L / DP83848 | 49.9 ohm | 49.9 ohm | pop    | pop    | 0 ohm  | 0 ohm  | pop    | pop    | no pop | pop    |
| LAN91C111        | pop      | pop      | pop    | pop    | pop    | pop    | no pop | no pop | no pop | no pop |
| LAN9117          | 49.9 ohm | 49.9 ohm | pop    | pop    | no pop | no pop | pop    | no pop | pop    | no pop |
|                  |          |          |        |        |        |        |        |        |        |        |
|                  | R87      | R88      | C1     | C48    | C49    | C50    | C51    | C52    | C53    |        |
| AC101L / DP83848 | pop      | no pop   | no pop | pop    | pop    | pop    | pop    | no pop | no pop |        |
| LAN91C111        | no pop   | pop      | pop    | no pop | no pop | no pop | no pop | no pop | no pop |        |
| LAN9117          | no pop   | pop      | no pop | pop    | pop    | no pop | no pop | pop    | pop    |        |

REVISIONS J->K:  
1. ADDED R83-R88 AND C48-C53

- REVISIONS F->G:
1. ADDED BOX AROUND THE NO POP RESISTOR ON ENET CONNECTOR
- REVISIONS C->F:
1. CONNECTED CT1 TO 3.3V\_WRLAN PER 91C111 SCHEMATIC CHECKLIST PROVIDED BY SMSC
  2. CHANGED THE CONNECTION OF CT1 TO 3.3V\_WRLAN DIRECTLY TO ONE THAT USES A 0OHM (R80) UNTIL QA HAS BEEN COMPLETED.
- REVISIONS B->C:
1. CHANGED THE IMPEDENCE MATCHAGE VOLTAGE ON THE ENET TX AND RX LINES TO 3.3V\_WRLAN
  2. CHANGED THE NET NAMES OF THE LNK AND ACT LED NETS TO ETHER\_nACT\_LED AND ETHER\_nLNK\_LED
  3. CHANGED THE NET NAMES OF THE LNK AND ACT LED NETS TO ETHER\_nACT\_LED AND ETHER\_nLNK\_LED
  4. CHANGED R3 AND R4 FROM 47 OHM 5%S TO 49.9 OHM 1%S
  5. GROUNDED PINS 4 AND 5 OF P1, PER PULSE CONNECTOR SPEC
  6. CHANGED R1,R2,R5,R6 FROM 24 OHM 5%S TO 24.9 OHM 1%S

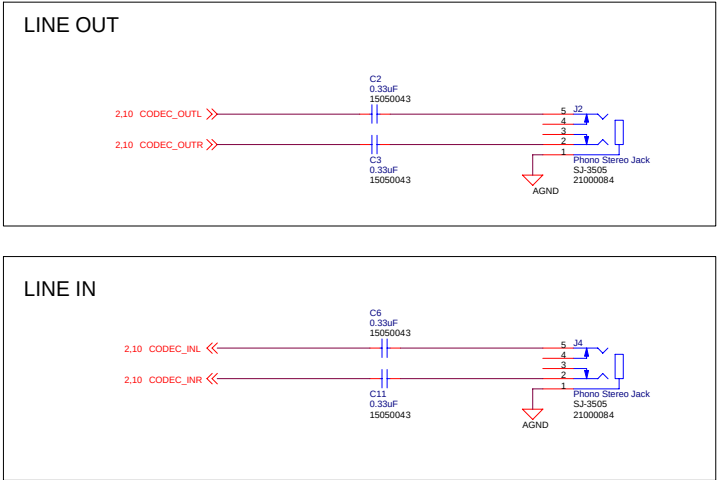
Schematic Modify Date = Friday, October 12, 2007



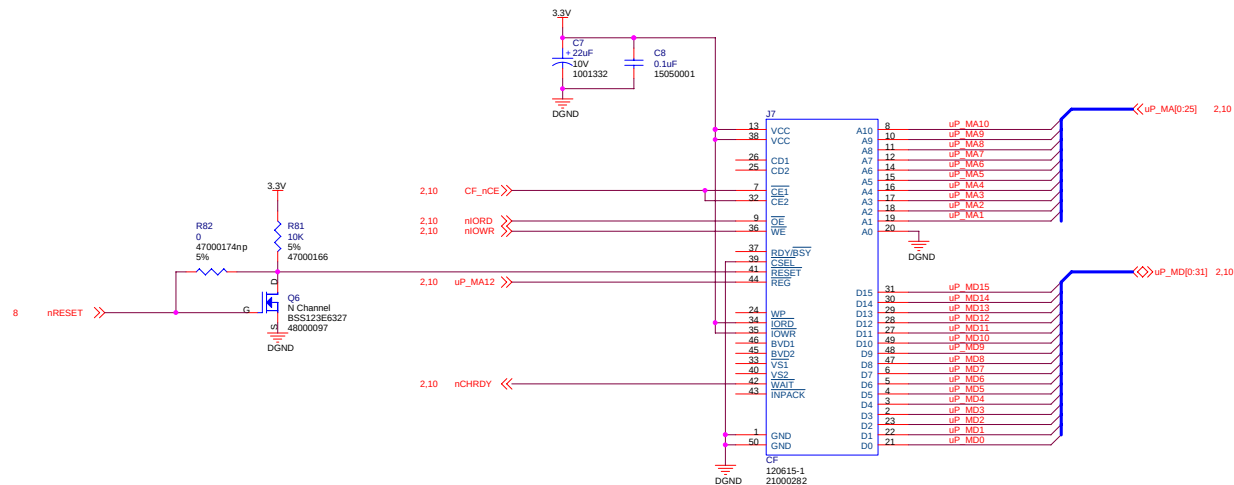
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| Size B                                     | Number 80000116 | Rev L         |
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# COMPACT FLASH SOCKET MEMORY MODE ONLY



## REVISIONS I->J:

CHANGED CF RESET FROM MSTR\_nRST TO nRESET

## REVISIONS H->I:

CHANGED C7 TO 1000014 (WAS 15150011)

## REVISIONS G->H:

1. INVERTED RESET SIGNAL TO CF CARD THIS SIGNAL IS ACTIVE HIGH  
REVISIONS F->G:

1. REMOVED A0 FROM CF CONNECTOR FOR COMPATABILITY WITH  
A400 BSC IN A 16BIT AREA

## REVISIONS C->D:

1. CHANGED NET THAT CONNECTS TO REG ON J7.44 FROM uP\_MA13  
TO uP\_MA12

2. REMOVED THE NET CF\_RDYnBSY

## REVISIONS B->C:

1. CHANGED NET THAT CONNECTS TO REG ON J7.44 FROM uP\_MA11  
TO uP\_MA13

2. REMOVED PULLUP ON CF\_RDYnBSY

## REVISIONS A->B:

1. ADDED NET uP\_MA3 TO J7.17 FOR 16BIT ADDRESSABILITY  
2. CHANGED NETS MFP3 AND MFP6 TO EVB1 AND EVB2

3. REMOVED NET uP\_MA0 AND TIED THAT PIN ON J7 TO GND

4. REMOVED HOT SWAPPABILITY, DELETED NETS  
uP\_PCCDRY AND CF\_3.3V, AND COMPONENTS Q1, C10

5. ADDED ADDRESS LINES uP\_MA0,4-9 AND uP\_MA11 FOR  
GREATER FUNCTIONALITY AND USABILITY OF MORE CF CARDS

6. CHANGED THE NET NAMES OF EVB1 AND EVB2 TO  
CF\_nCE AND CF\_BSYnRDY RESPECTIVELY

## REVISIONS J->K:

1. CHANGED C7 FROM 150uF TO 22uF

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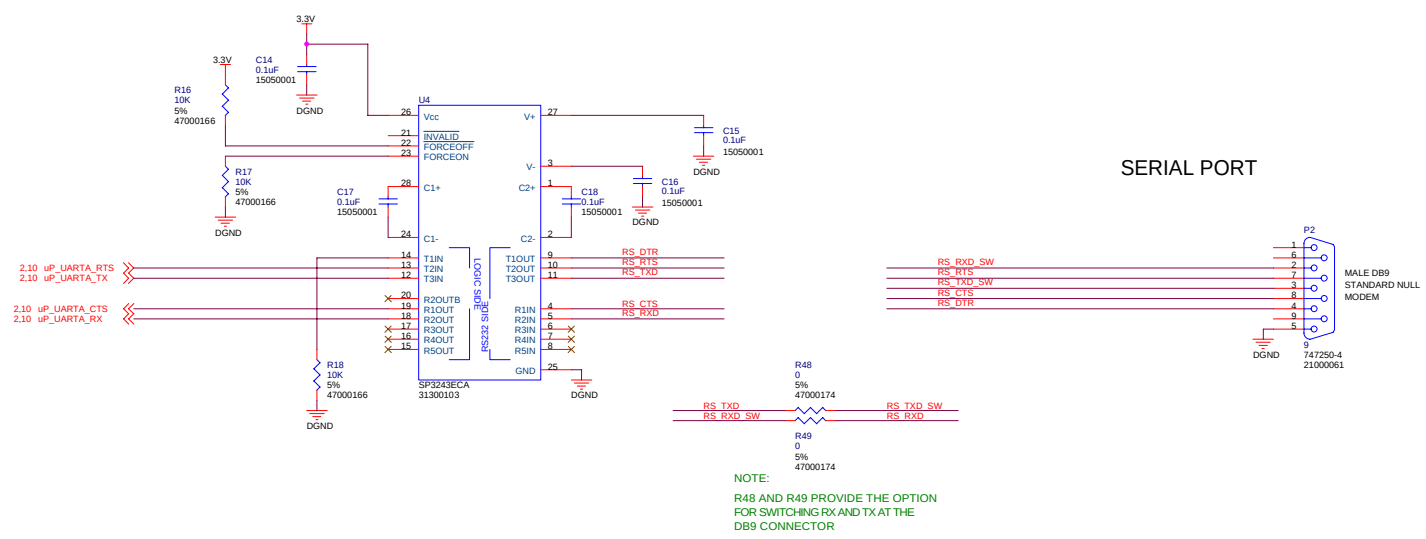


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| Design Create Date = Monday, July 01, 2002 |                 | Sheet 5 Of 12      |       |

06 - RS232 AND DB9 CONNECTOR



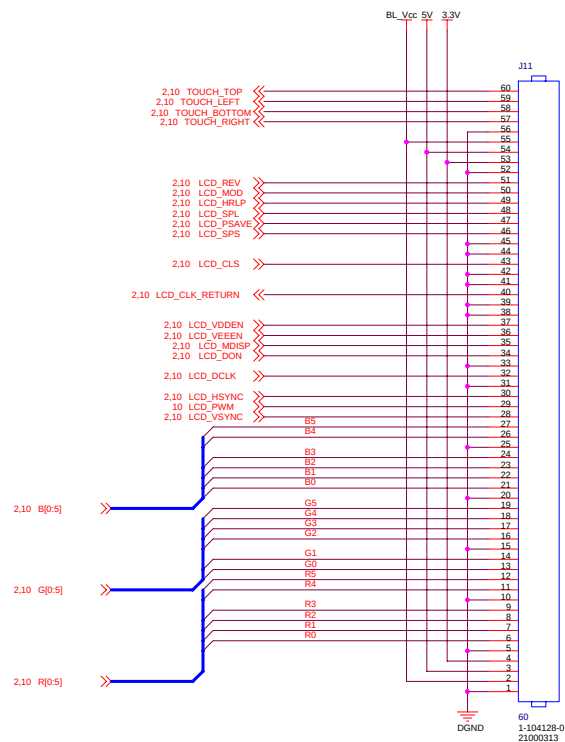
REVISIONS B->C:  
1. CHANGED REF DES FOR Q2np and R19np TO Q2 AND R19

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## NOTE:

THE NET BL\_Vcc IS CONNECTED  
TO A 2PIN HEADER J40 ON PAGE  
8.



## NOTE:

REFER TO THE PROCESSOR CARD ENGINE PINOUT  
PAGES (7, 10) FOR LCD DATA SIGNALS. THE DATA  
SIGNALS ARE SETUP FOR AN 18 BIT TFT  
INTERFACE. FOR SUPPORT OF OTHER DISPLAY  
TYPES, REFER TO THE LCD PINOUT TABLE IN THE  
CARD ENGINE HARDWARE SPECIFICATION  
MANUAL.

## NOTE:

THIS CONNECTOR IS ACTUALLY A 30X2 DUAL ROW .100" PITCH .025" SQ POST MALE  
HEADER. IT IS REPRESENTED SYMBOLICALLY AS A SINGLE ROW CONNECTOR TO  
ILLUSTRATE HOW THE SIGNALS WILL ROUTE THROUGH THE RIBBON CABLE.

## REVISIONS C-&gt;D:

1. CHANGED NETS  
A39 - TOUCH\_TOP (was TOUCHX2)  
A38 - TOUCH\_BOTTOM (was TOUCHX)  
A37 - TOUCH\_RIGHT (was TOUCHY2)  
A36 - TOUCH\_LEFT (was TOUCHY)

## REVISIONS B-&gt;C:

1. CHANGED THE 60PIN LCD CONNECTOR J11 TO A SHROUDEDKEYEDW  
EJECTOR TABS TYPE
2. SWITCHED THE PINS ON J11 THAT NETS LCD\_PSAVE  
AND LCE\_REV GO TO
3. RENAMED NET LCD\_CLKIN -> LCD\_CLK\_RETURN  
AND NET LCD\_CLKOUT -> LCD\_DCLK

## REVISIONS A-&gt;B:

1. CHANGED DIRECTION OF NETS LCD\_CLKIN AND  
LCD\_CLKOUT
2. CHANGED THE NAMES OF THE LCD DATA LINES

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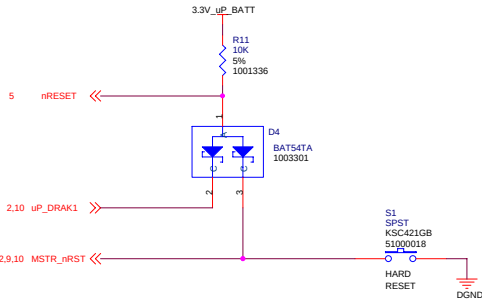


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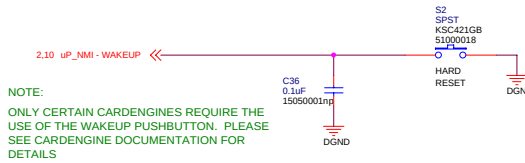
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| Design Create Date = Monday, July 01, 2002 |                 | Project LCE-APP-10 | Sheet 7 Of 12 |

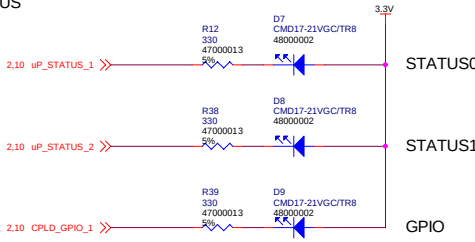
MASTER  
RESET



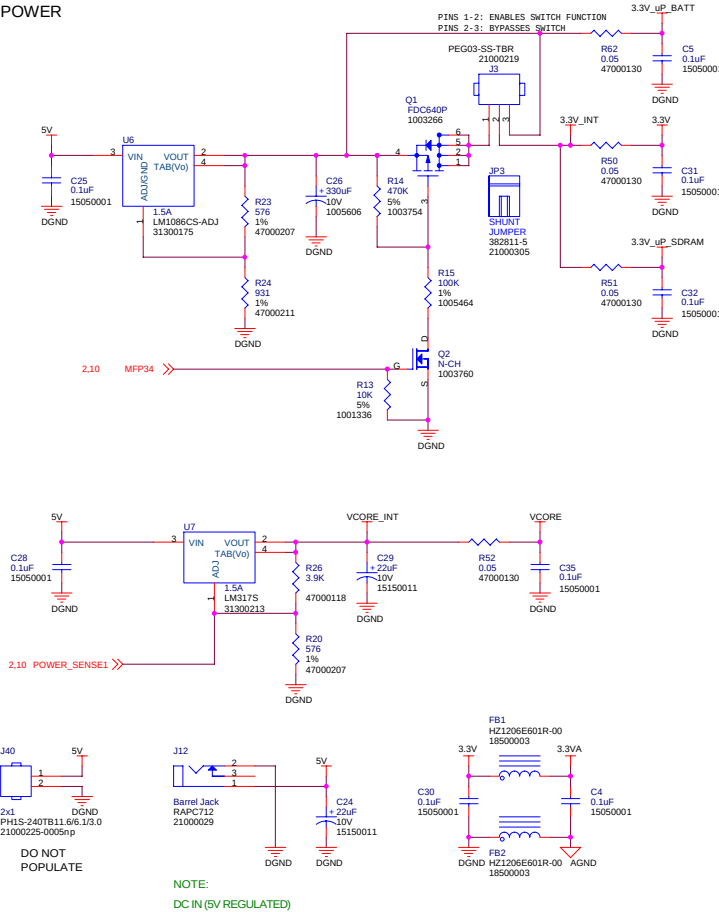
NMI - WAKEUP



STATUS  
LEDS



POWER



- REVISIONS I->J:
1. ADDED nRESET SIGNAL WHICH IS DIODE-OR'D SWITCH RESET AND uP\_nRESET\_OUT
  2. ADDED ON/OFF CONTROL TO 3.3V POWER SUPPLIES (AND JUMPER).
- REVISIONS H->I:
1. CHANGED C26 TO 1000014 (WAS 15150011)
  2. CHANGED S1 & S2 TO 51000018
- REVISIONS G->H:
1. MADE C27 A NO POP, DUE TO MSTR\_RST SIGNAL RISE TIME ISSUES
- REVISIONS E->F:
1. CHANGED J40 FROM BL\_VCC TO 5V AND GND
  2. MADE C36 A NO POP
- REVISIONS D->E:
1. ADDED THE CIRCUIT NMI - WAKEUP AND CHANGED NET uP\_NMI TO uP\_NMI - WAKEUP
- REVISIONS B->C:
1. CHANGED J40 FROM POPULATE TO DO NOT POPULATE
  2. SEPARATED THE 3.3V AND 3.3V\_uP\_SDRAM
  3. ADD SENSE RESISTORS AND .1uF CAPS TO THE 3 PLANES VCORE, 3.3V, AND 3.3V\_uP\_SDRAM
  4. CHANGED NET NAMES TO FOLLOW NEW NAMING CONVENTION SHOWING ACTIVE LEVEL IE. MSTR\_RST -> MSTR\_nRST.
  5. CHANGED REF DES J40np TO J40
- REVISIONS A->B:
1. CHANGED THE NETS THAT CONTROL THE LED'S FROM MFP11, MFP12, MFP4 TO uP\_STATUS1, uP\_STATUS2, CPLD\_GPIO1
  2. CHANGED U6 TO AN LDO REGULATOR

- REVISIONS J->K:
1. CHANGED C26 FROM 150uF TO 330uF
  2. CHANGED R14 FROM 10K TO 470K
  3. ADDED R15

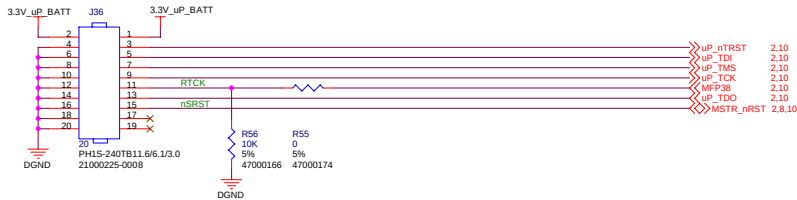
|                                                  |                            |                                                                                                |               |
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SH JTAG



ARM JTAG



ENGINE CPLD

DO NOT  
POPULATE

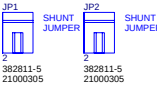


J6 JUMPER SETTINGS FOR  
NORMAL OPERATION

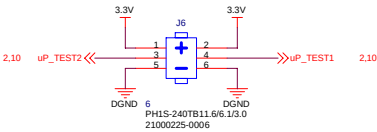
| ENGINE<br>TYPE | J6.1.3.5<br>uP_TEST2 | J6.2.4.6<br>uP_TEST1 | LPD PART<br>NUMBER               |
|----------------|----------------------|----------------------|----------------------------------|
| LH79520        | NO POP               | NO POP               | 80000113                         |
| LH75401        | NO POP               | NO POP               | 80000132<br>80000227             |
| LH7A400        | NO POP               | NO POP               | 80000126                         |
| LH7A404        | NO POP               | NO POP               | 80000127                         |
| RENESAS        | NO POP               | NO POP               | 80000114<br>80000117<br>80000115 |

J6 JUMPER SETTINGS FOR  
JTAG OPERATION

| ENGINE<br>TYPE | J6.1.3.5<br>uP_TEST2 | J6.2.4.6<br>uP_TEST1 | LPD PART<br>NUMBER               |
|----------------|----------------------|----------------------|----------------------------------|
| LH79520        | +                    | -                    | 80000113                         |
| LH75401        | +                    | -                    | 80000132<br>80000227             |
| LH7A400        | +                    | -                    | 80000126                         |
| LH7A404        | +                    | -                    | 80000127                         |
| RENESAS        | +                    | -                    | 80000114<br>80000117<br>80000115 |



NOTE:  
SEE QUICK START GUIDE OR  
HARDWARE SPEC FOR PICTORAL  
ILLUSTRATING PROPER JUMPER  
SETTINGS



REVISIONS I->J:

1. CHANGED ARM JTAG POWER TO 3.3V\_uP\_BATT

REVISIONS F->G:

1. UPDATED JUMPER TABLE FOR NORMAL OPERATION TO INDICATE THAT THE JUMPERS SHOULD BE NOT POPULATED
2. REMOVED NOTE REGARDING 75401L RTCK AND WGLER EMULATOR

REVISIONS D->F:

1. REMOVED uP\_TEST1 FROM J15.8 AND CONNECTED TO J15.10, GROUND J15.8
2. MOVED JUMPER BLOCK J6 OFF OF CIRCUIT FOR J15 FOR CLARITY

REVISIONS C->D:

1. CHANGED STYLE OF JUMPER SETTINGS TABLE AND CORRECTED THE SETTINGS FOR THE LH75401
2. CORRECTED THE SETTINGS FOR THE LH7A400

REVISIONS B->C:

1. CHANGED J6.5, J6.6 TO GND AND REMOVED R50
2. REMOVED JTAG PULLUPS FOR THE PROCESSOR R31 - R37 THESE ARE NOW LOCATED ON ALL CARD ENGINES
3. REMOVED JTAG PULLUPS FOR THE CPLD R43 - R46 THESE ARE NOW LOCATED ON ALL CARD ENGINES
4. CHANGED J36 TO A 20PIN CONNECTOR FOR THE ICE STANDARD 20PIN JTAG
5. ADDED SIGNAL uP\_RTCK TO MFP38 FROM THE 20PIN JTAG HEADER
6. CHANGED REF DES J41np TO J41

REVISIONS A->B:

1. CHANGED R34 TO A CONFIG RESISTOR. THIS WILL ALLOW THE SHARP ENGINE TO SWITCH BETWEEN JTAG MODE AND NORMAL MODES OF OPERATION.
2. DELETED CONFIGURATION RESISTORS R34, R37 AND ADDED A JUMPER BLOCK TO SWITCH BETWEEN JTAG MODE AND NORMAL MODE.

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| Size C                                     | Number 80000116    | Rev L         |  |
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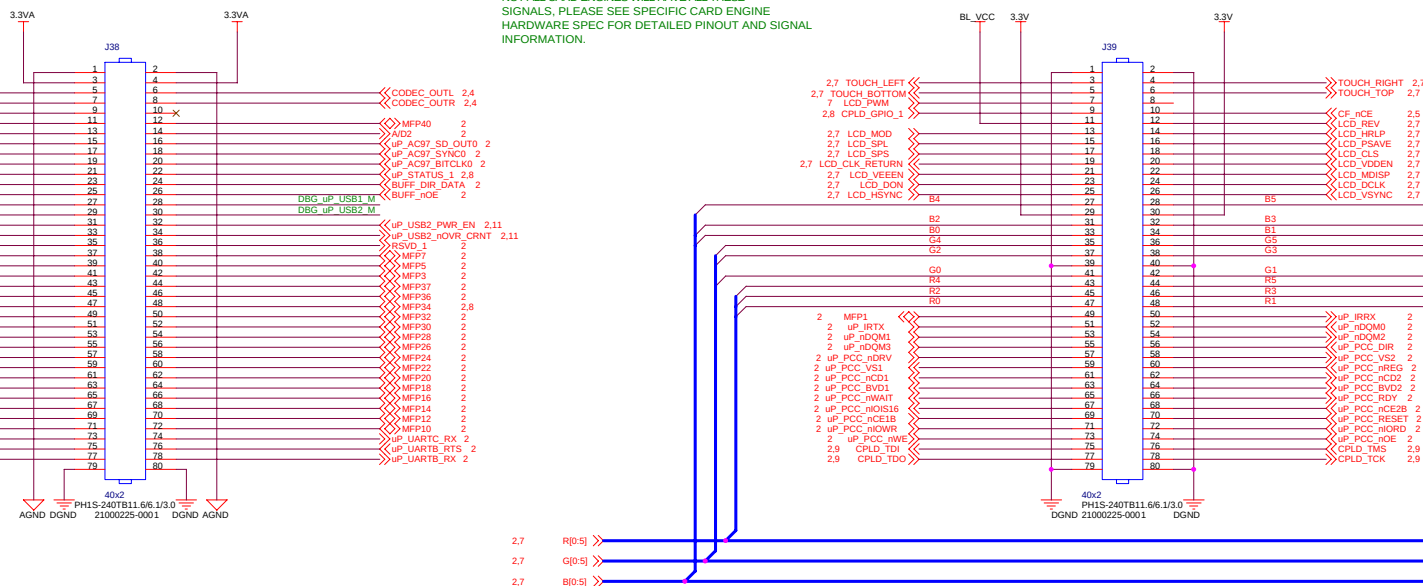
The left diagram shows the pin connections for J17 (40x2 pins). The pins are numbered 1 to 80. The connections are as follows:

- Pin 1: 3.3V
- Pin 2: 3.3V
- Pin 3: MSTR\_RST 2.8,9
- Pin 4: UP\_SW\_RESET 2
- Pin 5: SLOW\_MCMS 2
- Pin 6: BOOT\_MCMS 2
- Pin 7: WDRD 2.5
- Pin 8: WDRDY 2.5
- Pin 9: UP\_TEST2 2
- Pin 10: UP\_TMS 2.9
- Pin 11: UP\_TDI 2.9
- Pin 12: UP\_MODE2 2
- Pin 13: UP\_DREQ1 2
- Pin 14: UP\_DRAK1 2.8
- Pin 15: UP\_DACK1 2
- Pin 16: UP\_BUS\_CLK 2
- Pin 17: UP\_ICAS 2
- Pin 18: UP\_MMWE2 2
- Pin 19: UP\_nMWE2 2
- Pin 20: UP\_nMWE2 2
- Pin 21: UP\_nMWE2 2
- Pin 22: UP\_nMWE2 2
- Pin 23: UP\_A26 2
- Pin 24: UP\_A26 2
- Pin 25: UP\_A26 2
- Pin 26: UP\_A26 2
- Pin 27: UP\_A26 2
- Pin 28: UP\_A26 2
- Pin 29: UP\_A26 2
- Pin 30: UP\_A26 2
- Pin 31: UP\_A26 2
- Pin 32: UP\_A26 2
- Pin 33: UP\_A26 2
- Pin 34: UP\_A26 2
- Pin 35: UP\_A26 2
- Pin 36: UP\_A26 2
- Pin 37: UP\_A26 2
- Pin 38: UP\_A26 2
- Pin 39: UP\_A26 2
- Pin 40: UP\_A26 2
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- Pin 68: UP\_A26 2
- Pin 69: UP\_A26 2
- Pin 70: UP\_A26 2
- Pin 71: UP\_A26 2
- Pin 72: UP\_A26 2
- Pin 73: UP\_A26 2
- Pin 74: UP\_A26 2
- Pin 75: UP\_A26 2
- Pin 76: UP\_A26 2
- Pin 77: UP\_A26 2
- Pin 78: UP\_A26 2
- Pin 79: UP\_A26 2
- Pin 80: UP\_A26 2

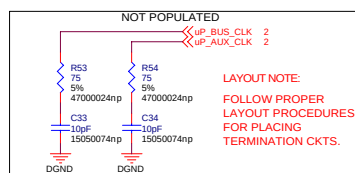
The right diagram shows the pin connections for J16 (40x2 pins). The pins are numbered 1 to 80. The connections are as follows:

- Pin 1: 3.3V VCORE
- Pin 2: 3.3V VCORE
- Pin 3: DBG\_ETHER\_TX(+) 2.3
- Pin 4: DBG\_ETHER\_RX(+) 2.3
- Pin 5: 2.3 ETHER\_nACT\_LED 2
- Pin 6: 2 nSTANDBY 2
- Pin 7: 2 UP\_IROD 2
- Pin 8: 2 UP\_IROD 2
- Pin 9: 2 UP\_IROD 2
- Pin 10: 2 UP\_IROD 2
- Pin 11: 2 UP\_IROD 2
- Pin 12: 2 UP\_IROD 2
- Pin 13: 2 UP\_IROD 2
- Pin 14: 2 UP\_IROD 2
- Pin 15: 2 UP\_IROD 2
- Pin 16: 2 UP\_IROD 2
- Pin 17: 2 UP\_IROD 2
- Pin 18: 2 UP\_IROD 2
- Pin 19: 2 UP\_IROD 2
- Pin 20: 2 UP\_IROD 2
- Pin 21: 2 UP\_IROD 2
- Pin 22: 2 UP\_IROD 2
- Pin 23: 2 UP\_IROD 2
- Pin 24: 2 UP\_IROD 2
- Pin 25: 2 UP\_IROD 2
- Pin 26: 2 UP\_IROD 2
- Pin 27: 2 UP\_IROD 2
- Pin 28: 2 UP\_IROD 2
- Pin 29: 2 UP\_IROD 2
- Pin 30: 2 UP\_IROD 2
- Pin 31: 2 UP\_IROD 2
- Pin 32: 2 UP\_IROD 2
- Pin 33: 2 UP\_IROD 2
- Pin 34: 2 UP\_IROD 2
- Pin 35: 2 UP\_IROD 2
- Pin 36: 2 UP\_IROD 2
- Pin 37: 2 UP\_IROD 2
- Pin 38: 2 UP\_IROD 2
- Pin 39: 2 UP\_IROD 2
- Pin 40: 2 UP\_IROD 2
- Pin 41: 2 UP\_IROD 2
- Pin 42: 2 UP\_IROD 2
- Pin 43: 2 UP\_IROD 2
- Pin 44: 2 UP\_IROD 2
- Pin 45: 2 UP\_IROD 2
- Pin 46: 2 UP\_IROD 2
- Pin 47: 2 UP\_IROD 2
- Pin 48: 2 UP\_IROD 2
- Pin 49: 2 UP\_IROD 2
- Pin 50: 2 UP\_IROD 2
- Pin 51: 2 UP\_IROD 2
- Pin 52: 2 UP\_IROD 2
- Pin 53: 2 UP\_IROD 2
- Pin 54: 2 UP\_IROD 2
- Pin 55: 2 UP\_IROD 2
- Pin 56: 2 UP\_IROD 2
- Pin 57: 2 UP\_IROD 2
- Pin 58: 2 UP\_IROD 2
- Pin 59: 2 UP\_IROD 2
- Pin 60: 2 UP\_IROD 2
- Pin 61: 2 UP\_IROD 2
- Pin 62: 2 UP\_IROD 2
- Pin 63: 2 UP\_IROD 2
- Pin 64: 2 UP\_IROD 2
- Pin 65: 2 UP\_IROD 2
- Pin 66: 2 UP\_IROD 2
- Pin 67: 2 UP\_IROD 2
- Pin 68: 2 UP\_IROD 2
- Pin 69: 2 UP\_IROD 2
- Pin 70: 2 UP\_IROD 2
- Pin 71: 2 UP\_IROD 2
- Pin 72: 2 UP\_IROD 2
- Pin 73: 2 UP\_IROD 2
- Pin 74: 2 UP\_IROD 2
- Pin 75: 2 UP\_IROD 2
- Pin 76: 2 UP\_IROD 2
- Pin 77: 2 UP\_IROD 2
- Pin 78: 2 UP\_IROD 2
- Pin 79: 2 UP\_IROD 2
- Pin 80: 2 UP\_IROD 2

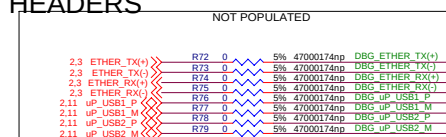
NOTE:  
NOT ALL CARD ENGINES WILL HAVE ALL THESE  
SIGNALS, PLEASE SEE SPECIFIC CARD ENGINE  
HARDWARE SPEC FOR DETAILED PINOUT AND SIGNAL  
INFORMATION.



## DIFF PAIRS TO DEBUG HEADERS



LAYOUT NOTE:  
FOLLOW PROPER  
LAYOUT PROCEDURES  
FOR PLACING  
TERMINATION CKTS.



**NOTE:**  
THE SDK SHIPS  
STANDARD WITH THESE  
RESISTORS NOT  
POPULATED TO MAKE  
THE CONNECTION FROM  
THE CARD ENGINE TO  
THE EXPANSION  
HEADERS, POPULATE  
R72 - R79.

REVISIONS C-&gt;D:

1. CHANGED NETS  
A39 - TOUCH\_TOP (was TOUCHX2)  
A38 - TOUCH\_BOTTOM (was TOUCHX)  
A37 - TOUCH\_RIGHT (was TOUCHY2)  
A36 - TOUCH\_LEFT (was TOUCHY)  
2. REMOVED THE NET CF\_RDYNBSY AND  
RENAMED THE NET RSVD\_1

### E REVISIONS D->E:

1. CHANGED NET NAME OF uP\_NMI (J16.12) TO MuP\_NMI - WAKEUP TO ACCOMODATE THE a400 AND A404.

REVISIONS E<sub>1</sub>→E<sub>2</sub>

1. ADDED R72 - R79 TO SEPARATE DIFF  
PAIRS FROM EXPANSION HEADERS

REVISIONS B-&gt;C

1. ADDED TERMINATIONS TO uP\_AUX\_CLK AND uP\_BUS\_CLK
2. CHANGED NET NAMES TO FOLLOW NEW NAMING CONVENTION SHOWING ACTIVE LEVEL IE. MSTR\_RST -> MSTR\_nRST.
3. RENAMED NET LCD\_CLKIN -> LCD\_CLK\_RETURN AND NET LCD\_CLKOUT -> LCD\_DCLK

4. SWITCHED THE PINS ON J39 THAT NETS LCD\_PSAVE AND LCE\_REV GO TO
5. CHANGED REF DES OF R53np, R54np, C33np, C34np TO R53, R54, C33, C34
- REVISIONS A->B:

## 1. CHANGES

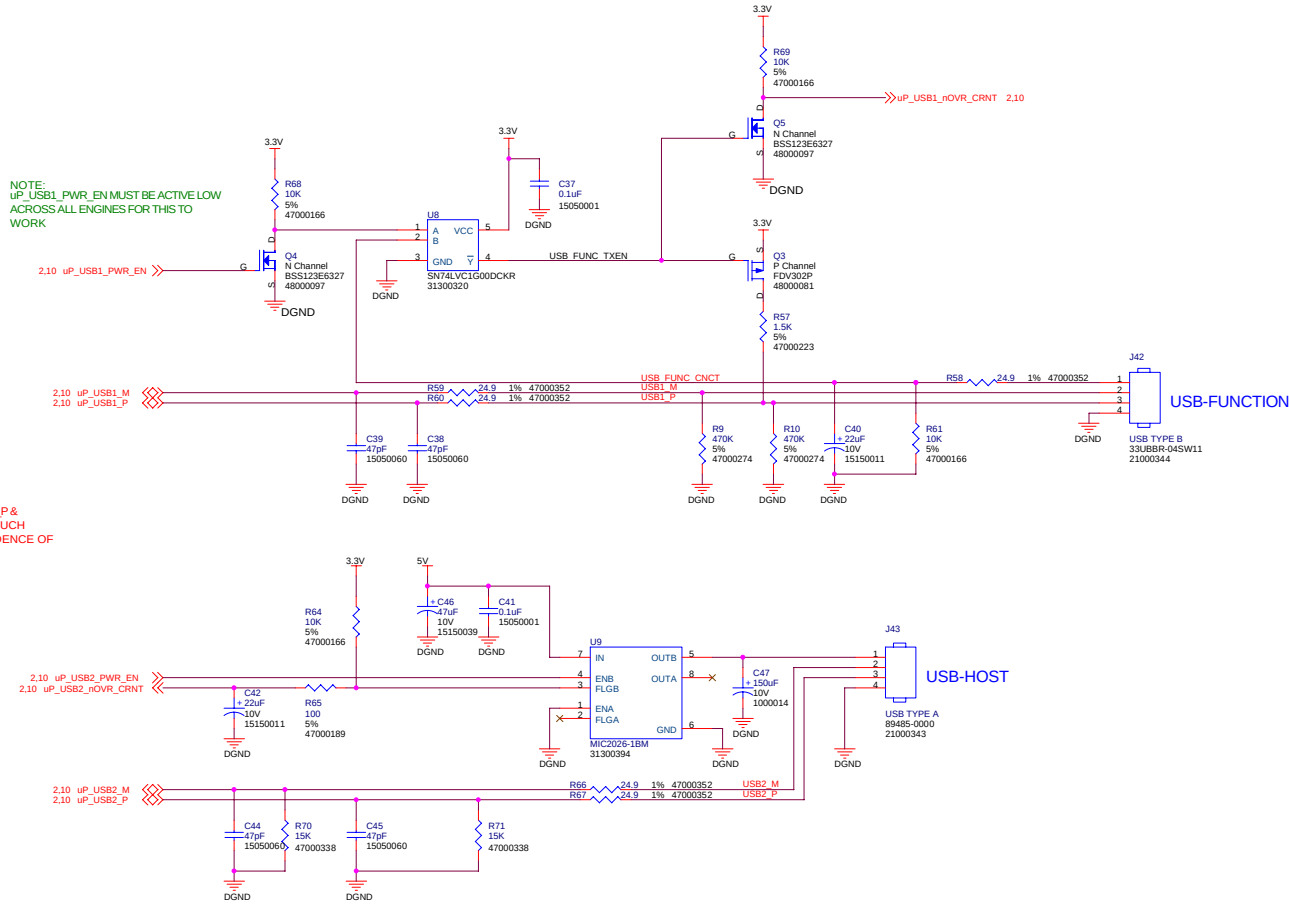
1. CHANGED THE NAMES OF THE LCD DATA LINES
2. CHANGED THE NET NAMES OF EVB1 AND EVB2 TO CF\_nCE AND CF\_BSYnRDY RESPECTIVELY

REVISIONS F-&gt;L:

1. Changed Net uP\_UARTB\_DSR to uP\_UARTB\_RTS

|                                                                                       |   |                                            |          |                                                                                                 |  |                |       |
|---------------------------------------------------------------------------------------|---|--------------------------------------------|----------|-------------------------------------------------------------------------------------------------|--|----------------|-------|
| Schematic Modify Date = Friday, October 12, 2007                                      |   |                                            |          | 411 WASHINGTON AVE. N.<br>MINNEAPOLIS, MN 55401<br>PHONE: (612) 672-9495<br>FAX: (612) 672-9489 |  |                |       |
|  |   | <b>LOGIC</b><br><b>PRODUCT DEVELOPMENT</b> |          |                                                                                                 |  |                |       |
| Title Zoom SDK Application Board                                                      |   |                                            |          |                                                                                                 |  |                |       |
| Size                                                                                  | C | Number                                     | 80000116 |                                                                                                 |  |                | Rev L |
| Design Create Date = Monday, July 01, 2002                                            |   |                                            | Project  |                                                                                                 |  | LCE-APP-10     |       |
|                                                                                       |   |                                            |          |                                                                                                 |  | Sheet 10 Of 12 |       |

# 11 - USB HOST/FUNCTION



12 - ECO LIST

| Revision Control |     |                                                                                                                                                 |          |
|------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| ECO Number       | Rev | Description of Change                                                                                                                           | Date     |
|                  | A   | RELEASE FOR PILOT RUN                                                                                                                           | 11/14/02 |
|                  |     | 1. CHANGED THE NET NAMES OF THE LCD DATA LINES. PG2,7,10                                                                                        |          |
|                  |     | 2. CHANGED THE NET NAMES OF EVB1 AND EVB2 TO CF_nICE AND CF_BSYnRDY RESPECTIVELY. PG2,5                                                         |          |
|                  |     | 3. REMOVED NET uP_MAO AND TIED THAT PIN ON J7 TO GND. PG5                                                                                       |          |
|                  |     | 4. REMOVED HOT SWAPPABILITY OF CF CARD. DELETED NETS uP_PCCDRV AND CF_3.3V, AND COMPONENTS Q1, C10. PG5                                         |          |
|                  |     | 5. ADDED ADDRESS LINES uP_MA3-9 AND uP_MALL FOR GREATER FUNCTIONALITY AND USABILITY OF MORE CF CARDS. PG5                                       |          |
|                  |     | 6. CHANGED THE NETS THAT CONTROL THE LEDS FROM MFP11, MFP12, MFP4 TO uP_STATUS1, uP_STATUS2, CPLD_GPIO1. PG8,2,10                               |          |
|                  |     | 7. CHANGED R34 TO A CONFIG RESISTOR. PG9                                                                                                        |          |
|                  |     | 8. REPLACED CONFIGURATION RESISTORS R34, R37 W/ JUMPER BLOCK TO SWITCH BETWEEN JTAG MODE AND NORMAL MODE. PG9                                   |          |
|                  |     | 9. CHANGED U6 TO AN LDO REGULATOR                                                                                                               |          |
|                  | B   | RELEASE FOR PRODUCTION                                                                                                                          | 1/6/03   |
|                  |     | 10. CHANGED NET THAT CONNECTS TO REG ON J7-44 FROM uP_MALL TO uP_MAI3                                                                           | 2/7/03   |
|                  |     | 11. CHANGED J40 FROM POPULATE TO DO NOT POPULATE                                                                                                | 2/7/03   |
|                  |     | 12. SEPARATED THE 3.3V AND 3.3V_uP_SDRAM ON PINS 61-64 OF THE SODIMM CON                                                                        | 2/7/03   |
|                  |     | 13. CHANGED THE IMPEDENCE MATCHING VOLTAGE ON THE ENET TX AND RX LINES TO 3.3V_WRLAN                                                            | 2/10/03  |
|                  |     | 14. ADDED 3.3V_WRLAN TO THE DIMM CONNECTOR J1C19                                                                                                | 2/10/03  |
|                  |     | 15. CHANGED THE 60PIN LCD CONNECTOR J11 TO A SHROUDED/KEYED W/ EJECTOR TABS TYPE                                                                | 2/10/03  |
|                  |     | 16. ADDED TERMINATIONS TO uP_AUX_CLK AND uP_BUS_CLK, AND DO NOT POPULATE                                                                        | 2/10/03  |
|                  |     | 17. CHANGED J6,5, J6,6 TO GND AND REMOVE R50                                                                                                    | 2/10/03  |
|                  |     | 18. REMOVED JTAG PULLUPS FOR THE PROCESSOR R31 - R37 THESE ARE NOW LOCATED ON ALL CARD ENGINES                                                  | 2/10/03  |
|                  |     | 19. REMOVED JTAG PULLUPS FOR THE CPLD R43 - R46 THESE ARE NOW LOCATED ON ALL CARD ENGINES                                                       | 2/10/03  |
|                  |     | 20. CHANGED J36 TO A 20PIN CONNECTOR FOR THE ICE STANDARD 20PIN JTAG                                                                            | 2/25/03  |
|                  |     | 21. ADD SENSE RESISTORS AND 1uF CAPS TO THE 3 PLANES VCOOE, 3.3V, AND 3.3V_uP_SDRAM                                                             | 2/25/03  |
|                  |     | 22. CHANGED NET NAMES TO FOLLOW NEW NAMING CONVENTION SHOWING ACTIVE LEVEL IE. MSTR_RST -> MSTR_HRST.                                           | 2/25/03  |
|                  |     | 23. CHANGED THE NET NAMES OF THE UNK AND ACT LED NETS TO ETHER_nACT_LED AND ETHER_nLNK_LED                                                      | 2/25/03  |
|                  |     | 24. CHANGED R3 AND R4 FROM 47 OHM 5%S TO 49.9 OHM 1%S                                                                                           | 2/25/03  |
|                  |     | 25. GROUNDED PINS 4 AND 5 OF P1, PER PULSE CONNECTOR SPEC                                                                                       | 2/25/03  |
|                  |     | 26. CHANGED R1,R2,R5,R6 FROM 24 OHM 5%S TO 24.9 OHM 1%S                                                                                         | 2/25/03  |
|                  |     | 27. ADDED SIGNAL uP_RTCK TO MFP38 FROM THE 20PIN JTAG HEADER                                                                                    | 2/26/03  |
|                  |     | 28. REMOVED PULLUP ON CF_RDYnBSY                                                                                                                | 2/26/03  |
|                  |     | 29. IMPLEMENTED CONVERSION TO NEW NET NAMING CONVENTION                                                                                         | 2/26/03  |
|                  |     | 30. SWITCHED THE PINS ON J1A THAT NETS LCD_PSAVE AND LCE_REV GO TO                                                                              | 3/05/03  |
|                  |     | 31. RENAMED NET LCD_CLKIN -> LCD_CLK_RETURN AND NET LCD_CLKOUT -> LCD_DCLK                                                                      | 3/05/03  |
|                  |     | 32. CHANGED REMOVED THE np SUFFIX ON ALL NO POP PARTS AND ADDED A FIELD TO INDICATE THIS IN THE BOM.                                            | 3/05/03  |
|                  |     | 33. REMOVED R22                                                                                                                                 | 3/05/03  |
|                  | C   | RELEASE FOR PROTO RUN                                                                                                                           | 3/05/03  |
|                  |     | 34. CHANGED NET THAT CONNECTS TO REG ON J7-44 FROM uP_MAI3 TO uP_MAI2                                                                           | 3/12/03  |
|                  |     | 35. CHANGED STYLE OF JUMPER SETTINGS TABLE AND CORRECTED THE SETTINGS FOR THE LH75401                                                           | 3/26/03  |
|                  |     | 36. CHANGED NETS A39 - TOUCH_TOP (was TOUCHX2), A38 - TOUCH_BOTTOM (was TOUCHX), A37 - TOUCH_RIGHT (was TOUCHY2), A36 - TOUCH_LEFT (was TOUCHY) | 3/26/03  |
|                  |     | 37. REMOVED THE NET CF_RDYnBSY FROM J7-37 AND RENAMED THIS NET RSV_D_1 ON THE EXPANSION HEADERS AND EXPANSIONS BUS                              | 3/29/03  |
|                  | D   | RELEASE FOR PRODUCTION                                                                                                                          | 4/10/03  |
|                  |     | 38. CORRECTED THE JUMPER SETTINGS IN THE JTAG TABLE FOR THE LH7A400                                                                             | 4/28/03  |
|                  |     | 39. ADDED THE CIRCUIT WAKEUP CONTAINING PARTS: C7 AND S7                                                                                        | 5/13/03  |
|                  |     | 40. ADDED USB HOST AND FUNCTION CIRCUITRY                                                                                                       | 5/25/03  |
|                  | E   | RELEASE FOR PRODUCTION                                                                                                                          | 5/29/03  |

| Revision Control |     |                                                                                                                     |          |
|------------------|-----|---------------------------------------------------------------------------------------------------------------------|----------|
| ECO Number       | Rev | Description of Change                                                                                               | Date     |
|                  |     | 41. ADDED USB HOST IMPEDENCE MATCHING DISCRETES TO USB2_M AND USB2_P                                                | 7/14/03  |
|                  |     | 42a. ADDED LOGIC TO PROPERLY IMPLEMENT USB FUNCTION ACROSS ALL CARD ENGINES.                                        | 7/14/03  |
|                  |     | 42b. CHANGED THE HOST POWER CONTROLLER TO THE "1" DEVICE WHICH IS ACTIVE HIGH INSTEAD OF ACTIVE LOW                 | 7/14/03  |
|                  |     | 43. ADDED R72 - R79 TO SEPARATE DIFF PAIRS FROM EXPANSION HEADERS                                                   | 7/21/03  |
|                  |     | 44. REMOVED uP_TEST1 FROM J15.8 AND CONNECTED TO J15.10, GROUNDED J15.8                                             | 7/24/03  |
|                  |     | 45. MOVED JUMPER BLOCK J6 OFF OF CIRCUIT FOR J15 FOR CLARITY                                                        | 7/24/03  |
|                  |     | 46. SUBMITTED PART FOR LCE-APP-10 AND UPDATED BLOCK DIAGRAM AND TITLE PAGE                                          | 7/24/03  |
|                  |     | 47. CHANGED J40 FROM BL_VCC AND GND TO 5V AND GND                                                                   | 7/24/03  |
|                  |     | 48. CONNECTED CT1 TO 3.3V_WRLAN PER 91C111 SCHEMATIC CHECKLIST PROVIDED BY SMSC                                     | 7/25/03  |
|                  |     | 49. CHANGED THE CONNECTION OF CT1 TO 3.3V_WRLAN DIRECTLY TO ONE THAT USES A 0OHM (R80) UNTIL QA HAS BEEN COMPLETED. | 7/28/03  |
|                  |     | 50. MADE C36 A NO POP                                                                                               | 8/15/03  |
|                  | F   | RELEASE FOR PRODUCTION                                                                                              | 8/15/03  |
|                  |     | 51. ADDED BOX AROUND THE NO POP RESISTOR ON ENET CONNECTOR                                                          | 9/16/04  |
|                  |     | 52. REMOVED A0 FROM CF CONNECTOR FOR COMPATABILITY WITH A400 BSC IN A 16BIT AREA                                    | 4/16/04  |
|                  |     | 53. UPDATED JUMPER TABLE FOR NORMAL OPERATION TO INDICATE THAT THE JUMPERS SHOULD BE NOT POPULATED                  | 4/16/04  |
|                  |     | 54. REMOVED NOTE REGARDING 75401, RTCK AND WIGGLER EMULATOR                                                         | 4/16/04  |
|                  | G   | RELEASE FOR PRODUCTION                                                                                              | 4/23/04  |
|                  |     | USB - ADDED 47uF CAP TO HOST CONNECTOR POWER PIN AND HOST POWER CONTROLLER POWER PIN                                | 6/21/04  |
|                  |     | CF - INVERTED RESET SIGNAL TO CF CARD THIS SIGNAL IS ACTIVE HIGH                                                    | 6/21/04  |
|                  |     | CHANGED C47 FROM 47uF TO 150uF PER USB 2.0 SPEC AND CHECKLIST                                                       | 10/19/04 |
|                  |     | MADE C27 A NO POP, DUE TO MSTR_RST SIGNAL RISE TIME ISSUES                                                          | 10/19/04 |
|                  | H   | RELEASE FOR PRODUCTION                                                                                              | 10/21/04 |
|                  |     | CHANGED C7 AND C26 TO 1000014 (WAS 15150011)                                                                        | 06/02/05 |
|                  |     | ADDED R9 AND R10.                                                                                                   | 06/02/05 |
|                  |     | CHANGED S1 & S2 TO 51000018                                                                                         | 06/02/05 |
|                  | I   | RELEASE FOR PRODUCTION                                                                                              | 06/02/05 |
|                  |     | ADDED DIODE OR FUNCTION TO SDK RESET                                                                                | 05/16/06 |
|                  |     | ADDED 3.3V_uP_BATT AND SWITCH TO ENABLE POWER TO THE OTHER 3.3V SUPPLIES                                            | 05/16/06 |
|                  |     | CHANGED PIN 61 OF SODIMM TO 3.3V_uP_BATT                                                                            | 05/16/06 |
|                  | J   | RELEASE FOR PRODUCTION                                                                                              | 06/21/06 |
|                  |     | ADDED R83-R88 AND C48-C53                                                                                           | 09/13/06 |
|                  |     | CHANGED C26 FROM 150uF TO 330uF                                                                                     | 09/13/06 |
|                  |     | CHANGED R14 FROM 10K TO 470K                                                                                        | 09/13/06 |
|                  |     | ADDED R15                                                                                                           | 09/13/06 |
|                  |     | CHANGED C7 FROM 150uF TO 22uF                                                                                       | 09/13/06 |
|                  | K   | RELEASE FOR PRODUCTION                                                                                              | 09/14/06 |
| EC04211          | L   | Changed Net Name uP_UARTB_DSR to uP_UARTB_RTS                                                                       | 10/05/07 |

Schematic Modify Date = Friday, October 05, 2007

 **LOGIC**  
PRODUCT DEVELOPMENT

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Title Zoom SDK Application Board

Size C      Number 80000116      Rev L

Design Create Date = Monday, July 01, 2002      Project LCE-APP-10      Sheet 12 Of 12