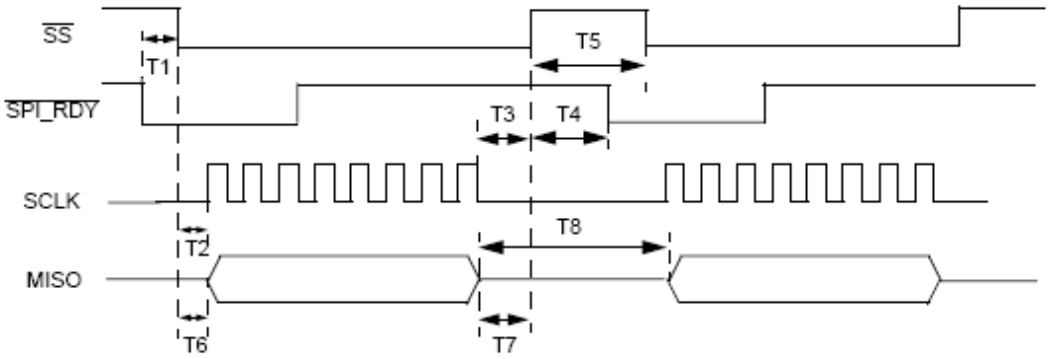

Figure 52-1 CSPI Timing

Table 52-3 CSPI timing Characteristic

Num	CHARACTERISTIC	MIN	MAX	Unit
1	SPIRDY to SS output low	-	4	T[1]
2	SS output low to first SCLK edge	2	-	T
3	Last SCLK edge to SS output high	2	-	T
4	SS output high to SPIRDY low	1	-	T
5	SS output pulse width/ input pulse width	2*ipg_clk +WAIT[2]	-	T
6	SS input low to first valid data	2	-	T
7	Last valid data to SS output high	1	-	T
8	pause between data word	4	-	T

[1]T = SPI clock period.
[2]Number of SPI clock or 32.768KHz clocks per Sample Period Control Register. For 32.768KHz clock source, there may be an uncertainty of one 32.768KHz clock period that is caused by clock domain crossing in design.