01 - TITLE PAGE

PROJECT:	iMX31-10
PART NUMBER:	1004734
ASSEMBLY NAME:	iMX31-10 SOM
SCHEMATICS:	KTL,NJK

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COLOR LEGEND

NOTE:
NOTES IN GREEN TEXT ARE GENERAL DESIGN OR SCHEMATIC NOTES

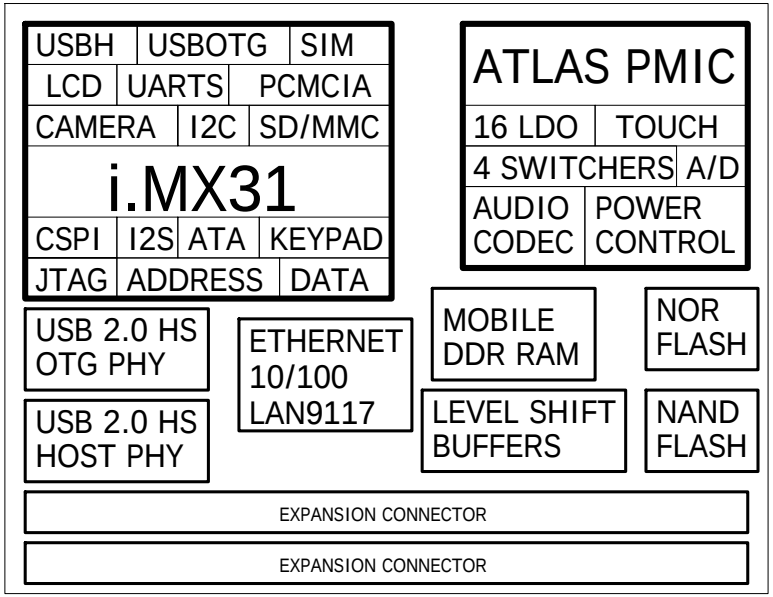
LAYOUT NOTE:
NOTES IN RED TEXT ARE PCB LAYOUT RECOMMENDATIONS OR GUIDLINES

NET NAMES

NET NAMES IN GREEN TEXT ARE NETS THAT ARE NOT DIRECTLY CONNECTED WITH A VISIBLE WIRE ON SINGLE SCHEMATIC PAGE, BUT USE THIS CONVENTION TO MAKE THE SCHEMATIC EASIER TO READ

NET NOTE

NET NOTES IN BLACK TEXT INDICATE A PARTICULAR FUNCTIONALITY OF A SPECIFIC NET, IT IS NOT A NET NAME MERELY TEXT AND HAS NO AFFECT ON THE DRC.



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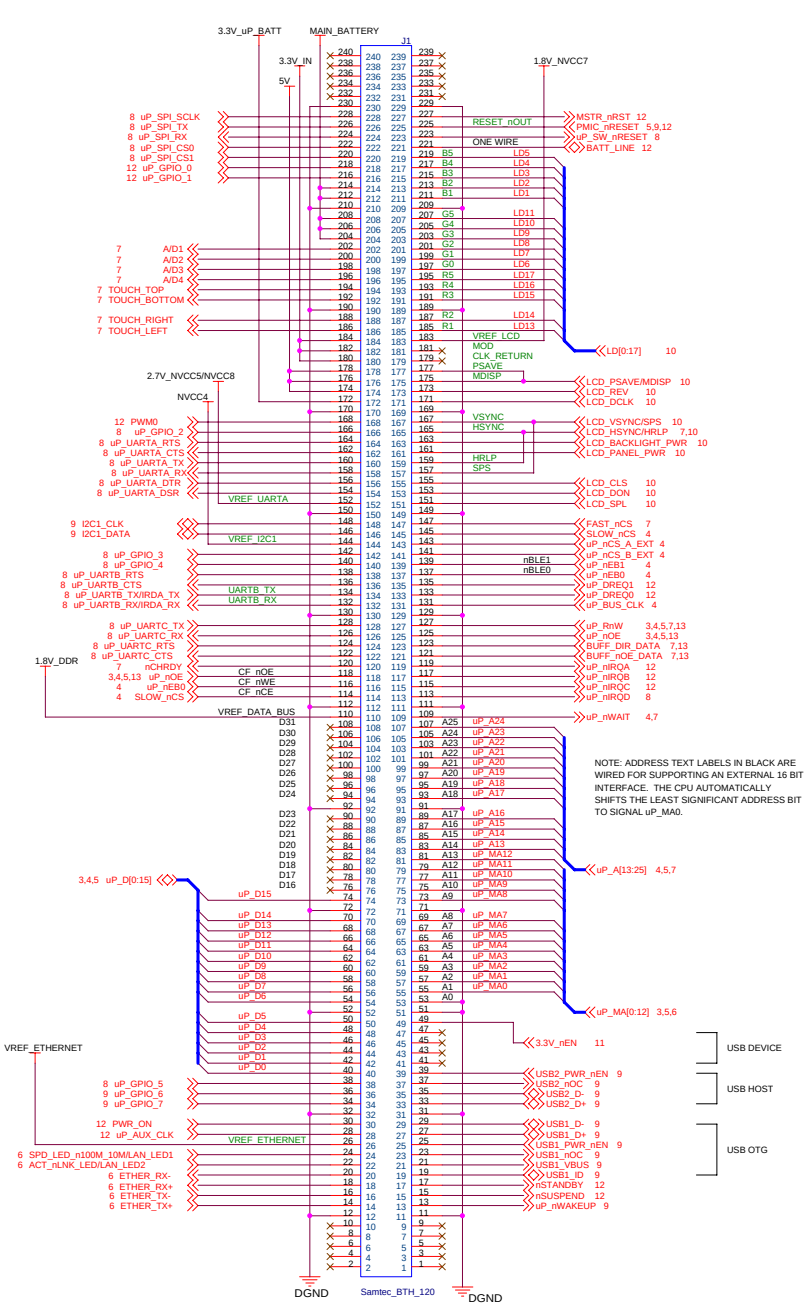
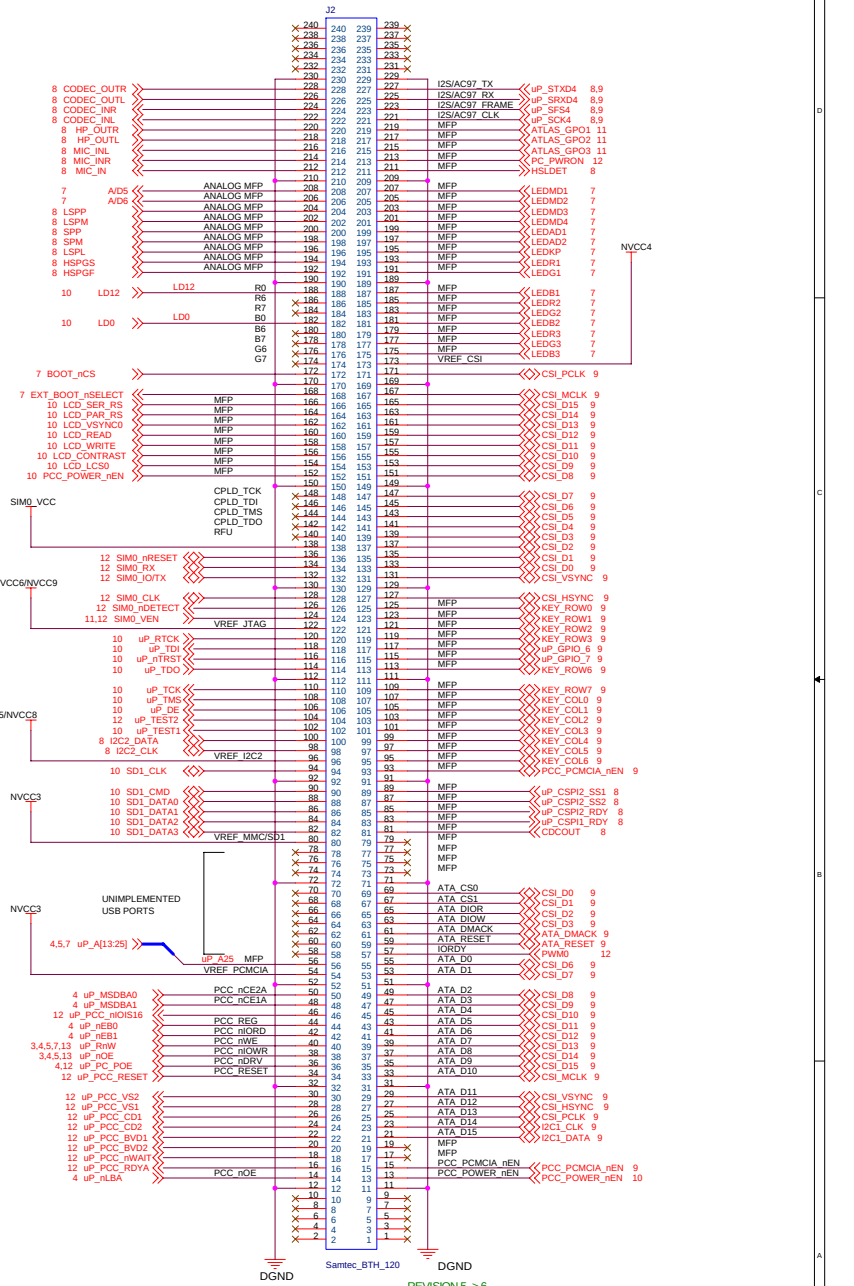
02 - EXPANSION BUS

NOTE: MAIN_BATTERY FIXED AT 3.3V ON SDK BASEBOARD, HOWEVER, ANY VOLTAGE WITHIN ATLAS (MC13783) PMIC SPECIFICIATIONS CAN BE USED. TYPICALLY CONNECTED DIRECTLY TO A BATTERY PACK.





REVISION 5 -> 6
1) ADDED PCC_POWER_nEN ON J2 PIN 13
2) ADDED PCC_PCMCIA_nEN ON J2 PIN 15

REVISION 4 -> 5
1) CHANGED LCD INTERFACE: LD0-5 --> B0-5; LD12-17 --> R0-5

REVISION 2 -> 3
1) SHIFTED ADDRESS BUS ON J1 UP ONE BIT
2) GROUNDED A0 ADDRESS OUTPUT ON J1
3) ADDED uP_AD25 to J2 PIN 56

REVISION 3 -> 4
1) CHANGED LCD_CONTACT TO LCD_CONTRAST
2) CHANGED PCC_nIOWR AND CF_nOE TO uP_nOE
3) ADDED BOOT_nCS AND EXT_BOOT_nSELECT

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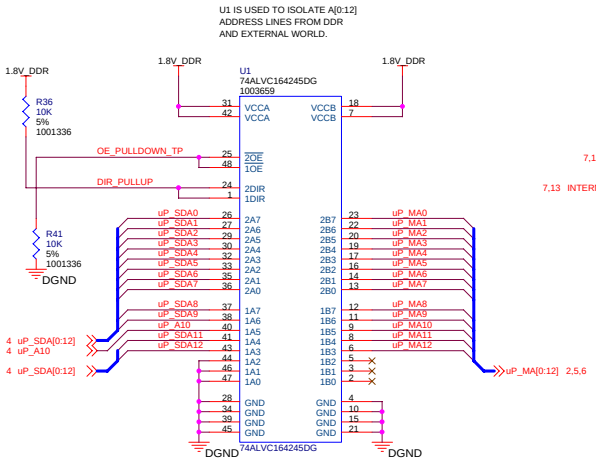
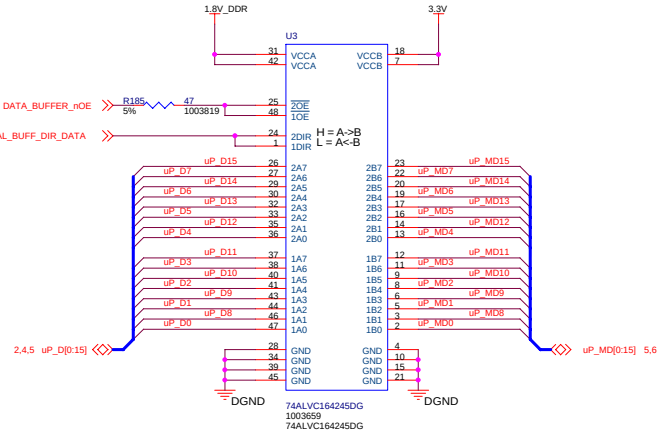
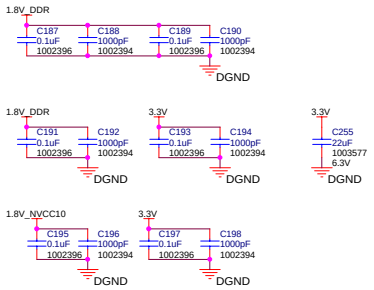
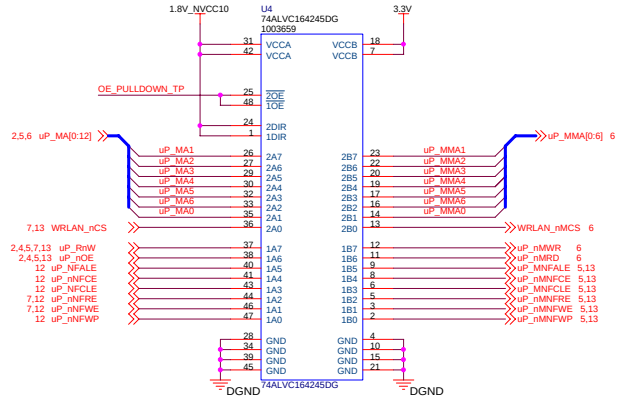
03 - WEIM BUS BUFFERS





PLACE ONE CAPACITOR NEAR EACH IC POWER PIN





REVISION 2 -> 3
1) CHANGED U4 PIN 36 FROM uP_MA7 TO uP_MA0.
2) CHANGED U4 PIN 13 FROM uP_MMA7 TO uP_MMA0

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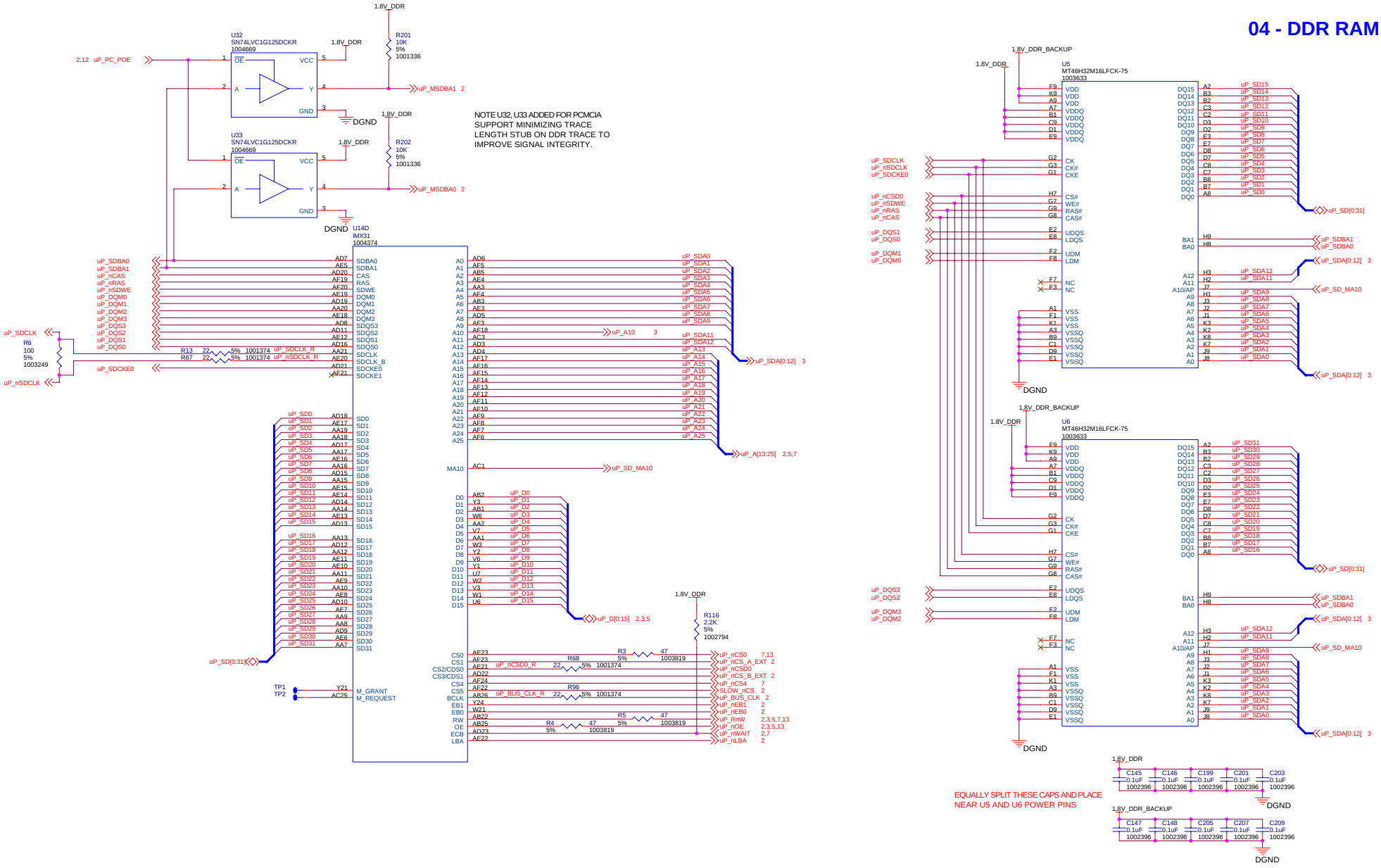
04 - DDR RAM



REVISION 5 -> 6
1) REMOVED C253, C254, C200, C202, C204, C206, C208-210.
2) ADDED R6

REVISION 4 -> 5
1) ADDED R201 AND R202
2) CHANGED OE ON U32 AND U33 TO BE CONTROLLED BY uP_PC_POE

REVISION 3 -> 4
1) CHANGED U38, U39 TO U32, U33 ACTIVE LOW
SINGLE BIT BUFFERS

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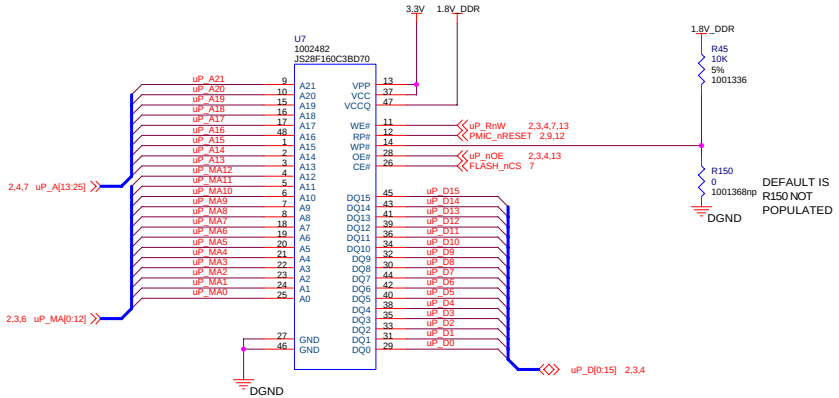
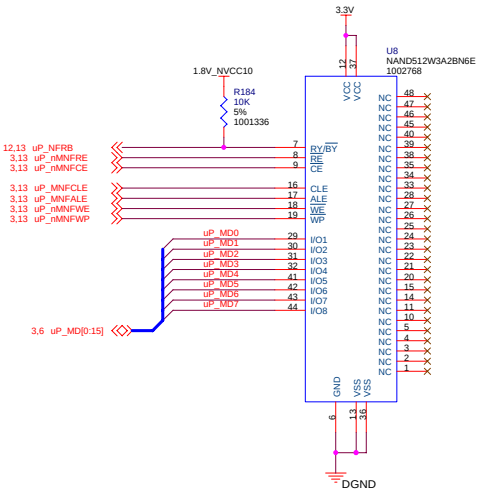
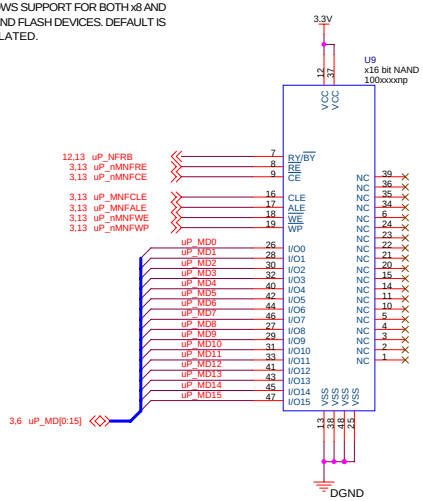
05 - FLASH

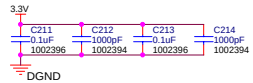


NOTE: PADS FOR U9 OVERLAP U8, ONLY ONE DEVICE WILL EVER BE POPULATED AT ONCE. THIS ALLOWS SUPPORT FOR BOTH x8 AND x16 BIT NAND FLASH DEVICES. DEFAULT IS U8 POPULATED.





PLACE ONE CAPACITOR NEAR EACH IC POWER PIN



REVISION 2 -> 3
1) SHIFTED ADDRESS BUS UP ONE BIT ON U7

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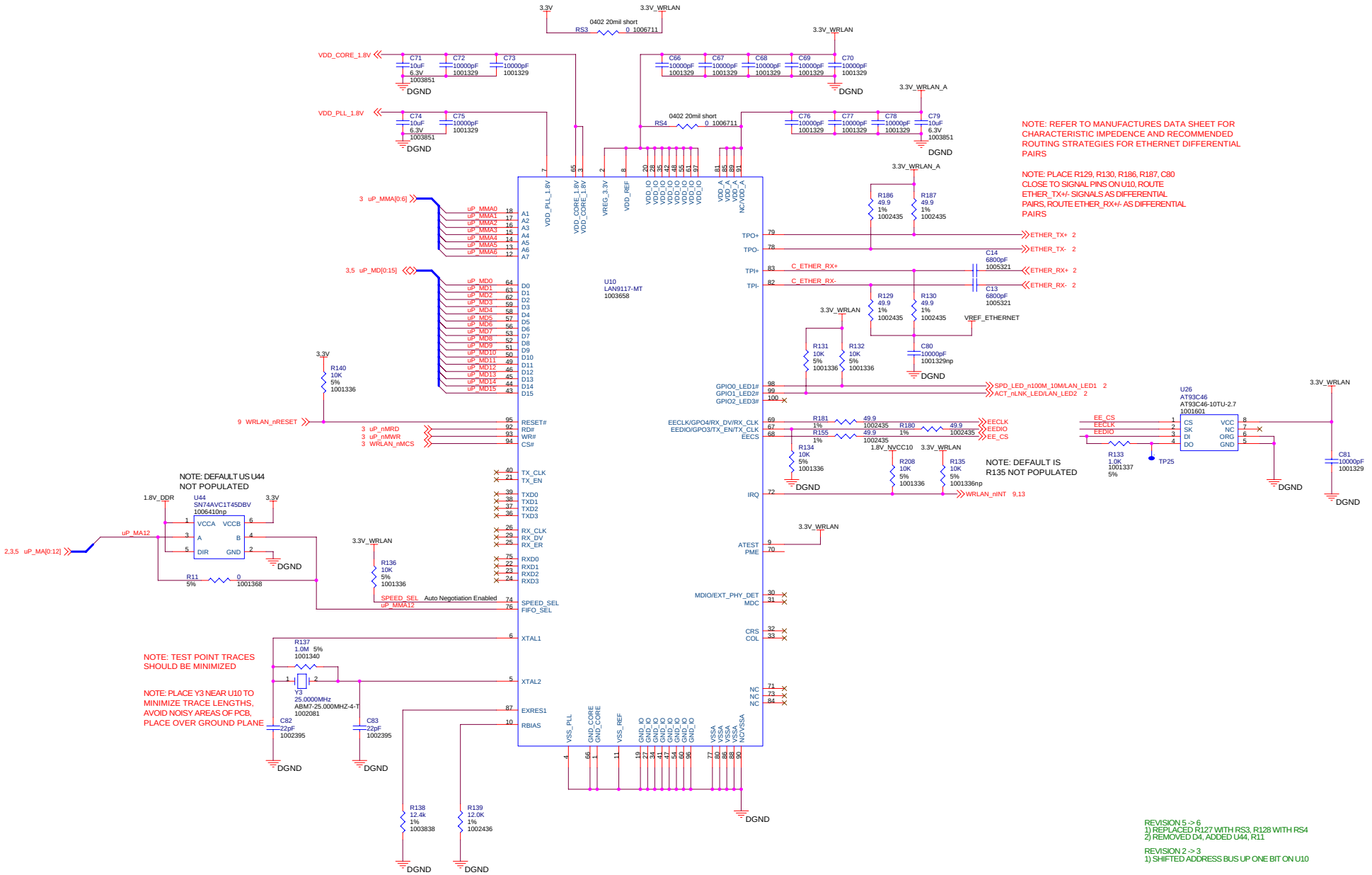
06 - WIRED LAN



REVISION 5 -> 6
1) REPLACED R127 WITH RS3, R128 WITH RS4
2) REMOVED D4, ADDED U44, R11

REVISION 2 -> 3
1) SHIFTED ADDRESS BUS UP ONE BIT ON U10

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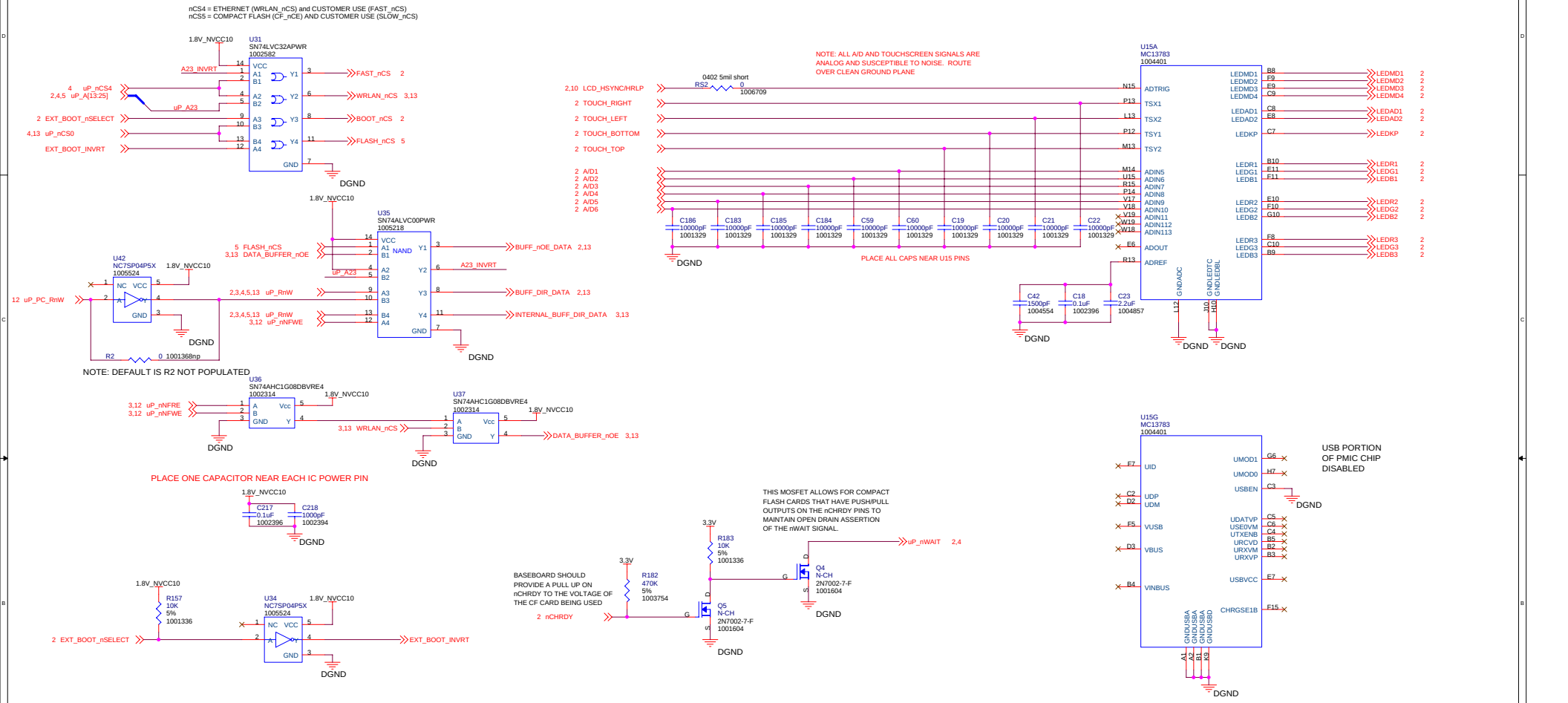
07 - LOGIC/ADC



REVISION 5 -> 6
1) REMOVED C251
2) ADDED U42, PADS FOR R2
3) REPLACED R35 WITH RS2
4) SWAPPED X AND Y TOUCH SIGNAL GROUPS, SWAPPED X INPUTS.

REVISION 3 -> 4
1) CHANGED U35 PIN 12 INPUT FROM uP_nNFRE TO uP_nNFWE
2) CHANGED TO A23 FOR ADDRESS CONTROL LINE FOR DIFFERENT MEMORY AREAS
3) CHANGED U35 PIN 13 TO uP_RnW
4) DROPPED SUPPORT CF_nCE SIGNAL, ADDED EXTERNAL NOR BOOT OPTION
5) CHANGED U34 FROM BUFFER (INCORRECT PART) TO INVERTER

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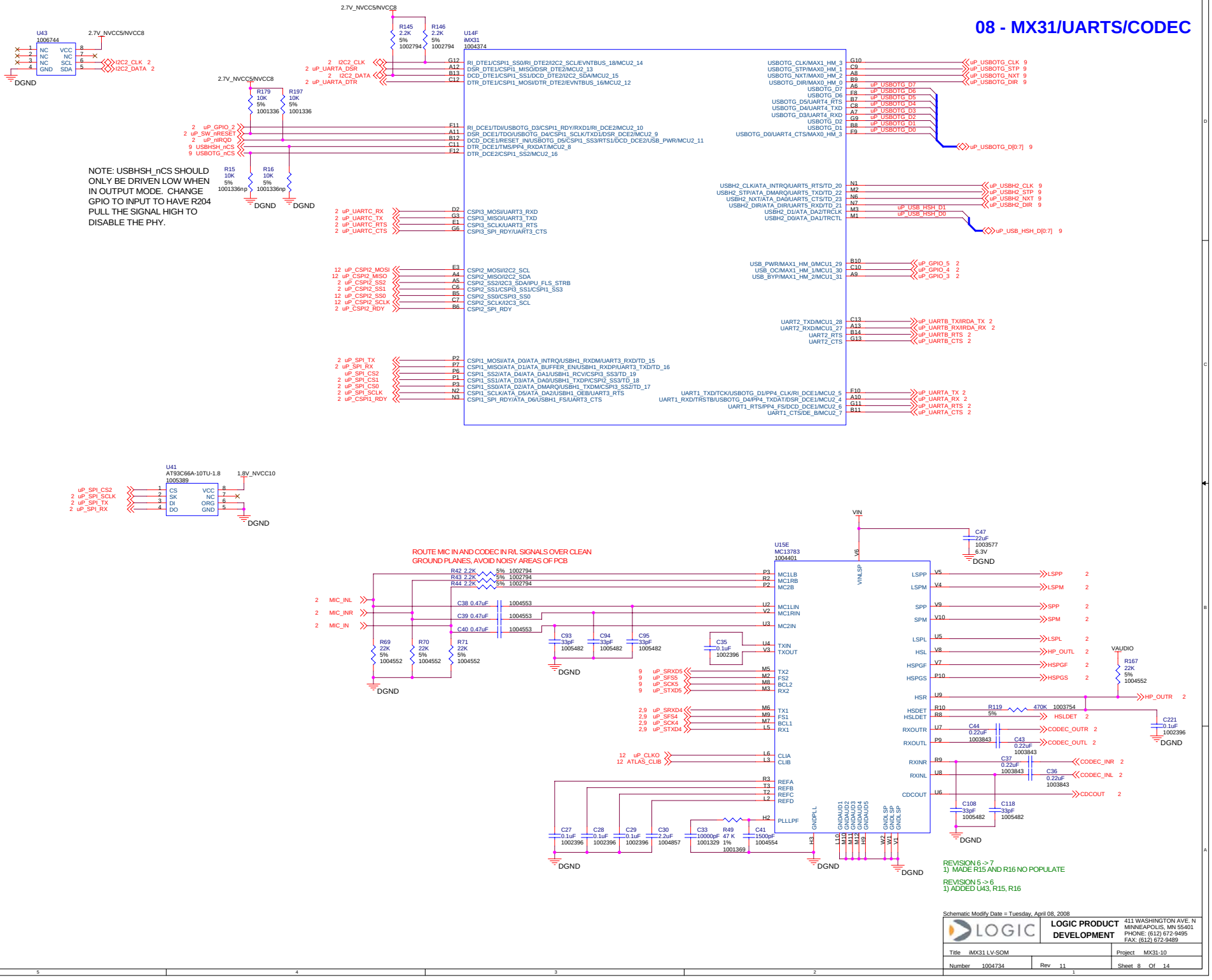
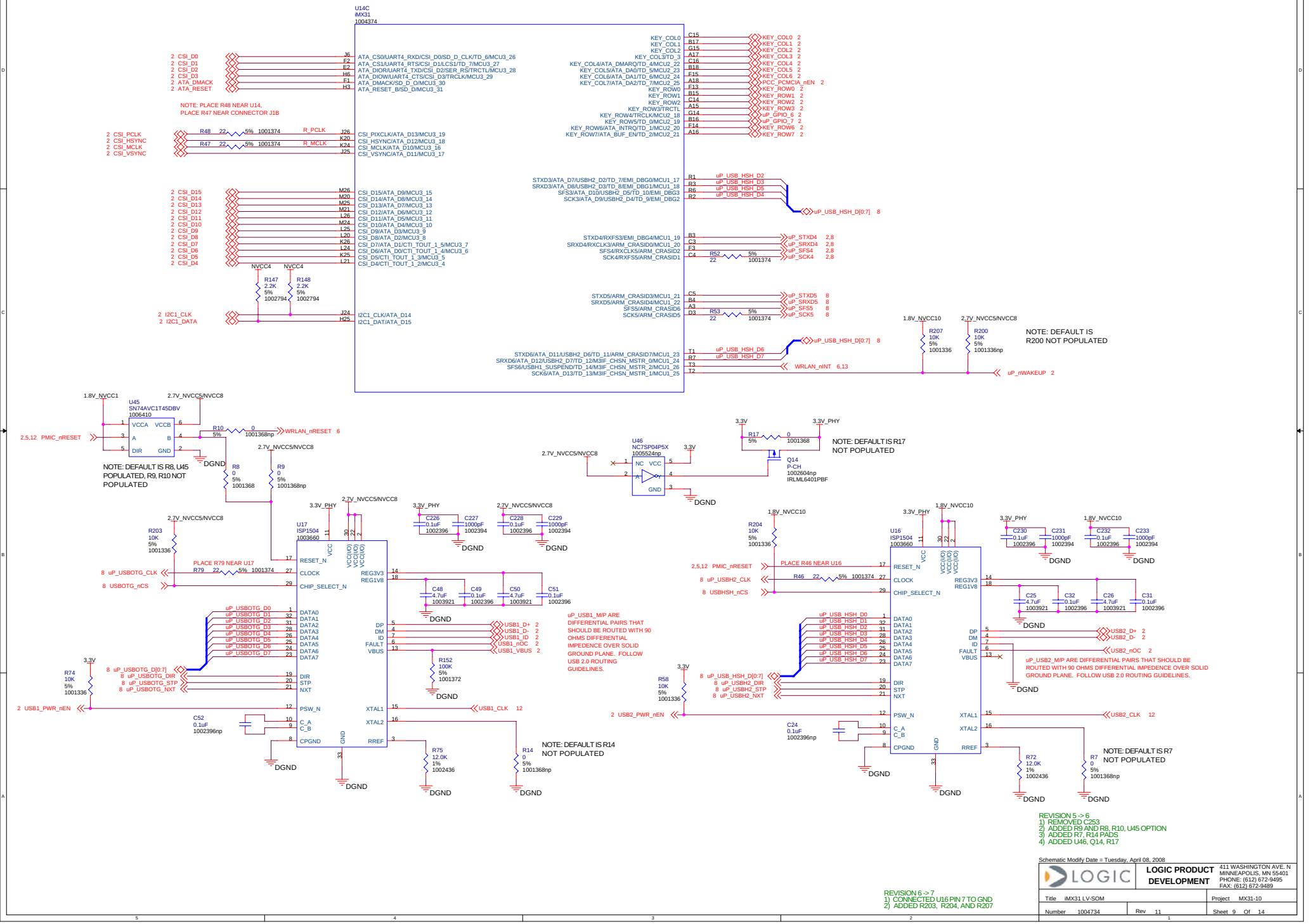
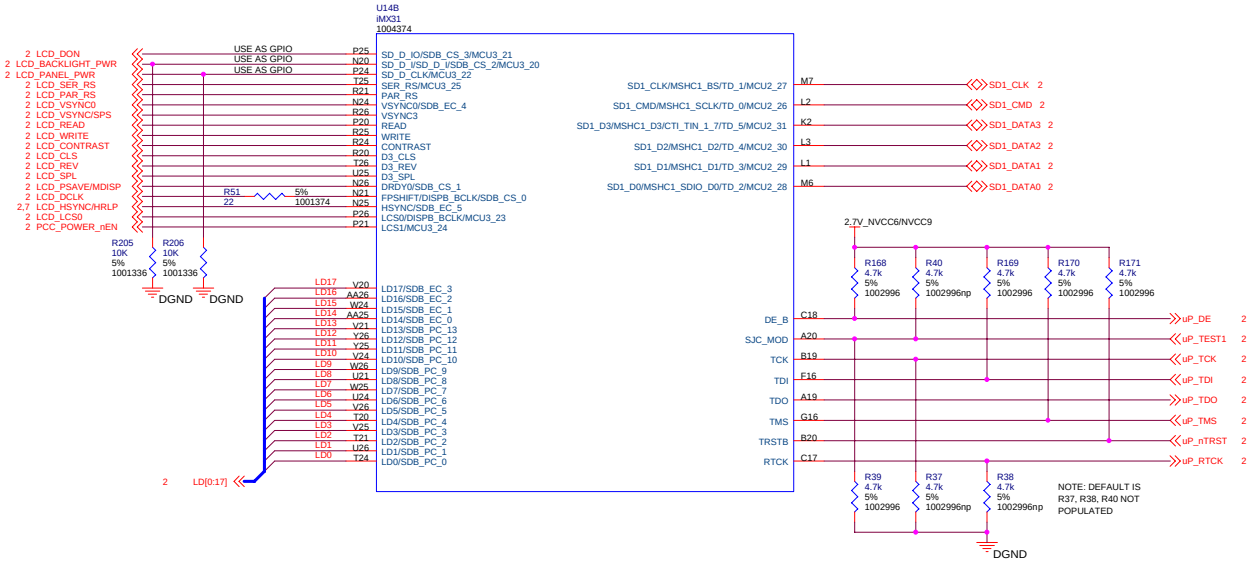
08 - MX31/UARTS/CODEC



09 - MX31/CSI/KEYPAD/USB PHYS



10 - MX31/LCD/JTAG/SD1



REVISION 6 -> 7
1) ADDED R205 AND R206 TO DISABLE LCD BACKLIGHT AT POWER ON.

REVISION 5 -> 6
1) CHANGED LCD_LCS1 TO PCC_POWER_nEN

REVISION 3 -> 4
1) CHANGED LCD_CONTACT TO LCD_CONTRAST

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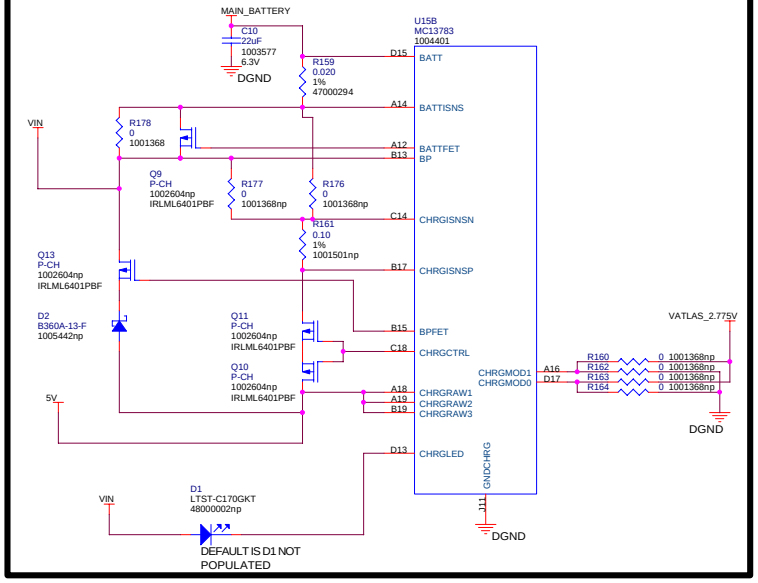
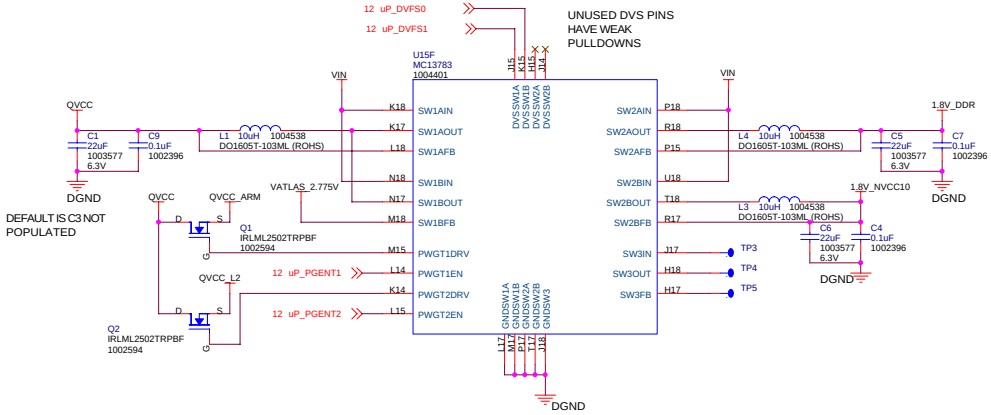
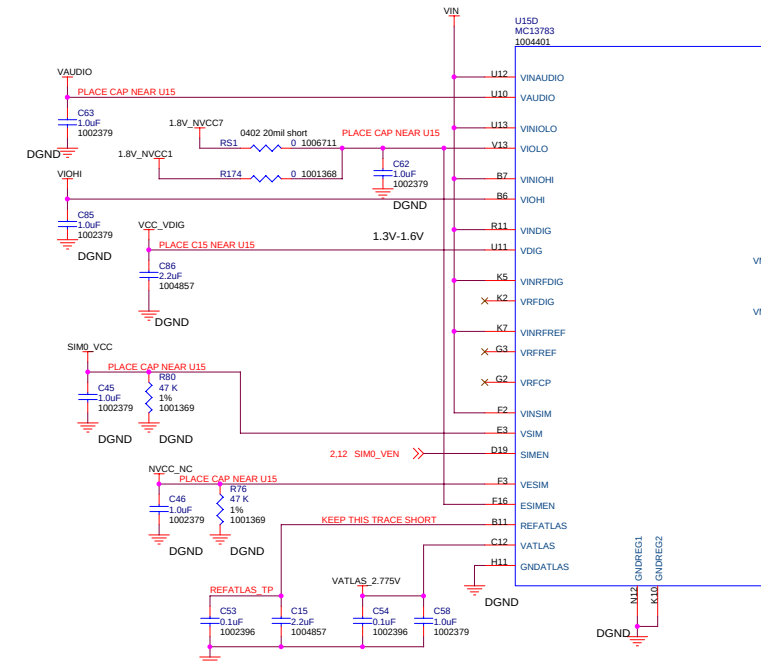
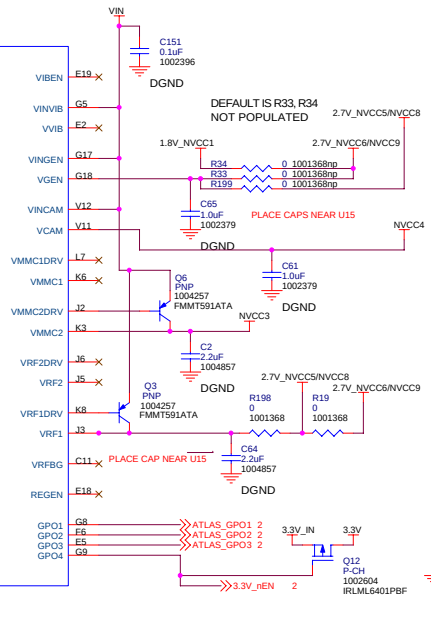
11 - MX31/ATLAS POWER

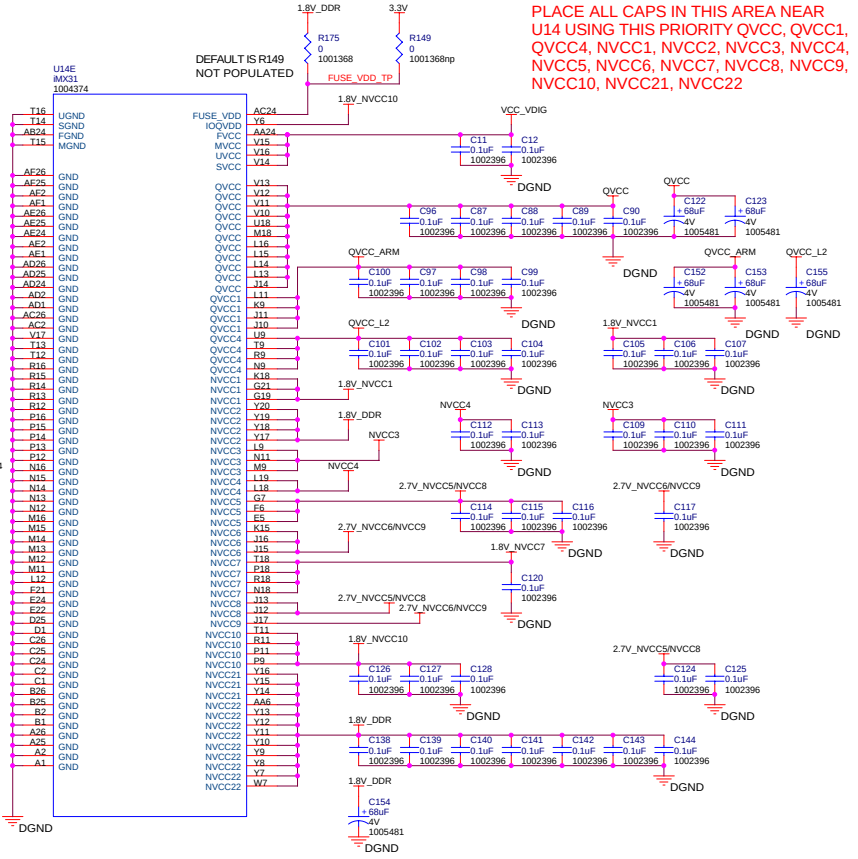
CHARGING OPTIONS	POPULATE
DUAL PATH CHARGING	Q9, Q10, Q11, Q13, D2, R161, R176, R159, C10, R164
SERIAL PATH CHARGING	Q10, Q11, R161, Q9, R159, C10, R177, R163
SINGLE PATH CHARGING	Q10, Q11, R161, R159, C10, R177, R178
NO CHARGE CIRCUIT (DEFAULT)	R159, R178, C10











REVISION 4 -> 5
1) REMOVED uP_DVFS0 CONNECTION TO DVSSW2A AND CONNECTED uP_DVFS0 TO DVSSW1B INSTEAD

REVISION 3 -> 4
1) R173 NO POPULATE
2) ADDED R2

REVISION 5 -> 6
1) REMOVED R173, R2, R30
2) ADDED Q6, C2
3) REMOVED C149, C150, C8, C3
4) REPLACED R29 WITH RS1
5) CHANGED NVCC9 TO NVCC_NC – IT IS NOT CONNECTED TO THE CPU

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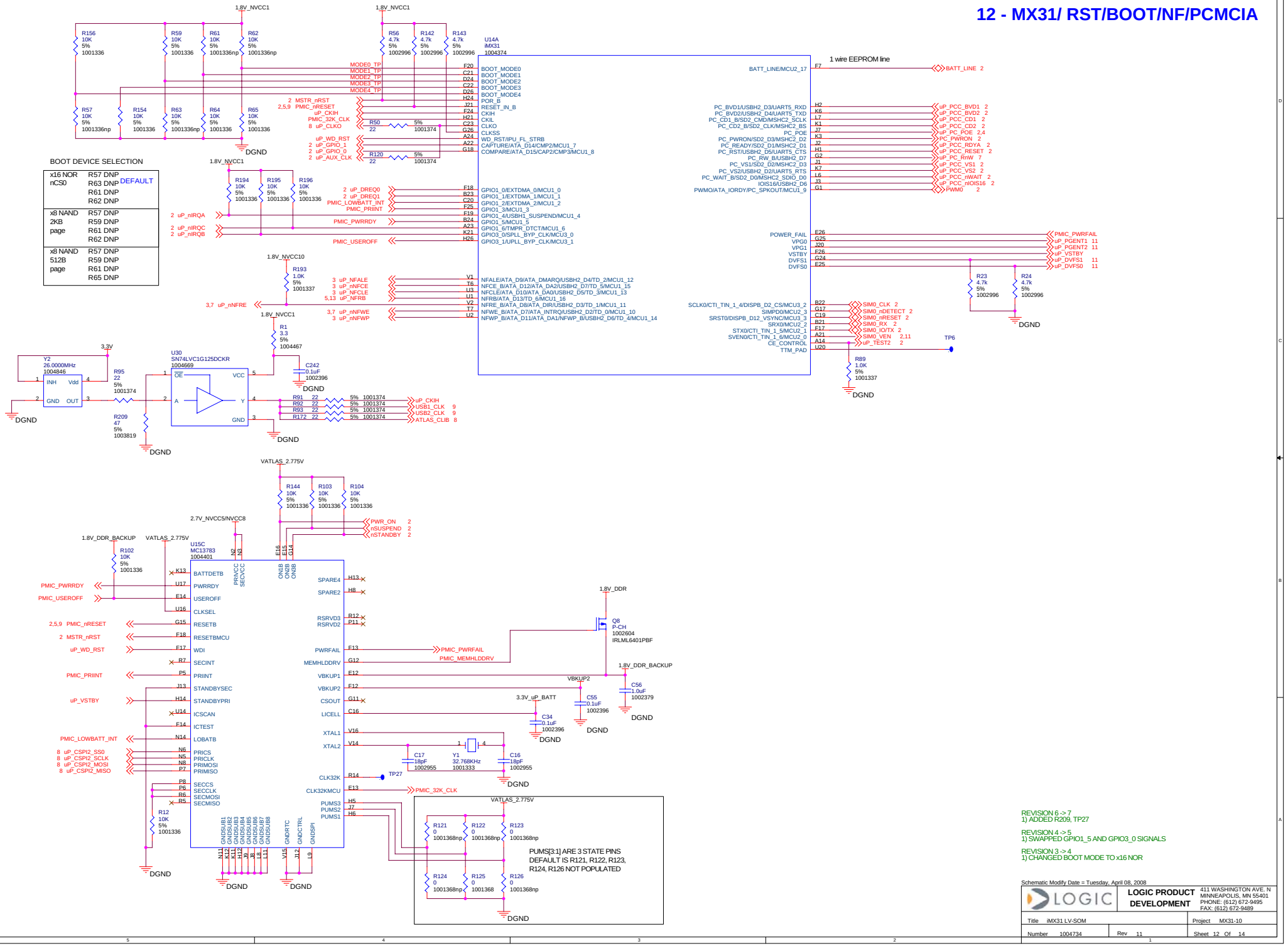
12 - MX31/ RST/BOOT/NF/PCMCIA



REVISION 6 -> 7
1) ADDED R209, TP27

REVISION 4 -> 5
1) SWAPPED GPIO1_5 AND GPIO3_0 SIGNALS

REVISION 3 -> 4
1) CHANGED BOOT MODE TO x16 NOR

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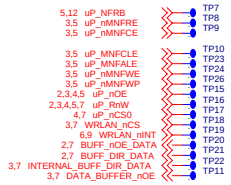
13 - TESTPOINTS

THESE NETS SHOULD HAVE TEST POINTS ON BOTH SIDES OF THE BOARD FOR DEVELOPMENT PURPOSES.



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14 - ECO LIST

Revision Control			
ECO Number	Rev	Description of Change	Date
	1	Initial schematic	02/14/2006
C02687	2	Design review feedback updates complete	03/06/2006
C02705	3	Shifted onboard address lines up 1 bit.	06/19/2006
C02839	4	Changes for Beta spin	08/08/2006
		LCD_CONTRAST signal correction.	
		Added R2 for NVCC4 separation.	
		Changed U8 to 512Mb NAND flash.	
		Changed from active high to active low single bit buffers for U32, U33.	
		Dropped support CF_nCE signal	
		Added external NOR boot option	
		Changed U35 pin 12 input from uP_nNFRE to uP_nNFWE	
		Changed to A23 for address control line for different memory areas	
		Changed U35 pin 13 to uP_RnW	
		Changed LCD_CONTACT to LCD_CONTRAST	
		Changed PCC_nIOWR and CF_nOE to uP_nOE	
		Added BOOT_nCS and EXT_BOOT_nSELECT	
C02947	5	Changes for Beta Build 2 spin	09/15/2006
		Added R201 and R202	
		Changed OE on U32 and U33 to be controlled by uP_PC_POE	
		Removed uP_DVFS0 connection to DVSSW2A and connected uP_DVFS0 to DVSSW1B instead	
		Swapped GPIO1_5 and GPIO3_0 signals	
		Changed LCD interface: LD0-5 --> B0-5; LD12-17 --> R0-5	
C03377	6	Changes for Pilot	12/12/2006
		ADDED U43, REMOVED C253	
		REMOVED C253, C254, C200, C202, C204, C206, C208-210.	
		REPLACED R127 WITH RS3, R128 WITH RS4	
		CHANGED LCD_LCS1 TO PCC_POWER_nEN	
		ADDED U42, Q6, C2, REMOVED R173, R2, R30, C149, C150, C8, C3, C251,	
		REPLACED R29 WITH RS1, R35 WITH RS2	
		CHANGED LCD_LCS1 TO PCC_POWER_nEN	
		CHANGED NVCC9 TO NVCC_NC	
		ADDED PCC_POWER_nEN ON J2 PIN 13 ADDED PCC_PCMCIA_nEN ON J2 PIN 15	
		ADDED U46, Q14, R17, R15, R16FOR USB PHY POWER CONTROL	
C03377	7	Changes for Production	06/04/2007
		CONNECTED U16 PIN 7 TO GND	
		ADDED R203, R204, R205, R206, R207, R208, R209	

Production Changes v7 - v8 ECO C04175		
Mantis #	Pages	Description
0003232	9	If the IMX31 system is reset while there is an active ActiveSync connection, the connected host PC will not realize that the IMX31 system was reset. Therefore, it will not show as disconnected. This is because the USBF phy chip is only reset at power up but not at system reset. From this state, the only way to get connected again is by a power cycle to the IMX31 system. Soft resetting the phy in that state does not help. Changed default population to populate U45 and R8 and not pop R9.
0003462	11	The BJT's Q3 and Q6 have been implemented backwards. This results in the device operating in the reverse active mode. From Jeno's analysis no device degradation will occur provided the die temp remains in spec, however the gain will be much less and the current provided through the device will be limited. In addition the ref cap C15 needs to be populated. Jeno found during his analysis of the BJT issue that a start up condition exists in that boards will not start up if the voltage level of the the MAIN_BAT input was lowered to about 3.1V. When C15 was populated with at least a 1.0uF capacitor the issue went away and the input voltage could be lowered to the 2.7V min as required. Fixed BJT's Q3 and Q6, populated C15.

Production Changes v8 - v11 ECO C04737		
Mantis #	Pages	Description
		This revision step has been done to sync up the correct revision of the schematic with the associated PCB. Revision 9 and 10 were done for a specific application, but in the Agile CM system all assemblies use the latest revision of the underlying parts. Therefore assemblies built using the PCB designed off of schematic revision 8 show schematic revision 10 on their BOMs. This revision step rolls back the changes addressed in version 9 and 10 of the schematic and ups the revision to version 11. This will maintain the history of this action, and the Agile CM system will then bump the revision of the schematic automatically and the proper set of schematics will then match all of the released assemblies. The single assembly done for a specific customer that uses schematic revision 10, will be addressed by assigning a new schematic part number to capture these changes. This will differentiate it from all other previous revisions of the schematic in the CM system. Moving forward all new releases of the schematic document will warrant the assigning of a new schematic part number.

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MINNEAPOLIS, MN 55401
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