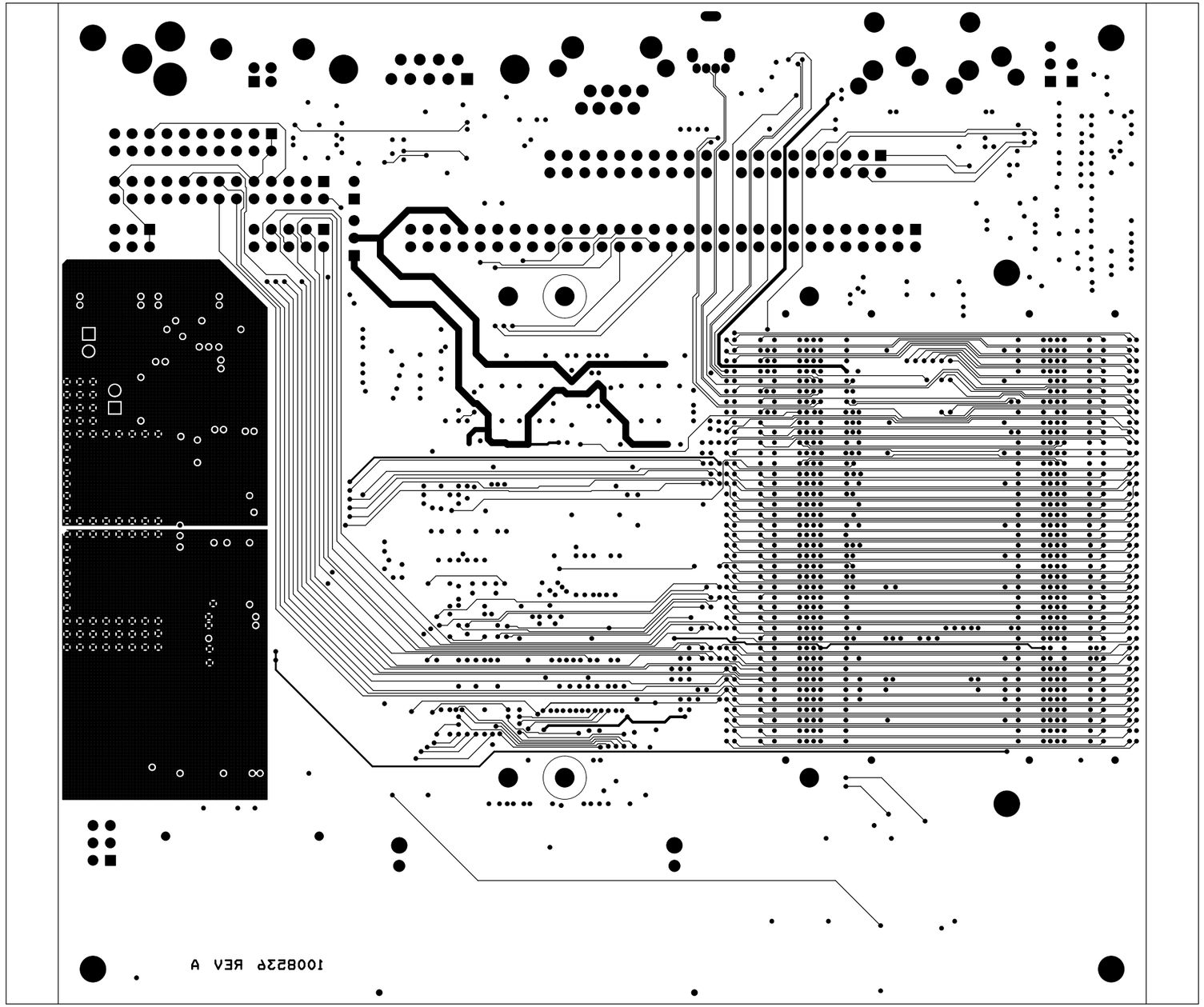
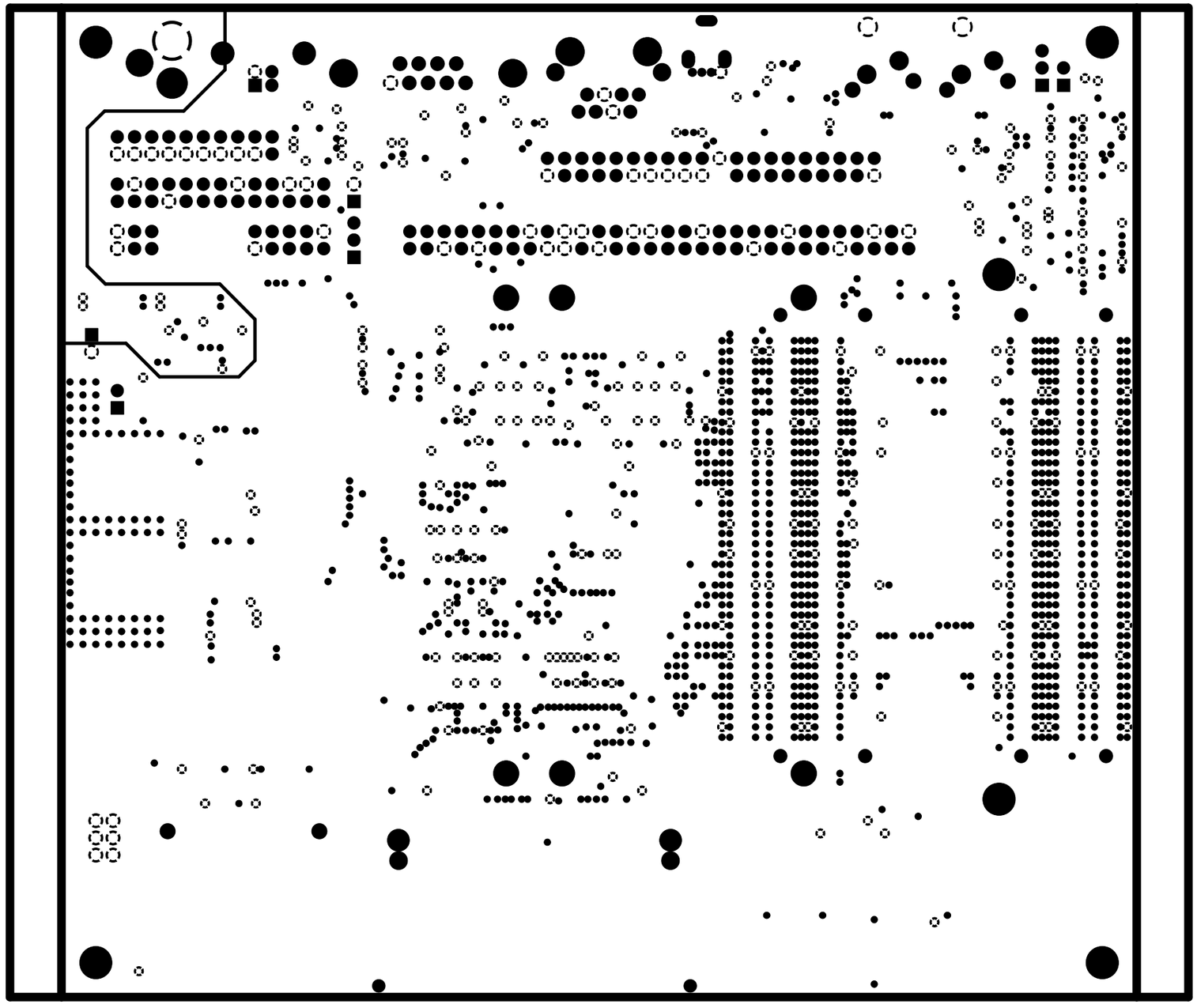
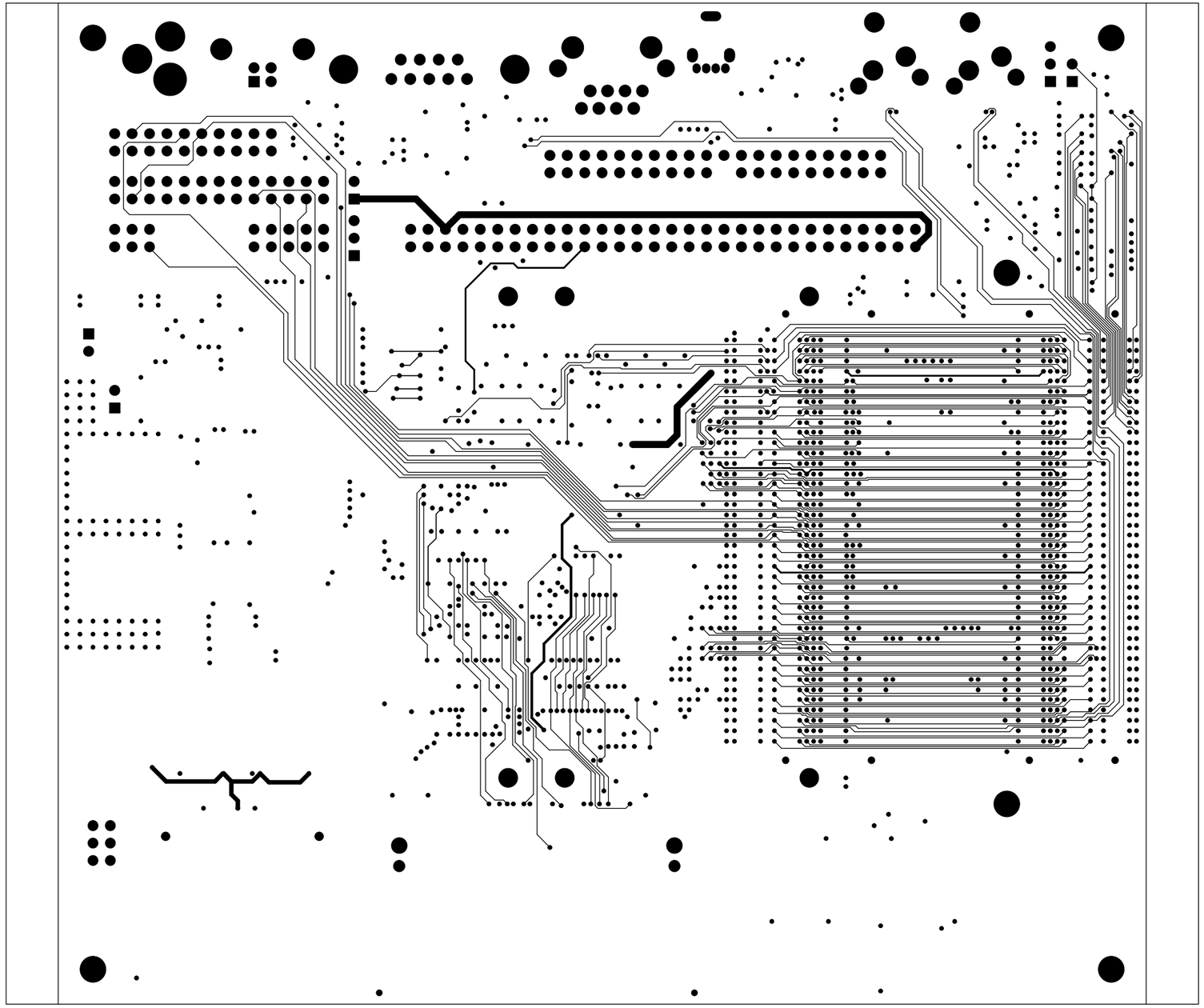


LOGIC PRODUCT DEVELOPMENT

LAYER 6 BOTTOM

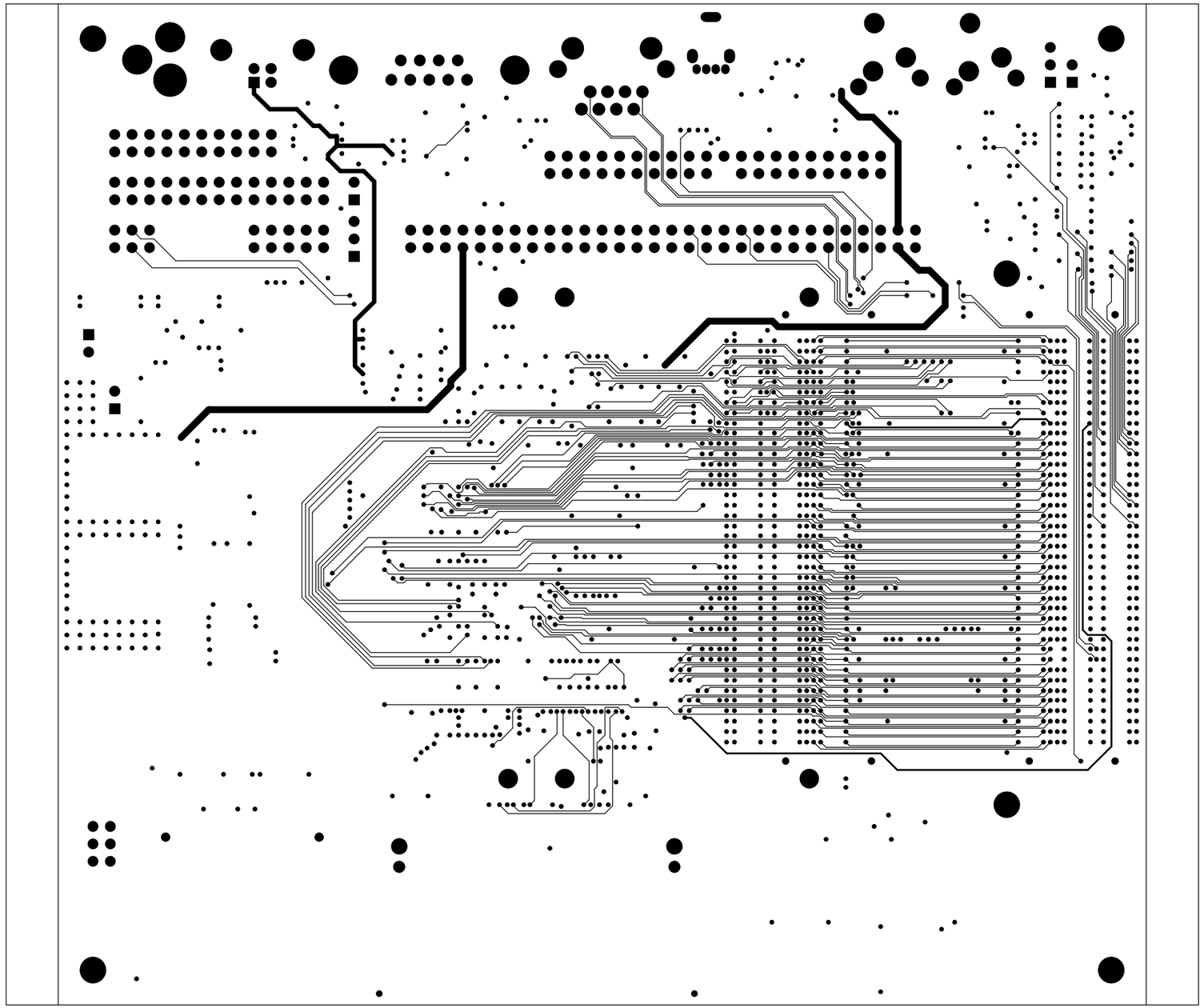


LOGIC PRODUCT DEVELOPMENT
LAYER 2 GND



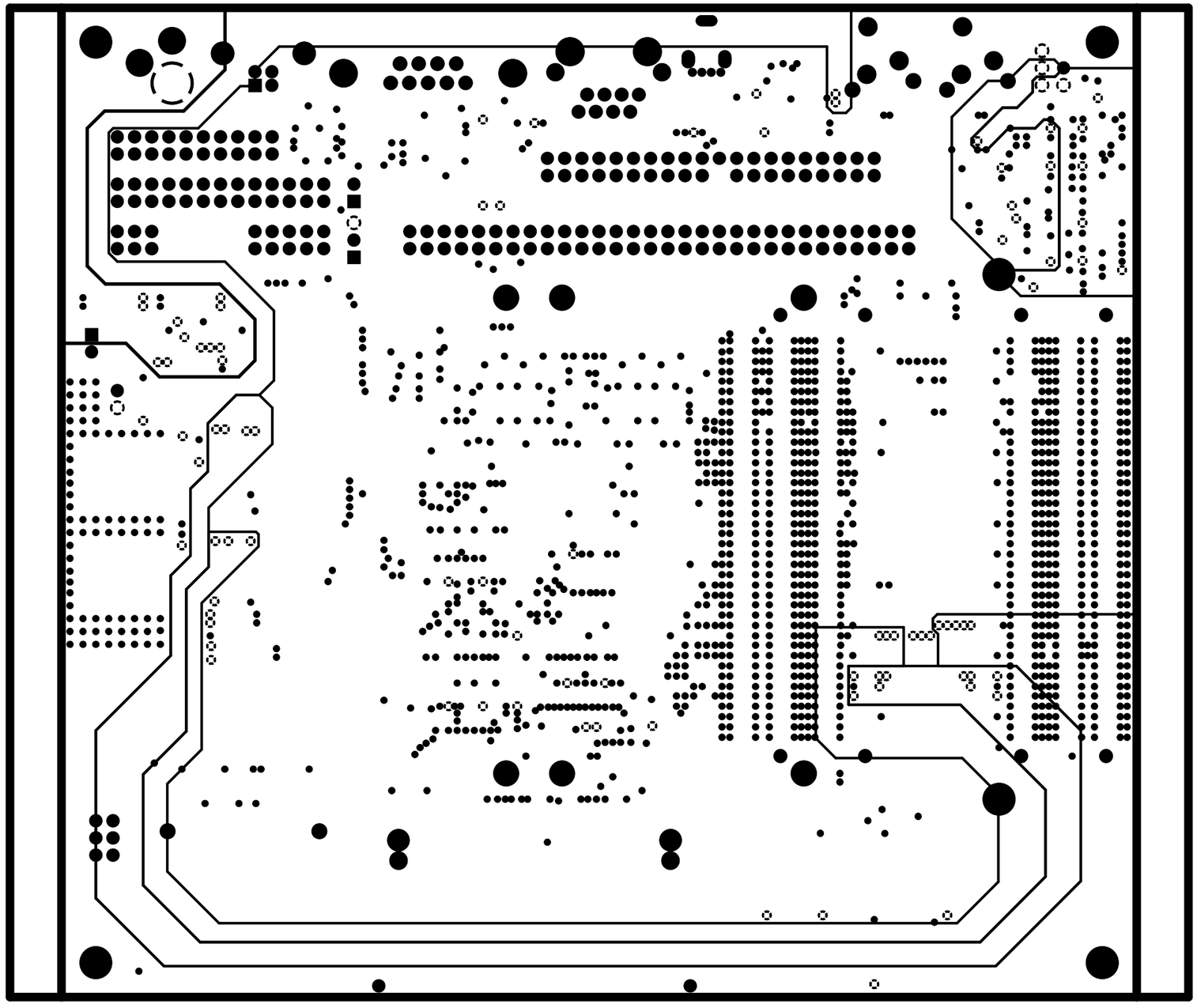
LOGIC PRODUCT DEVELOPMENT

LAYER 3



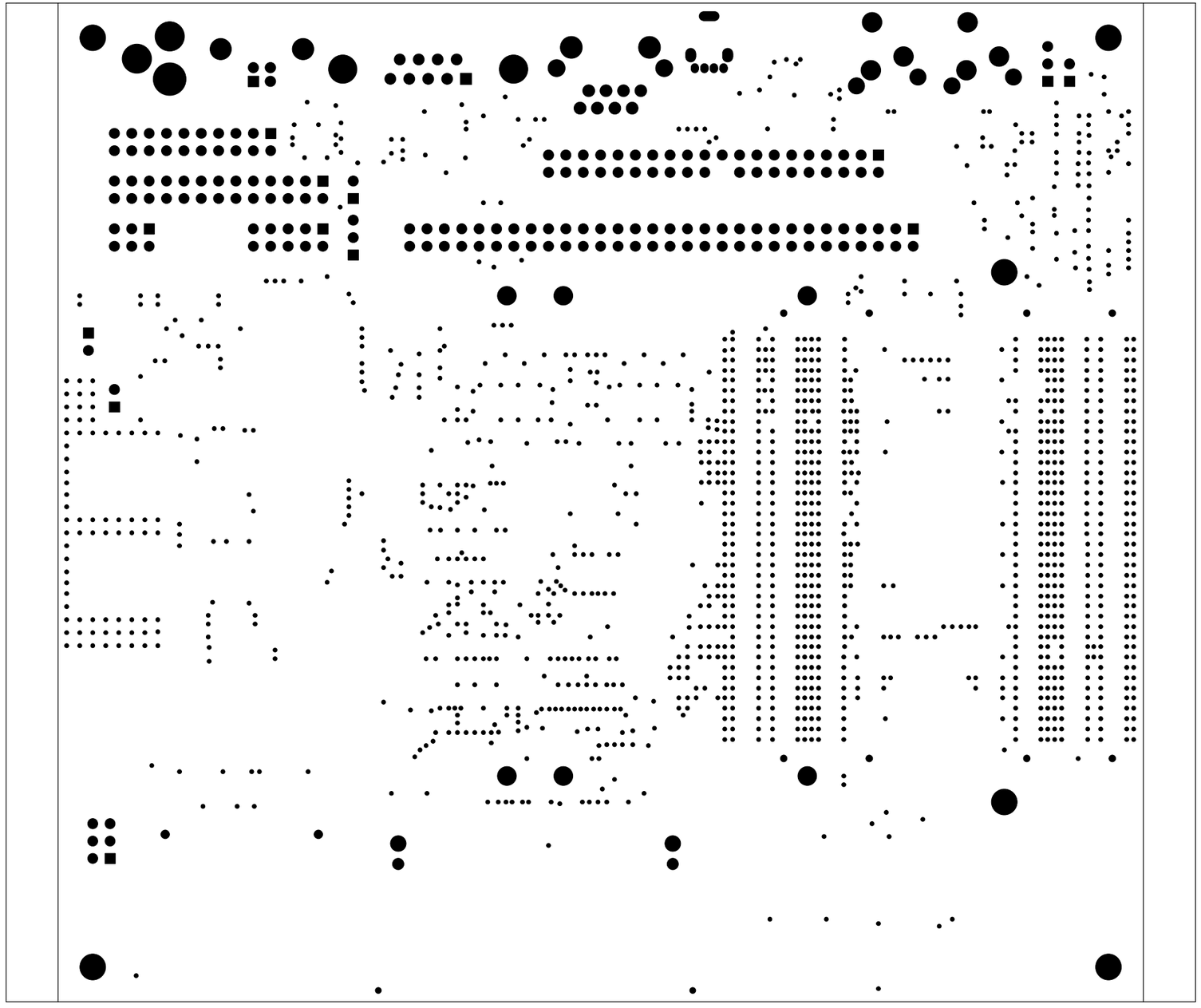
LOGIC PRODUCT DEVELOPMENT

LAYER 4



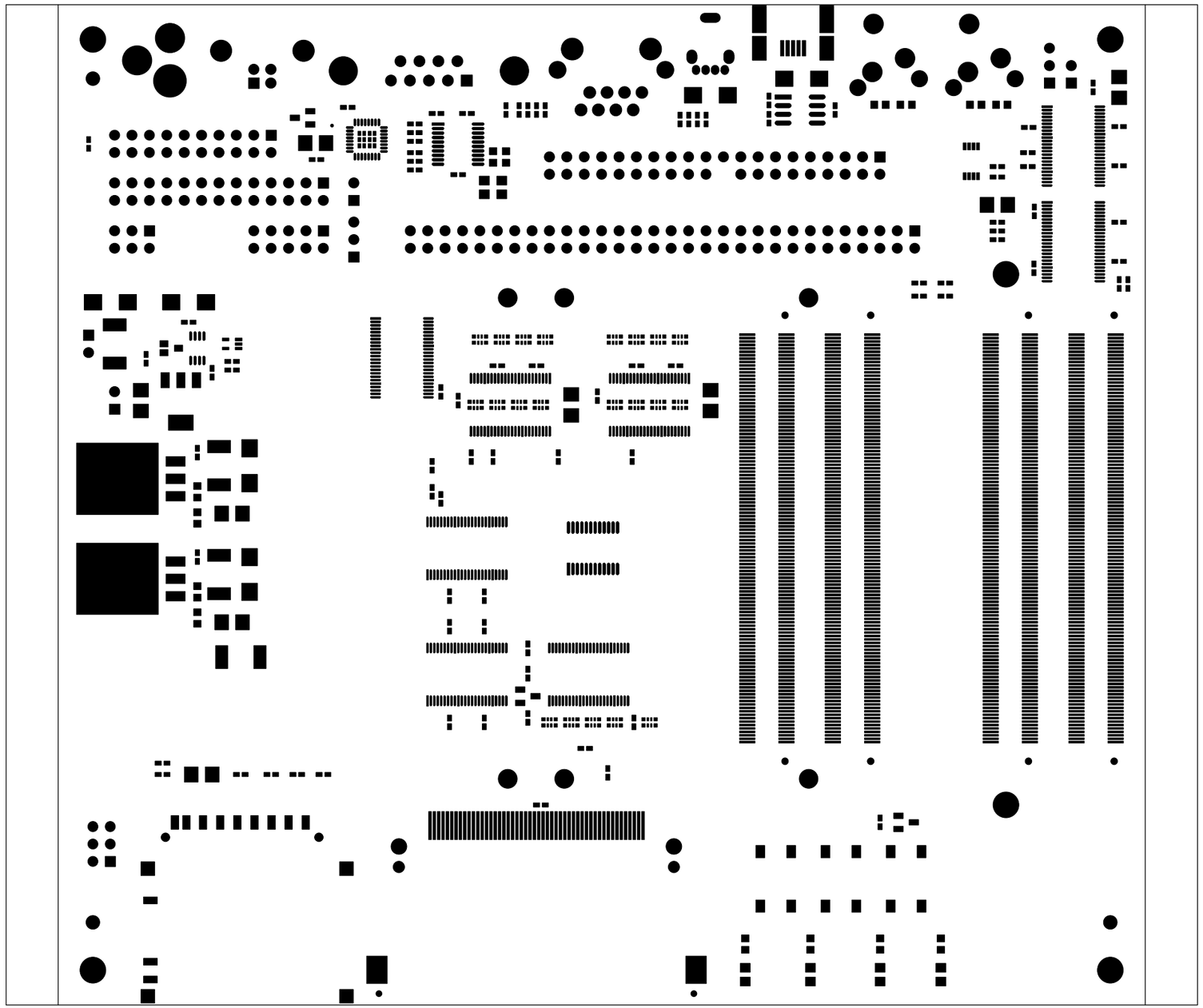
LOGIC PRODUCT DEVELOPMENT

LAYER 5 PWR



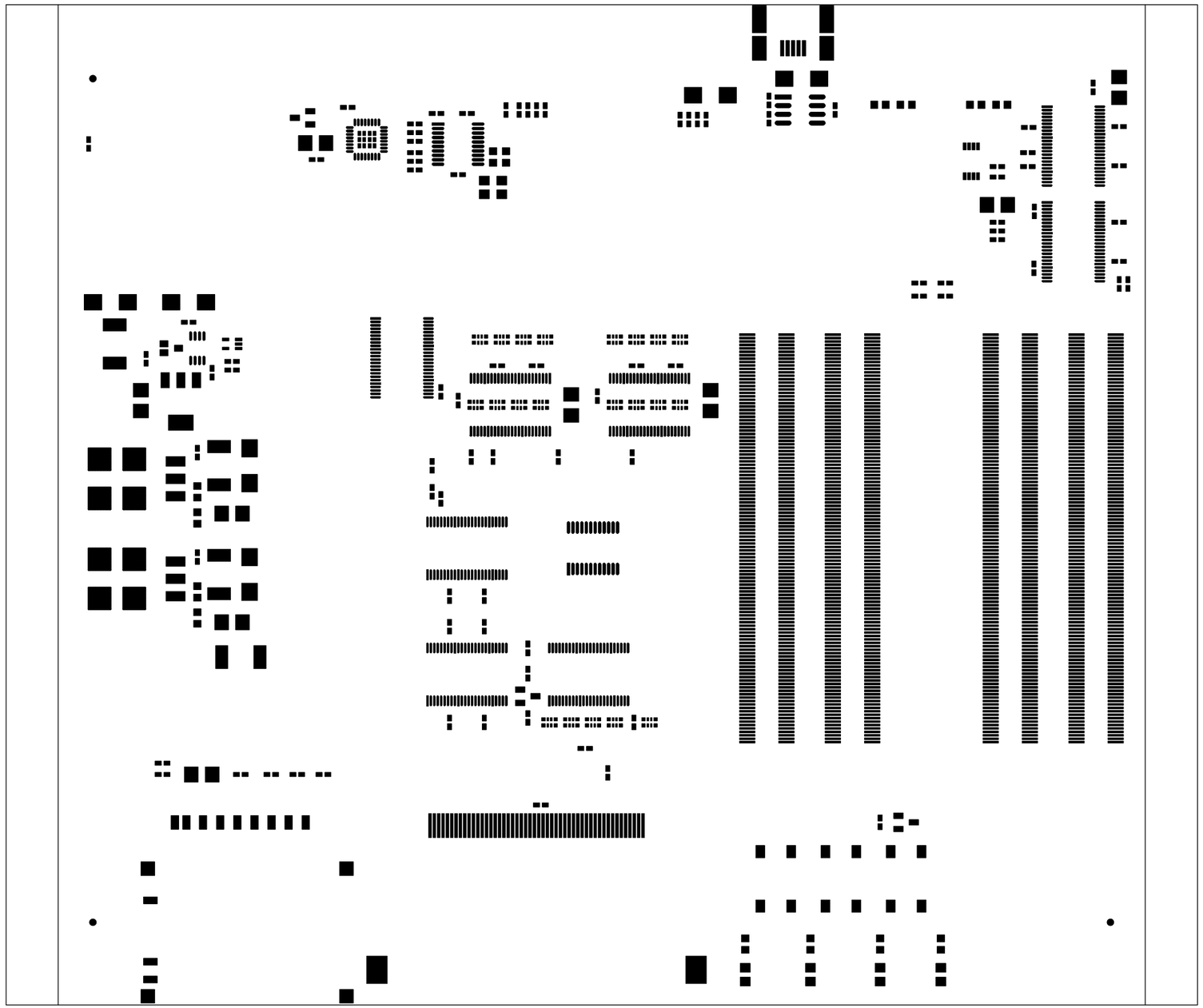
LOGIC PRODUCT DEVELOPMENT

SOLDERMASK BOT



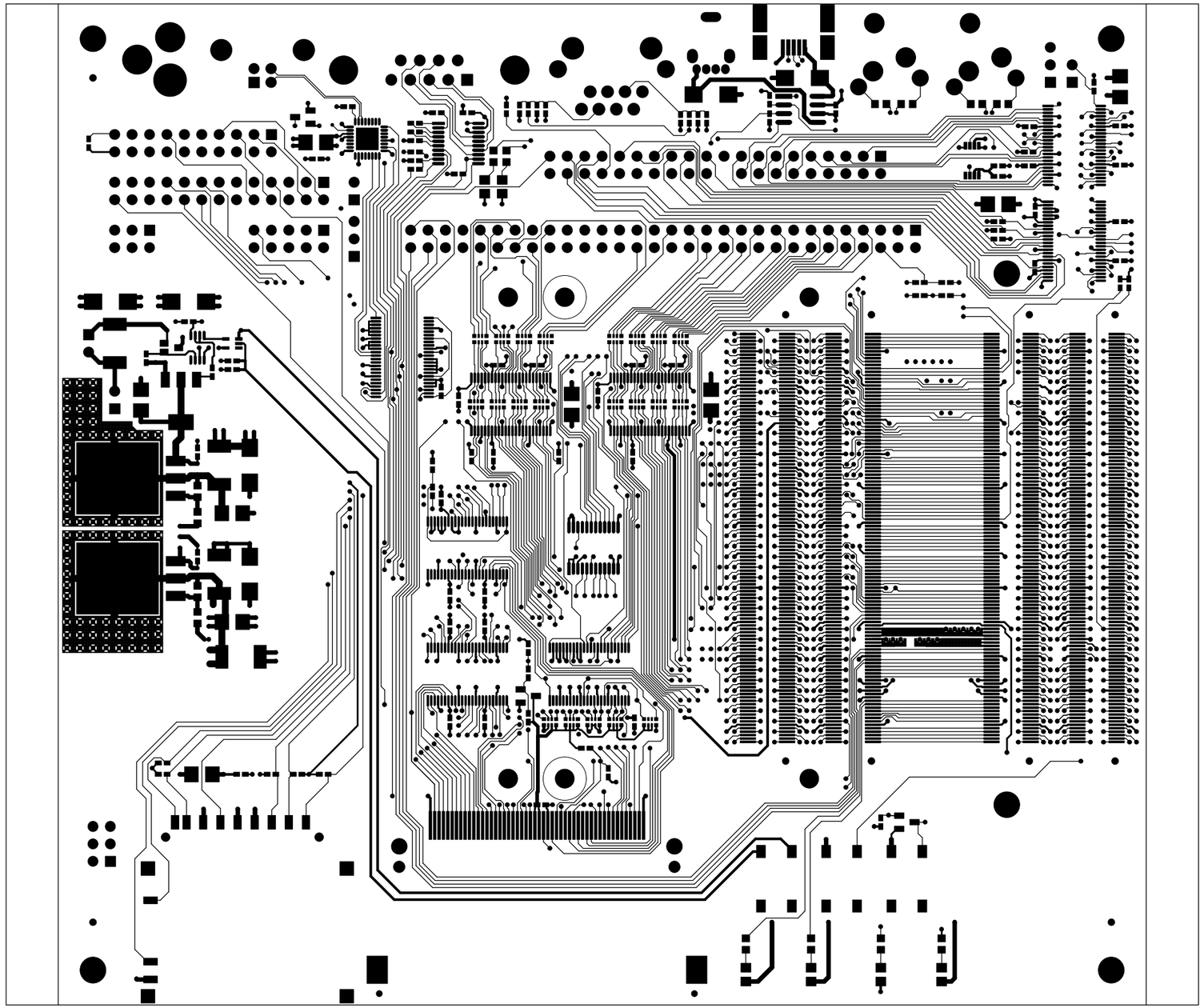
LOGIC PRODUCT DEVELOPMENT

SOLDERMASK TOP

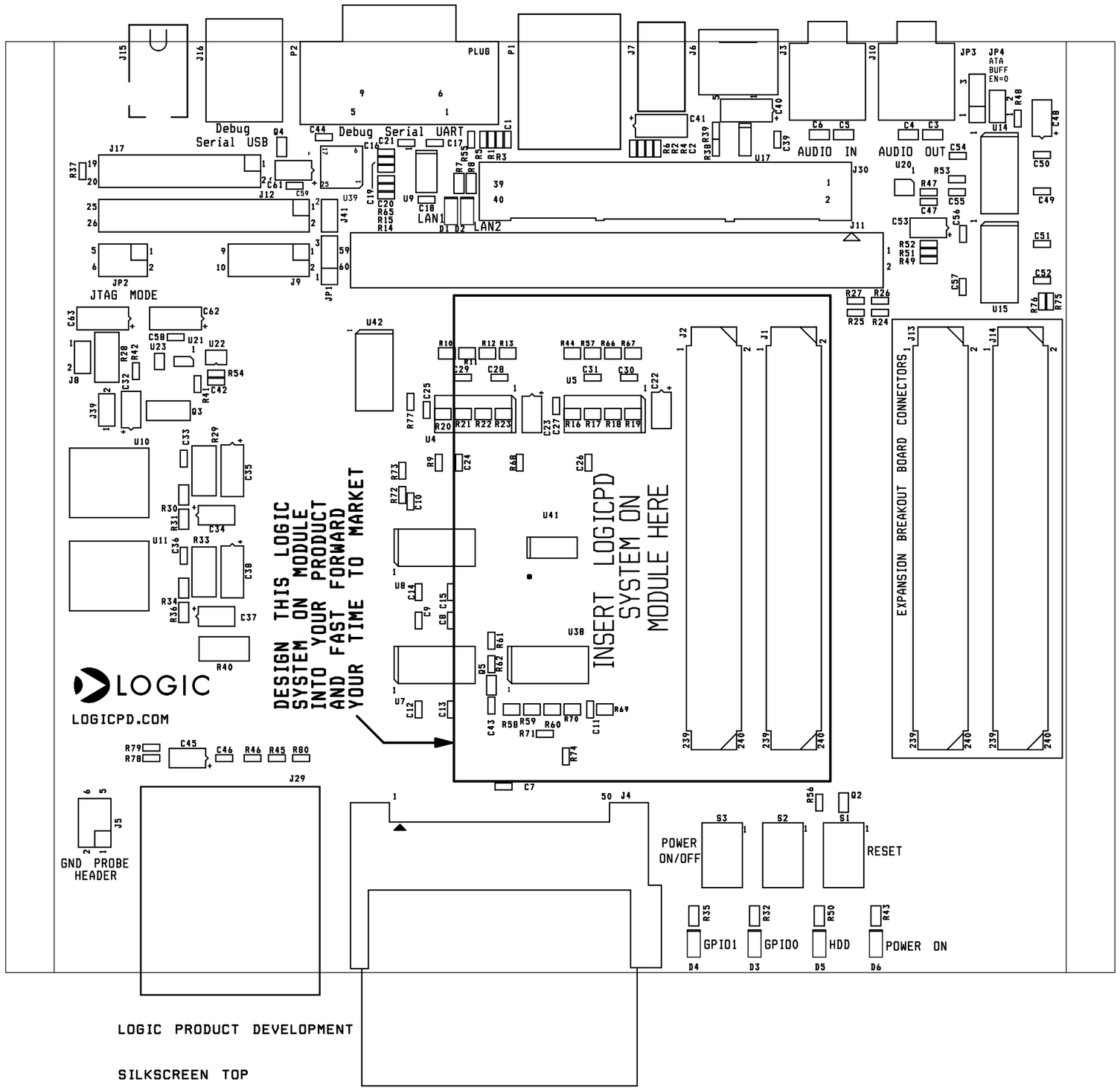


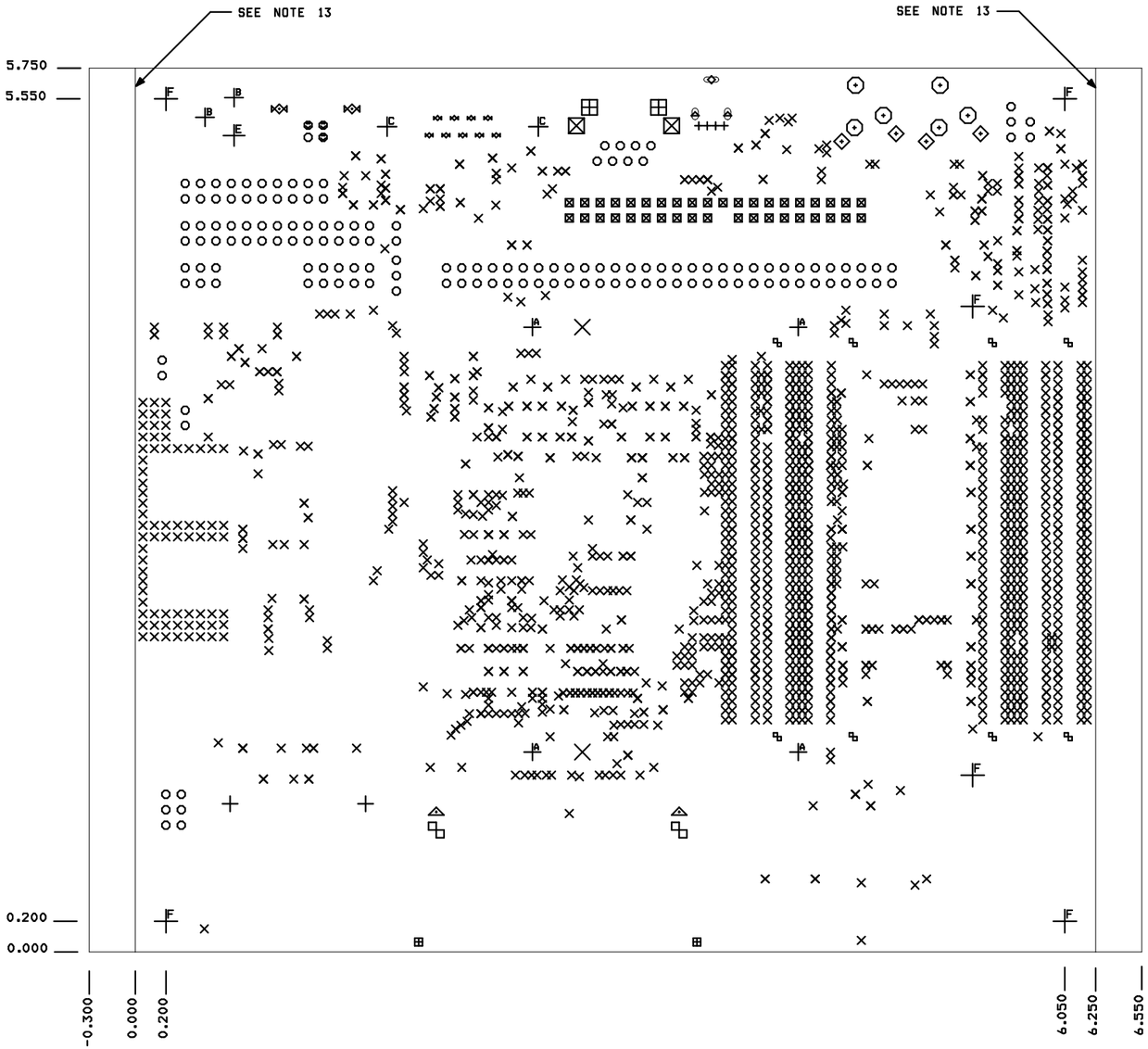
LOGIC PRODUCT DEVELOPMENT

SOLDERPASTE TOP



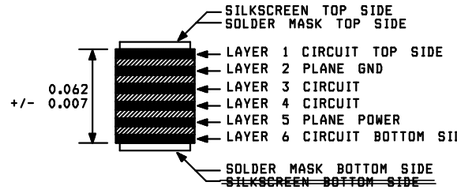
LOGIC PRODUCT DEVELOPMENT
LAYER 1 TOP


Debug Serial USB
Debug Serial UART
PLUG
AUDIO IN
AUDIO OUT
JTAG MODE
LAN1
LAN2
JP3
JP4
ATA BUFF EN=0
DESIGN THIS LOGIC SYSTEM ON MODULE INTO YOUR PRODUCT AND FAST FORWARD YOUR TIME TO MARKET
INSERT LOGICPD SYSTEM ON MODULE HERE
EXPANSION BREAKOUT BOARD CONNECTORS
LOGIC
LOGICPD.COM
GND PROBE HEADER
POWER ON/OFF
RESET
GPIO1
GPIO0
HDD
POWER ON
LOGIC PRODUCT DEVELOPMENT
SILKSCREEN TOP



NOTE:

1. MATERIAL SELECTION:
   6 LAYER. EPOXY GLASS, NEMA GRADE FR-4, 0.062 +/- 0.007 THICK.
   THE PRINTED CIRCUIT BOARDS MANUFACTURED TO THIS DRAWING MUST BE RoHS COMPLIANT.
   COPPER THICKNESS ON ALL LAYERS TO BE 1/2 OUNCE (NOMINAL).
2. FINISH ON ALL SOLDERABLE SURFACES TO BE:
   ImAg (Immersion Silver).
3. SOLDER RESIST: - BLUE (COLOR MUST BE APPROVED BY LOGIC PRIOR TO USE).
   THE USE OF SOLDER RESIST COATING SHALL BE IN ACCORDANCE WITH
   THE REQUIREMENTS OF IPC-SM-840.
   ALL SOLDERABLE SURFACES ARE TO BE FREE OF SOLDER RESIST.
   USE LIQUID PHOTOIMAGEABLE RESIST APPLIED OVER BARE COPPER.
4. SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND
   TESTPOINT LANDS ARE TO BE FREE OF INK.
5. MANUFACTURER'S IDENTIFICATION: ADD TO SILKSCREEN BOTTOM SIDE.
6. ELECTRICAL BARE BOARD TEST REQUIRED.
7. DRILL SIZES ARE FINISHED SIZE AFTER PLATING.
8. BOARD VENDOR MAY REMOVE THERMALS FRO VIA'S ON PLANE LAYERS.
9. BOARD VENDOR MAY REMOVE NON FUNCTIONAL PADS ON INNER LAYERS.
10. BOARD VENDOR MAY ADD TEAR SHAPING TO INNER LAYERS.
    BOARD VENDOR TO ADD TEAR SHAPING TO OUTER LAYERS.
11. THEIVING STRUCTURES MAY BE ADDED TO COMPENSATE FOR VARIATIONS
    IN COPPER DENSITIES ACROSS THE PWB. SPACING BETWEEN THEIVING AND
    CONDUCTIVE PATTERN TO BE 20MILS MINIMUM.
12. WIDTH OF TRACES ON SIGNAL LAYERS MAY BE ADJUSTED AS NECESSARY
    TO ACHIEVE THE IMPEDANCE SPECIFIED.
    90 OHM +/-10% DIFFERENTIAL IMPEDANCE CALCULATED WITH .0049 TRACE.
    100 OHM +/-10% DIFFERENTIAL IMPEDANCE CALCULATED WITH .0045 TRACE.
13. BOARD TO BE SCORED AT DESIGNATED LINE. SCORING TO BE 30 DEG.
    AND A MINIMUM OF 0.015 INCHES BOARD MATERIAL IN CHANNEL.
14. UNLESS OTHERWISE NOTED USED IPC-6012B CLASS 2.



6 LAYER STACK-UP

DRILL CHART

SYM	DIAM	TOL	QTY	NOTE
×	0.012	+/-.003	1487	PLATED
+	0.032	+/-.003	4	PLATED
◇	0.096x0.033	+/-.003	1	PLATED SLOT
⊠	0.035	+/-.003	39	PLATED
⊞	0.035	+/-.003	2	NON-PLATED
⊜	0.036	+/-.003	3	PLATED
○	0.040	+/-.003	151	PLATED
⧉	0.040	+/-.003	8	NON-PLATED
⧋	0.075x0.041	+/-.003	2	PLATED SLOT
⋈	0.043	+/-.003	9	PLATED
┼	0.051	+/-.003	2	NON-PLATED
⊙	0.052	+/-.003	4	PLATED
⊠	0.064	+/-.003	2	PLATED
⧉	0.067	+/-.003	2	NON-PLATED
⊙	0.072	+/-.003	6	PLATED
⧋	0.091	+/-.003	2	NON-PLATED
⋈	0.091	+/-.003	2	PLATED
┼A	0.110	+/-.003	4	PLATED
╳	0.110	+/-.003	2	NON-PLATED
┼B	0.120	+/-.003	2	PLATED
┼C	0.125	+/-.003	2	PLATED
⊞	0.128	+/-.003	2	NON-PLATED
┼E	0.140	+/-.003	1	PLATED
┼F	0.150	+/-.003	6	NON-PLATED
TOTAL			1745	

REVISION CHANGES

PART NO.	REV	DATE	CHANGES
1007028	A	02-07-2007	R75-R76 ADDED
1008536	A	10-02-2007	SEE BELOW

1. ADDED U42,C62,C63,R77-R80