



GS2985

Design Guide

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Overview

Together with the GS2985 Evaluation Board (EB-GS2985-S) and the GS2985 Data Sheet, this document serves as a reference for designing with the GS2985, a Gennum multi-rate serial digital reclocker. This document contains two main areas of focus:

1. Considerations in the schematic design.
2. Recommended PCB layout practices when designing with the GS2985.

The figure below shows a typical GS2985 application block diagram.

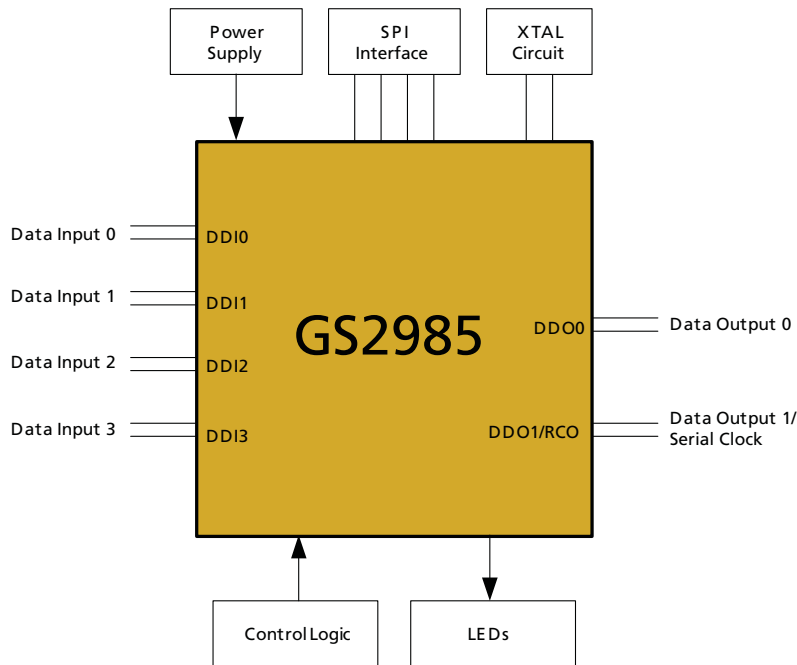


Figure A: Typical Application of the GS2985

1. Power

1.1 Power Supply

The GS2985 requires a single power supply at 3.3V or 2.5V.

The following guidelines are recommended when designing the power for the GS2985:

- Use coupled power and ground planes i.e. use minimum spacing between power and ground planes. Power and ground planes form a natural capacitor, which will increase capacitance
- Do not overlap power planes. If it is unavoidable, different power planes should be isolated from each other with a ground plane between them
- Power and ground planes should be placed near the component side, which will reduce inductance of vias

- Bulk supply decoupling capacitors of $10\mu\text{F}$ and 100nF are recommended to filter-out high frequency noise
- It is recommended to decouple each power supply pin individually with a 10nF capacitor. All decoupling capacitors should be placed as close as possible to the power and ground pin pairs of the GS2985. Please see Figure 1-1 below. Wherever possible, use two vias for each VCC and GND pin and flood the copper area

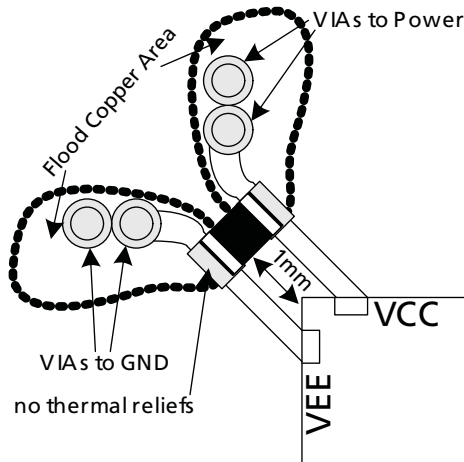


Figure 1-1: Local Decoupling of the GS2985

- Central paddle should be connected to ground with multiple vias for proper thermal dissipation. At least 36 vias are recommended

1.2 VCO Decoupling

For performance reasons, it is particularly important to maintain low noise on the VCO power supply. It is recommended to connect VCC_VCO to either the 2.5V or the 3.3V power supply through the RC filter shown in Figure 1-2. The RC components should be placed as close as possible to the GS2985, and further away from noise sources. For a 2.5V power supply R should have a value of $422\Omega \pm 1\%$. For a 3.3V power supply, R should have a value of $267\Omega \pm 1\%$.

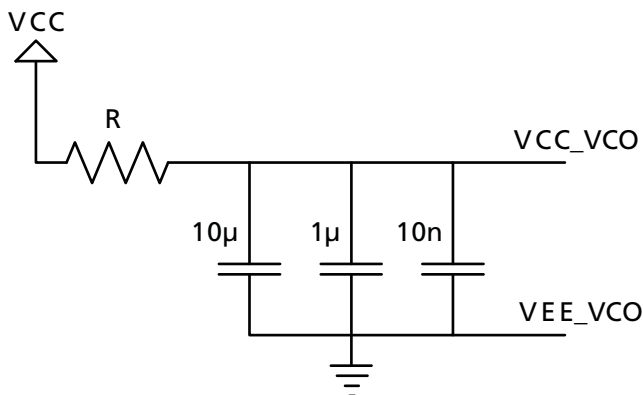


Figure 1-2: VCO Decoupling

2. SDI Input and Output

The SDI inputs and outputs are 100Ω differential signals.

The following guidelines are recommended when designing the transmission lines for the GS2985:

- Trace lengths should be minimized and the differential traces should be closely matched, and curved rather than sharp-angled
- Any discontinuity (ie. impedance transitions) should be avoided on the transmission lines
- No silk-screen is allowed on these traces to ensure an accurate impedance
- PCB trace widths coming out of the GS2985 should be closely matched to SMT component width to minimize reflections due to change in trace impedance
- Non transmission line components should be at a minimum distance of 10x the transmission line width (example: if transmission line is 1mm wide, the closest non transmission line component needs to be at least 10mm away); to eliminate cross-talk, it is recommended that this rule also be followed when routing parallel differential pairs (example: parallel inputs). If board space is of concern, this distance could be decreased to 5x
- If passive components are used on the high-speed transmission lines, then antipads are recommended to deal with transmission line component parasitics. The antipad sizes used on the evaluation board are given in [Figure 2-1](#), [Figure 2-2](#) and [Figure 2-3](#). These antipad sizes are specific to this design, which uses a FR-4 dielectric with a 10mil thickness between the top routing layer and the associated GND layer. NOTE: Antipads are defined as the absence of copper in the underlying GND and PWR plane layers. As well, there should be no routing on any routing layer underneath the antipads

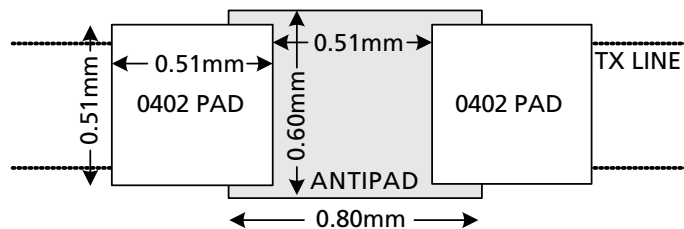


Figure 2-1: Series 0402 Component Antipad optimized for 50Ω traces

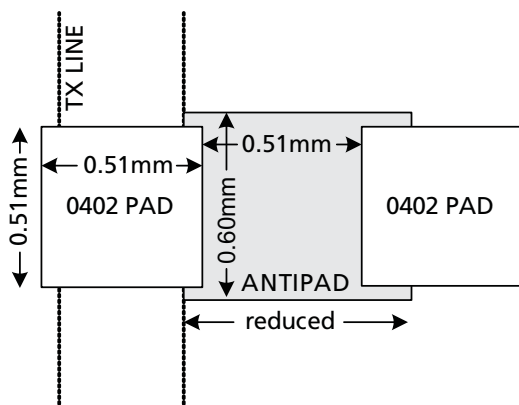


Figure 2-2: Shunt 0402 Component Antipad optimized for 50Ω traces

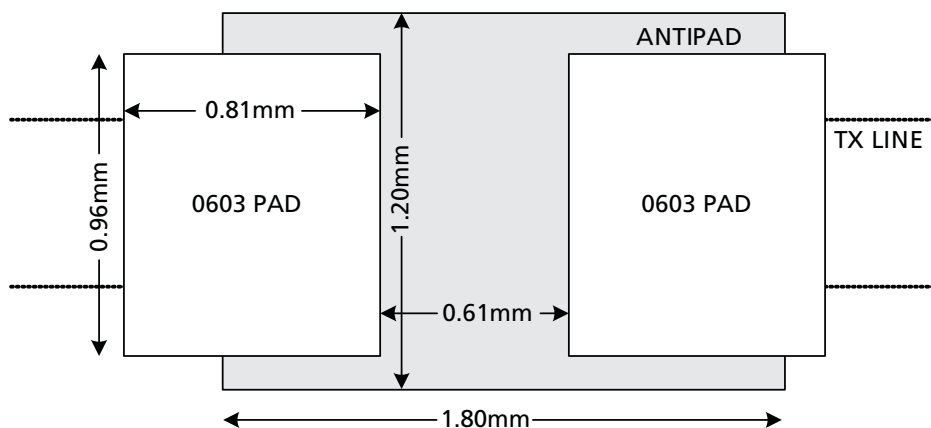


Figure 2-3: Series 0603 Component Antipad optimized for 50Ω traces

3. Crystal Circuit

The GS2985 requires a 27MHz reference clock for correct operation. The crystal recommended by Gennum is CS10-27.000M, and the recommended circuit is shown in Figure 3-1. The circuit will vary depending on the crystal being used. The crystal used on the GS2985 evaluation board has a low frequency tolerance and a load capacitance of 18pF.

NOTE: a high value parallel resistor (ie. $1\text{M}\Omega - 1.5\text{M}\Omega$) is required regardless of what crystal is used as shown in Figure 3-1.

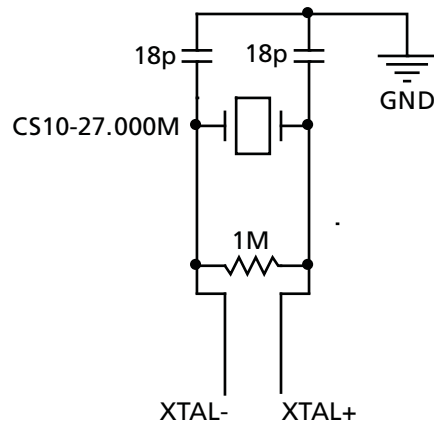


Figure 3-1: Recommended Crystal Circuit

The XTAL_BUF_OUT pin makes cascading multiple reclockers using a single crystal possible.

The following crystal circuit is recommended when operating multiple reclockers using a single crystal:

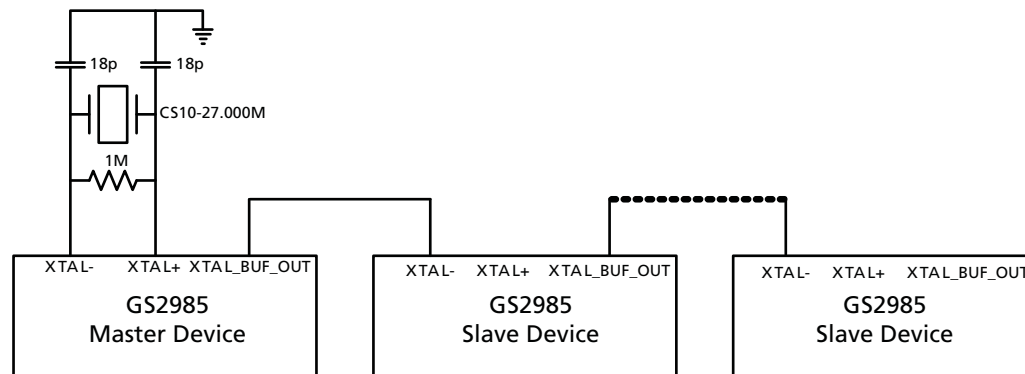


Figure 3-2: Daisy Chain XTAL Configuration

4. External Capacitors

External capacitors are needed for the following pins:

VDD_1P8 (pin 27) - A 220nF external capacitor is needed for the 1.8V digital supply.

LF+ (pin 62) - A 47nF external capacitor is needed for the loop filter.

CP_CAP (pin 63) - A 220nF external capacitor is needed for the internal LDO regulator supplying the charge pump circuit.

These external capacitors should be placed as close as possible to the GS2985 pins and connected to ground with multiple vias.

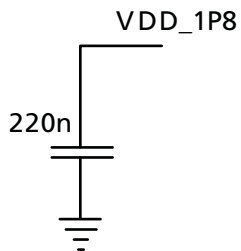


Figure 4-1: VDD_1P8

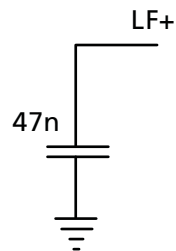


Figure 4-2: LF+

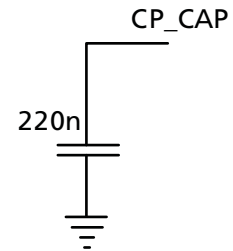


Figure 4-3: CP_CAP

5. Other Considerations

- Output pins should not be used to drive LEDs directly as they can only sink or source 100μA. Instead, LED drivers should be used
- Any unused DDI pin pairs should be connected to VCC through a 1kΩ resistor

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