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ODAS Serial Lines

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Product reference: P004, P026 & P005

Introduction

The purpose of this document is to explain voltage polarity in the Serial Lines of the ODAS system used with all Transmitting Microstructure Systems manufactured by RGL Consulting Ltd.

Line Polarity

Lines labeled TX+ and RX+. Pin label on driver and receiver chip is DO/RI.

Data Bits & Parity Bit

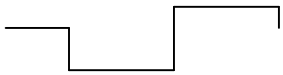
Address Pre-amble or Synch-bits. Sync = 1

= One

= Zero

Lines labeled TX- and RX-. Pin label on driver and receiver chip is DO*/RI*.

Data Bits & Parity Bit

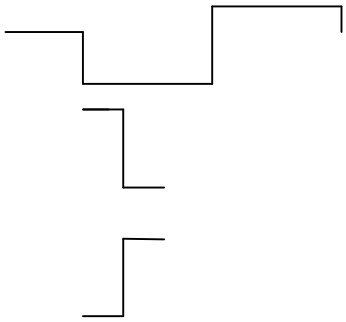


Address Pre-amble

= One

= Zero

Lines labeled TX+ and RX+. Pin label on driver and receiver chip is DO/RI.

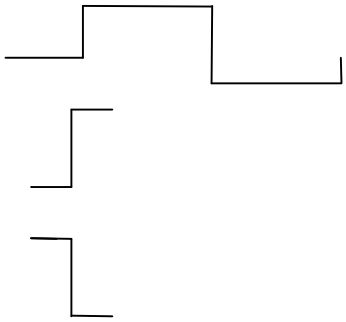


Data Pre-amble or sync bits. Sync = 0

= One

= Zero

Lines labeled TX- and RX-. Pin label on driver and receiver chip is DO*/RI*.



Data Pre-amble

= One

= Zero

NOTES:

1. RX+ and RX- are reverse labeled, on connector J4 of RTRANS P004R01 2003-01-08, with respect to RI and RI* of U7.
2. RX+ and RX- are correctly labeled, on connector J4 of RTRANS P004R01 2004-10-24 and later, with respect to RI and RI* of U7.
3. Labeling on UTRANS, P026R00, 2004-03-01 and later is correct and consistent with the labeling on the driver/receiver chips.
4. Labeling on J4 of RTRANS, P004R03, is correct and consistent with the labeling on the driver/receiver chips.

J4 RTRANS P004R01		
Pin #	Label	Function
1	TX-	DO*, Negative driver
2	TX+	DO, Positive Driver
3	RX-	RI*, Negative Driver
4	RX+	RI, Positive Driver
5	GND	Ground
6	GND	

J4 RTRANS P004R03		
Pin #	Label	Function
1	TX-	DO*, Negative driver
2	TX+	DO, Positive Driver
3	RX-	RI*, Negative Driver
4	RX+	RI, Positive Driver
5	Driver_Enable	For use by custom cable driver.
6	+5VDC	For use by custom cable driver.

7	GND	
8	GND	

7	GND	
8	GND	

5. The received signal (RO) from an RS-485 receiver goes directly to Unipolar_dat_In of the Manchester Decoder (without any inversion).
6. The received signal (RO) from an RS-485 receiver goes directly to the Xilinx chip (Serial_Man_Input) on RTRANS, P004R03, which has the Manchester II Encoder and Decoder programmed into this logic chip.
7. The mean voltage on both lines is 2.500 volts.
8. Lines go into high impedance after each word has been transmitted.

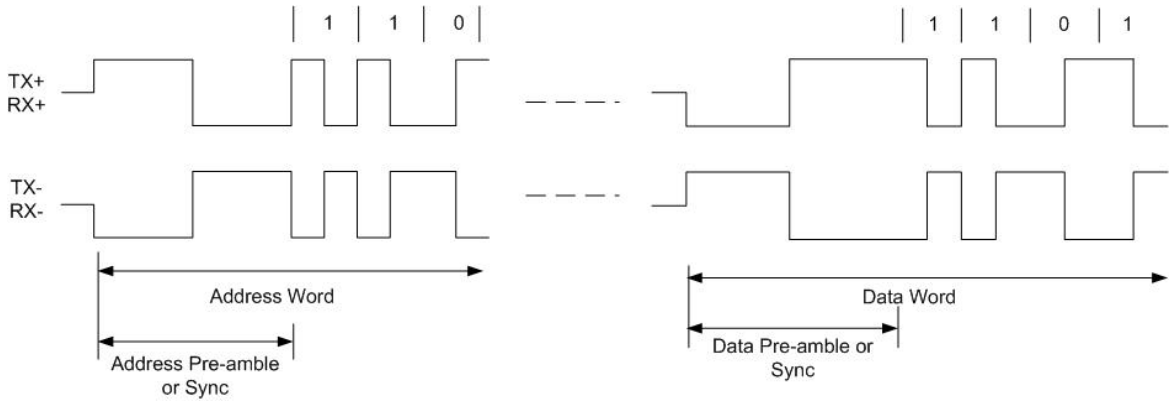


Figure 1. Summary of the transmit and receive line polarities for the ODAS serial communication system. A 3-bit pre-amble precedes all address and data words. This is sometimes called a “sync” bit. A pre-amble with a positive phase followed by a negative phase (on the TX+ and RX+ lines) identifies an address word. The opposite pre-amble identifies a data word. For both data and address words a positive phase followed by a negative phase indicates a bit value of 1. The opposite phasing indicates a bit value of 0. Address and data words are terminated by an odd parity bit (the sum of all bits, including the parity bit, must be odd). After the parity bit all lines go into a high impedance state. Lines should be terminated at both ends with a resistor that matches the characteristic impedance of the cable (usually, 120Ω).

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