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Bi-Directional Instrument Bus Protocol

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Product reference: P004, P006, P025, P026 & P029

Introduction

The purpose of this document is to explain the signaling protocol used with the 16-bit bi-directional Instrument Bus of the ODAS system. This bus is used with all instruments manufactured by RGL Consulting Ltd.

Overview

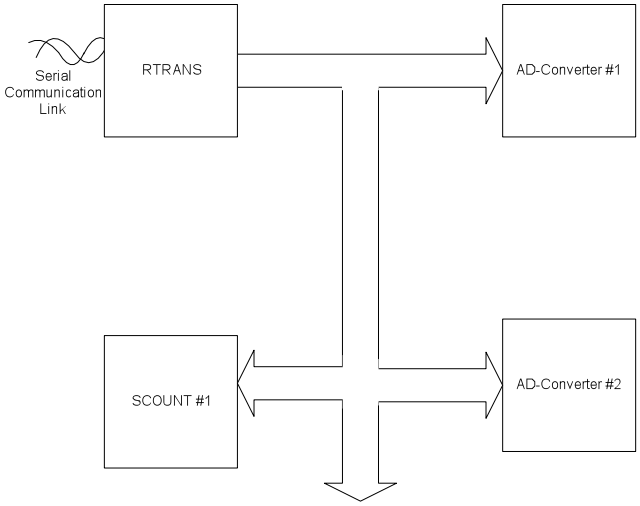

Figure 1. Overview of the ODAS Instrument Bus. This is a 16-bit bi-directional bus for transmitting address to peripheral devices. An address constitutes a request for a single 16-bit datum. A peripheral device responds by presenting its 16-bit data word. Currently supported devices are a 16-bit and 16-channel Analog-to-Digital converter and a frequency counter. The frequency counter is available in a 2-channel version (SCOUNT-2) and an 8-cheannel version (SCOUNT-8).

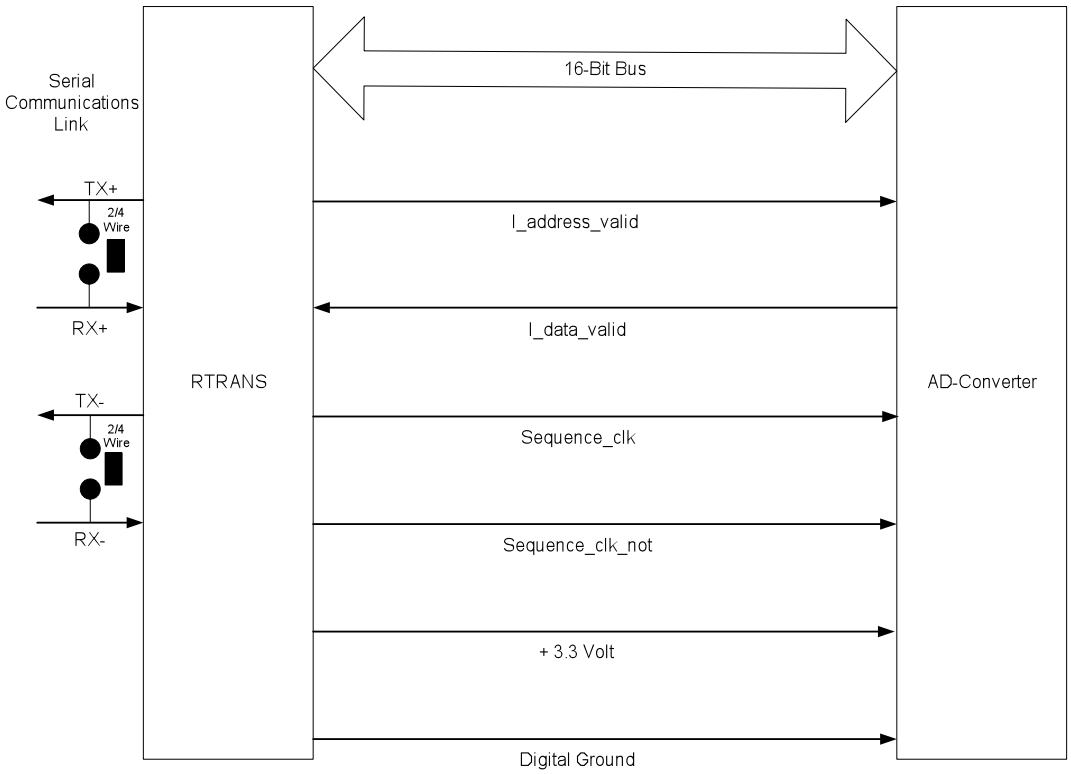

Figure 2. Detail of the ODAS Instrument Bus. The 16-bit bus is bi-directional and in a high-impedance state when not in use. There are 2 control lines. The rising edge of "I_address_valid" is used by peripheral devices to latch the address on the bus. RTRANS exclusively places addresses on the bus. The rising edge of "I_data_valid" is used by RTRANS to latch data placed on to the bus by a peripheral device. This control line is shared by all peripheral devices. The peripheral devices must place this line into high-impedance after the completion of a data transfer. The line is pulled high by a resistor on the RTRANS board. The sequence clock is used for timing activity. The inverse of the sequence clock is also place on to the bus to reduce EMI radiation. 3.3 volt power is also available for energizing peripheral devices.

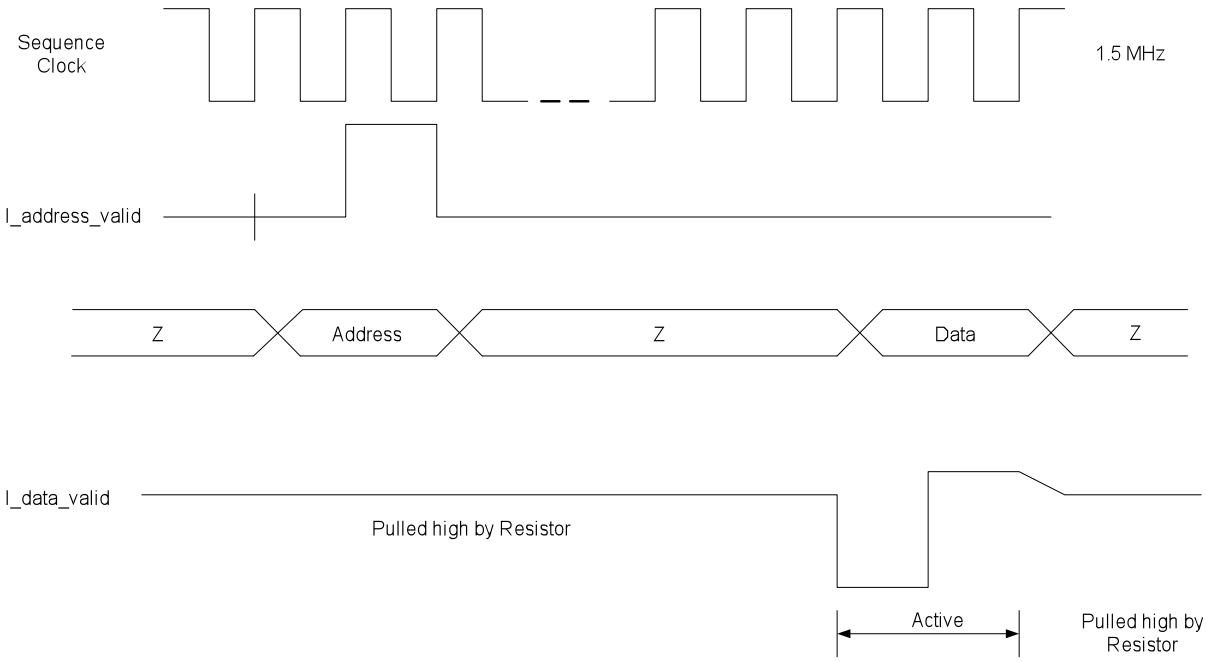

Figure 3. Timing detail of the Instrument Bus. Z indicates the high-impedance state. The bus is usually active for 2 cycles of the sequence clock. After RTRANS receives an address via the ODAS serial communication link, it places the address on to the 16-bit bus. The rising edge of "I_address_valid" should be used by peripheral devices to latch the addresses. Sometime later, one of the peripheral devices places a data word on to the bus. RTRANS uses the rising edge of "I_data_valid" to latch the datum. The datum are then transmitted over the serial communication link to the master computer (usually aboard a ship). The sequence clock typically runs at 1.5 MHz.

Details

Instrument Bus, IDC-26 Pin Connector (0.1 inch spacing) and Ribbon Cable			
#	Function	#	Function
1	Add(0), Data(0), Least Significant Bit	2	Add(1), Data(1)
3	Add(2), Data(2)	4	Add(3), Data(3)
5	Add(4), Data(4)	6	Add(5), Data(5)
7	Add(6), Data(6)	8	Add(7), Data(7)
9	Add(8), Data(8)	10	Add(9), Data(9)
11	Add(10), Data(10)	12	Add(11), Data(11)
13	Add(12), Data(12)	14	Add(13), Data(13)
15	Add(14), Data(14)	16	Add(15), Data(15), Most Significant Bit
17	I_data_valid	18	Data_transfered (not used)
19	I_address_valid	20	Digital Ground
21	Sequence_clk	22	Sequence_clk_not
23	Digital Ground	24	Digital Ground

25	3.3V Power	26	3.3V Power

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