

**DC Drive
Design Description
MBARI 5580DOC-1.20**

M B A R I



Related documentation:

DC Drive:

Schematic	5580SCH-1.20
Configuration Template	5580CFG-1.00
Assembly Notes	5580ASY-1.00

H-Bridge Output section:

Harris Semiconductor HIP4080A datasheet.
Harris Semiconductor AN9404.1 appnote.
International Rectifier IRFR120 datasheet.
The Berquist Co. Sil-Pad® Design Guide

DCD Motherboard:

Schematic	5581SCH-1.00
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Dave Wright, 29 April, 1998

Revisions

1st Draft 9/9/97

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Summary

The DC Drive module provides a power control function with an H-Bridge output topology. Bus voltages to 75V and currents to 5A are supported. Overload protection is built in and status indication, output current monitoring, signal conditioning for a position feedback potentiometer, and local power regulation are included. It is intended to be a component of a microprocessor based motor control system, providing power amplification, and fault protection independent of the controlling logic.

Background

The DC Drive module was developed to provide a method of controlling the small permanent magnet motor used in the antifouling “shutters” attached to the optical instruments on the moored platforms M1 and M2. While the requirements of the moored application are quite simple, it was thought wise to include features on the DC Drive module to allow PWM control of motor current by digital inputs, and provide an analog output of filtered current for use in closed loop control applications. Additionally, the output stage was designed to be capable of operation from the 50V. bus present on Tiburon, as well as from lower voltages found in battery powered systems.

Physical

The DC Drive module is a small PCB of 2.5” x 2.2” x 0.25” overall size. All components are surface mount and provision has been made for the attachment of a heatsink in high power applications. Mounting holes of 0.125” diameter, for 4-40 hardware, are found in each corner as well as adjacent to the power transistors. The choice of connectors is application dependent, accepting any 0.1”SIP pattern, allowing the module to be “piggybacked” on another PCB, or mounted standalone. For use in an OASIS can, a motherboard 5581PWB, provides a mating connector pattern for two modules, a common power connection, an IDC or discrete wire connector for control, and pluggable screw terminals for output connections. To facilitate a variety of mounting options, all mounting holes and connector pin locations register on a 0.1” grid to allow mounting on an IBC or other breadboard pattern.

Control

Control input signals consist of; **Run/Sense** for turning the module on and off and detecting an overload, **Direction** for the polarity of output current, and **PWM** for modulation of the highside transistors. The polarities of the PWM and Direction inputs are selectable by configuration pads to suit the application. The Run/Sense input is a bidirectional latching signal. To enable the module, drive the input high ($>4V@500\mu A$) for 1mS. Assuming no overload is present the module will power on, the input will latch itself high and the driving signal is permitted to go HiZ. The Run/Sense input will then remain weakly hi ($\sim 100\mu A@5V$) indicating the module is enabled. To disable the module, the input should be pulled low by the driving signal, and held there ($<1V@-1mA$). If an overload condition occurs while the module is enabled the overload latch will trip and disable the module. The external signal must then drive the input high again to re-enable the module. The Run/Sense signal may be monitored by the same microprocessor I/O port bit that controls the module, changing the mode from output to input to determine if an overload occurs. If the Run/Sense input is being held high when an overload occurs, the module output will be disabled, but internal circuitry will remain powered until Run/Sense is allowed to go low.

Power Supply

The DC Drive module employs four voltages for its operation. **Motor Power** is the high current input to the H-Bridge output stage, it can range from 0 to ~ 75 VDC, with current draw being application dependent. Internal to the module is **Drive Power** ~ 9.5 to ~ 12 VDC, for operation of the HIP4080 gate driver, and **A+5V** for the logic and overcurrent detection. Both internal voltages are usually provided by onboard regulators taking their input from the Motor Power bus, provided the input voltage is below 24V. For higher voltages, provision is made for supplying the driver voltage externally via the control input connector, J1. Separate from the overcurrent sensing circuit is the **Filtered Current** and **Feedback Conditioning** section, which is powered externally by a ~ 5 to ~ 20 VDC supply. This section was intentionally left separate to allow checking of the position feedback pot without powering up the entire motor drive. Quiescent current draw for the entire module is approximately 12mA for a 13VDC input to Motor Power and onboard regulation. Dissipation will increase with PWM, and is highly dependent on switching frequencies and the attached load.

Thermal

Quiescent dissipation of the drive section is approximately **150mW at 12VDC**, rising to 300mW at 24VDC due to onboard linear regulators. Dissipation of the output section can be estimated for DC as a worst case series resistance of $640m\Omega$, yielding **16W for a 5A load**. This is distributed among the two mosfets that are on at the time, and the current sense resistor at $100m\Omega$. At higher power levels heatsinking is required, and can be accomplished by clamping an appropriately shaped aluminum mass directly on top of the power transistor area of the PCB, using a Berquist Gap Pad V0™ thermally conductive gasket. Refer to the IRFR120 datasheet for derating at elevated case temperatures. For dynamic conditions during PWM operation the dissipation model becomes more complex. Mosfet gate capacitance and transition time losses begin to appear and make their contributions, and increase with higher switching rates. Refer to Harris AN9404.1 for a detailed analysis, and additionally take the empirical approach and measure input vs. output power under actual operating conditions. With respect to device maximum ratings, a general rule of “thumb” is that if a finger can be held on a device package without discomfort for an indefinite period, you are not likely to be pushing the limits. Just bear in mind that this is a first point of reference, not a substitute for analysis.

Circuit Walkthrough

Refer to the schematic for this discussion. Power enters via J3, and is conditioned by D4, a transient suppressor. Option jumper W2 allows selection of either J1 or J3 as the raw power source for onboard regulation. Q1 and Q3 form a simple switch to control power to the driver functions of the module. U2 and U4 are the linear regulators, with option jumpers W1 and W3 allowing for bypassing of onboard regulation should an external 12V regulated source be available via J1. U2 is programmed to provide $\sim 9.5V$ when operating on external power in the 10V to 24V range, whether from the J3 or J1 source. U4 provides 5V at low current for U3 and U1.

Circuit Walkthrough, cont.

U1 sections E and F form a latch with hysteresis, and in concert with Q1 and Q3 provides the power on/off and overcurrent trip function. From an initial condition of Q1 off, the external control signal at J1 pin 2 going high begins to drive Q1 into conduction via Q3. U3 pin 14 is also driven high by the external signal via R11, forcing the latch into the clear state as it powers up. Once the turn on is complete, the latch is capable of sourcing current via R11 to hold the module in the on state, and the external signal may be removed or allowed to go to a HiZ state. If the node formed by the junction of R12 and C14 is driven to ~2.75V by an overcurrent event, the latch will be set, the disable input of the mosfet driver will go true, the gate drive signals will go false, and if the external control signal is absent or in the HiZ state, the module will turn itself off.

R28 senses the H-Bridge load current, and U1B amplifies it by 10. U1A forms a comparator with hysteresis and an adjustable trip point. D2, R17, C4 and D1 form a filter that allows transients and motor startup surges to be ignored if desired. It's time constant of ~40mS was chosen for the OASIS shutter application, and should be reviewed for other loads to determine the appropriate values needed for adequate load and output stage protection. The values of sense resistor R28, and gain setting resistors R3 and R4, may be changed to suit the expected operating current for your application. As normally configured, variable resistor R9 allows adjustment of trip current over a ~100mA to 4A range.

Opamp U6 serves two functions. The upper section forms a buffer and filter for the load current signal generated by U1B. The values of feedback network components C9, R24 and R25 can be selected to filter PWM ripple components and present an average load current signal to an external A/D converter for closed loop control.

The lower section of U6 interfaces with a position sensing potentiometer in either a two wire or three wire configuration, selectable by W6 and W7. In the two wire mode it generates a linear 0.5V to 4.5V signal when used with a 5K pot in series with a 380Ω fixed resistor, the fixed resistor being included to differentiate between a shorted cable and the “zero” position. In three wire mode, it serves as a 5V (or other) reference voltage generator, the wiper terminal of the pot being connected directly to the signal pin of J3.

Inverter U3, sections A through D, buffer the incoming PWM and Direction signals, and via the programming pads W4 and W5 allow the selection of signal polarity. If PWM operation is not required, the input at J1 pin 4 may be left open, and W4 pins 2-3 selected to permanently enable the “highside” mosfets. U5 provides high current gate drive for the output transistors, and internal logic drives the correct transistors for the state of the direction and enable inputs, with “shoot through” protection included. Refer to the Harris HIP4080A datasheet and appnote for details on internal operation. Q2,4,5,6 are the output pass transistors, being N-channel mosfet devices rated at 7.7A. Id and 100V. breakdown.

Application Information

The DC Drive board can be operated in a number of modes including; **static**, **unipolar PWM**, **bipolar PWM**, and hybrids of all three.

In **static** operation the Run/Sense input is used as a simple on off switch, the direction input having been set before turn on. In this case the motor or other load receives full power at turn on, and remains powered until Run/Sense is brought low or an overcurrent occurs. This approach is useful for limiting the maximum output torque of a motor by setting the current trip level appropriately, and monitoring Run/Sense during operation to determine if a mechanical obstruction occurs. In this case the time constant of the trip circuit must be balanced between the duration of the motor startup surge and the maximum allowable time to respond to an overload.

In **unipolar PWM** operation, the “highside” mosfets may be modulated by a signal input at J1 pin 4. If frequent reversals of load current direction are not required this is more efficient than switching both the “upper” and “lower” mosfets at the same time. This mode can be used to actively regulate load current via open or closed loop methods, the filtered current output at J2 pin 3 being provided for that purpose. An example of an open loop case would be to “soft start” a motor by applying a precalculated PWM acceleration profile followed by a constant running value, to overcome startup current surges or mechanical shock. If unipolar operation is contemplated, pay specific attention to the bootstrap recharge (C6,C14) requirements with respect to your intended load.

Application Information, cont.

If it is desired to close a position or velocity loop around a motor or other actuator, then **bipolar PWM** is used to provide true current controlled operation. In this mode the PWM signal drives the Direction input at J1 pin 3, and the instantaneous output polarity follows the state of the input. For an input duty cycle of 50%, at a frequency that is high in relation to the $\Delta I/\Delta T$ characteristics of the load, the net effect is zero average current. As the duty cycle departs from 50%, the average current becomes nonzero, with the polarity being determined by whether the duty cycle has become greater or lesser than 50%, and the magnitude increasing as either 0% or 100% is approached. If the PWM signal is being generated by a microprocessor or hardwired logic, it is possible to adjust the load current and polarity on a moment by moment basis to achieve the desired mechanical output function. Note that the filtered current output signal is unipolar, and as such only represents current sourced to the load, regardless of polarity. Regenerative currents force the output signal to zero. This was done to simplify the overcurrent protection circuitry, at the expense of some loss of information.

When driving inductive loads such as motors or solenoid operated valves, consideration must be given to reactive currents. The body diode in each of the mosfets, in conjunction with the topology of the H-Bridge output stage, forms a bridge rectifier which directs all reactive and regenerative currents back to the supply bus. If the impedance of the supply bus is not low in relation to these currents, the bus voltage can be driven upwards, possibly to damaging levels. For this reason a transient suppressor diode, D4, has been placed across the Motor Power bus to clamp any short lived spikes that might occur. In the case of motor regeneration, the energy capacity of the suppressor may be exceeded in some applications. Careful analysis is required when driving high inertia mechanical loads, to insure that excess energy is adequately dealt with. For protection of the drive module, transients should be clamped at 80V maximum. If a large motor or other inductive load is being driven, the transient suppression should be placed at the load, rather than the module, to reduce EMI in the interconnecting wiring.

Proper operation of the “bootstrap” charge pump for the highside mosfets depends on the source terminal voltage going to zero (or slightly negative) during that transistors off time. For this reason, highly capacitive loads cannot be driven directly in PWM operation. The ideal case is some inductive reactance that will quickly “snap” the source terminal towards ground when the transistor turns off, thereby quickly recharging the bootstrap capacitor.

When low power or battery operation is contemplated, be aware that U2, the LM2931 regulator for the 9.5V drive power will drop out of regulation at ~300mV input-output differential. When this occurs, quiescent current consumption for the module will rise from ~15mA to ~90mA! It will continue to function in this state until the HIP4080A low voltage cutoff threshold of ~8.5V is reached. If the voltage is allowed to hover around the cutoff threshold, erratic operation or oscillation may occur.

At higher power levels it is very important to reduce the time constant of the overload trip circuit. Trip times should be consistent with the pulsed energy limits of the IFR120 pass transistors. See the datasheet for details

The drive module may be operated directly from the PWM outputs of the 87C196 microprocessor in either “fast” or “slow” mode. For the IBC or 3x5 micro operating at a 16MHz clock, the output frequencies are 31.5KHz or 15.36KHz. For OASIS at a 9.8304MHz clock, 19.2KHz or 9.6KHz are available. Duty cycles from 0 to 99.6% are available with 8 bit resolution. For other PWM sources, frequencies into the hundreds of kilohertz can be accommodated if the attached load will allow.

Component Values

Several component values can and should be changed depending on the power levels and type of operation desired.

REFERENCE	NOMINAL VALUE	OPTION
R28	100m Ω	50m Ω and 10m Ω , reduce dissipation at higher power levels
R4, R3	9.09K, 1K	Compensate for changing R28
R17, C4	200K, 0.22uf	Overcurrent time constant, must be reduced at high power
R24, R25, C9	10K, 10K, 0.18uf	Filtered current gain and rolloff to suit application
D4	15V	Motor Power transient voltage limit, <=75V.

Configuration Options

Several “jumpers” exist to support various options. The jumpers are programmed by shorting the adjacent pads with “blobs” of solder. PCB rev1.0 represented the first attempt at this method, and the gap is not optimal, requiring a large amount of solder. Be careful!

Jumpers: Defaults are marked by * for *static* operation, local regulation, Motor Power < 24VDC

REFERENCE	CONNECT	FUNCTION
W1	1-2 *	Use onboard 10V reg.
"	open	Disable 10V reg.
W2	1-2	Use J1 pin 5 as module power
"	2-3 *	Use Motor Power (J3) as module power
W3	1-2	Do not locally regulate module power
"	2-3 *	Regulate module power to 10V
W4	1-2	Highside PWM is active HI
"	2-3 *	Highside PWM is active LO
W5	1-2	Direction input HI is output A+ B-
"	2-3 *	Direction input LO is output A+ B-
W6	1-2	Position feedback pot in 3-wire mode
"	2-3*	Position feedback pot in 2-wire mode
W7	1-2	Position feedback pot in 3-wire mode
"	2-3*	Position feedback pot in 2-wire mode

Connector Pinouts

REFERENCE	FUNCTION	REFERENCE	FUNCTION
J1	Digital Control Inputs	J3	Motor Power Input
1	GND	1 & 2	GND
2	Run/Sense	3 & 4	Motor V+
3	Direction		
4	PWM	J4	Motor Drive Output
5	Module Power	1 & 2	“A” output
		3 & 4	“B” output
J2	Analog Outputs		
1	GND	J5	Feedback Pot Connections
2	Position pot output	1	CW terminal / GND
3	Filtered current output	2	Wiper
4	Analog V+ input	3	CCW terminal
		4	Analog V+ output

Checkout Procedure

Refer to latest schematic for any modifications relevant to PCB revision level you are working with.

Refer to configuration template and confirm that jumpers and component values are correct for intended application.

Connect current limited adjustable power supply to the input connector you have configured for module power, set current limit for 20mA, voltage to 12V. Confirm that no current is drawn when module is disabled. Enable module, confirm that module remains enabled when taking run/sense tristate, and that no more than 18mA of current is drawn. Confirm that output of U2 pin 1 is 9.5 to 9.8V, and output of U4 pin 1 is 4.75V to 5.25V. Confirm that taking run/sense low disables the module.

Enable module and adjust R9 for 500mV at U1 pin 8. Attach motor power supply (if different from module supply), assert PWM input true, and observe output connector J4 while taking direction input high and low. Confirm that the motor supply voltage appears on the correct pins for the state of the direction input.

Apply a resistive load to the module output and vary the motor voltage so as to cause 500mA to be drawn when enabled. Confirm that adjustment of the overload trip point can be made to occur at the desired level. Confirm that load current is identical in either direction, and that overload trip is not affected. Measure the overload trip response time and confirm it is appropriate to the application.

Apply power to the Analog V+ input, current should be $\ll \sim 1\text{mA}$. Observe the filtered current waveform at TP4 for static and PWM operation and confirm that the amplitude and ripple are as desired.

Connect a reference resistance value to the appropriate connections on J5 for the type of feedback potentiometer desired. Confirm that the output voltage at J2 pin 2 is correct for several reference resistance values.

TEST POINTS:

REFERENCE	FUNCTION
TP1	Enable/Sense control input
TP2	Feedback pot output signal
TP3	Raw Current
TP4	Filtered Current
TP5	GND

Notes:

[illegible]

END